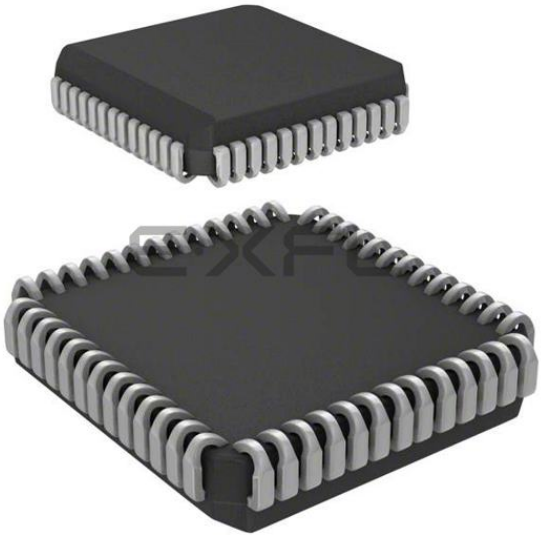

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	15KB (15K x 8)
Program Memory Type	OTP
EEPROM Size	256 x 8
RAM Size	352 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LCC (J-Lead)
Supplier Device Package	52-PLCC (19.1x19.1)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mchc705b16nvfne

MC68HC05B6

High-density Complementary Metal Oxide Semiconductor (HCMOS) Microcomputer Unit

7
PULSE LENGTH D/A CONVERTERS

8
ANALOG TO DIGITAL CONVERTER

9
RESETS AND INTERRUPTS

2.2 Serial RAM loader

The ‘load program in RAM and execute’ mode is entered if the following conditions are satisfied when the reset pin is released to V_{DD}. The format used is identical to the format used for the MC68HC805C4. The SEC bit in the options register must be inactive, i.e. set to ‘1’.

- $\overline{IRQ}$ at $2xV_{DD}$
- TCAP1 at V_{DD}
- PD3 at V_{DD} for at least 30 machine cycles after reset
- PD4 at V_{SS} for at least 30 machine cycles after reset

In the ‘load program in RAM and execute’ routine, user programs are loaded into MCU RAM via the SCI port and then executed. Data is loaded sequentially, starting at RAM location $0050, until the last byte is loaded. Program control is then transferred to the RAM program starting at location $0051. The first byte loaded is the count of the total number of bytes in the program plus the count byte. The program starts at the second byte in RAM. During the firmware initialization stage, the SCI is configured for the NRZ data format (idle line, start bit, eight data bits and stop bit). The baud rate is 9600 with a 4 MHz crystal. A program to convert ASCII S-records to the format required by the RAM loader is available from Freescale.

If immediate execution is not desired after loading the RAM program, it is possible to hold off execution. This is accomplished by setting the byte count to a value that is greater than the overall length of the loaded data. When the last byte is loaded, the firmware will halt operation expecting additional data to arrive. At this point, the reset switch is placed in the reset position which will reset the MCU, but keep the RAM program intact. All routines can now be entered from this state, including the one which will execute the program in RAM (see Section 2.3).

To load a program in the EEPROM, the ‘load program in RAM and execute’ function is also used. In this instance the process involves two distinct steps. Firstly, the RAM is loaded with a program which will control the loading of the EEPROM, and when the RAM contents are executed, the MCU is instructed to load the EEPROM.

The erased state of the EEPROM is $FF.

Figure 2-1 shows the schematic diagram of the circuit required for the serial RAM loader.

3.5 EEPROM

The user EEPROM consists of 256 bytes of memory located from address $0100 to $01FF. 255 bytes are general purpose and 1 byte is used by the option register. The non-volatile EEPROM is byte erasable.

An internal charge pump provides the EEPROM voltage (V_{PP1}), which removes the need to supply a high voltage for erase and programming functions. The charge pump is a capacitor/diode ladder network which will give a very high impedance output of around 20-30 MΩ. The voltage of the charge pump is visible at the VPP1 pin. During normal operation of the device, where programming/erasing of the EEPROM array will occur, VPP1 should never be connected to either VDD or VSS as this could prevent the charge pump reaching the necessary programming voltage. Where it is considered dangerous to leave VPP1 unconnected for reasons of excessive noise in a system, it may be tied to V_{DD}; this will protect the EEPROM data but will also increase power consumption, and therefore it is recommended that the protect bit function is used for regular protection of EEPROM data (see Section 3.5.5).

In order to achieve a higher degree of security for stored data, there is no capability for bulk or row erase operations.

The EEPROM control register ($0007) provides control of the EEPROM programming and erase operations.

Warning: The VPP1 pin should never be connected to VSS, as this could cause permanent damage to the device.

3.5.1 EEPROM control register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
EEPROM/ECLK control	$0007	0	0	0	0	ECLK	E1ERA	E1LAT	E1PGM	0000 0000

ECLK

See Section 4.3 for a description of this bit.

E1ERA — EEPROM erase/programming bit

Providing the E1LAT and E1PGM bits are at logic one, this bit indicates whether the access to the EEPROM is for erasing or programming purposes.

1 (set) – An erase operation will take place.

0 (clear) – A programming operation will take place.

Once the program/erase EEPROM address has been selected, E1ERA cannot be changed.

5
PROGRAMMABLE TIMER

The programmable timer on the MC68HC05B6 consists of a 16-bit read-only free-running counter, with a fixed divide-by-four prescaler, plus the input capture/output compare circuitry. The timer can be used for many purposes including measuring pulse length of two input signals and generating two output signals. Pulse lengths for both input and output signals can vary from several microseconds to many seconds. In addition, it works in conjunction with the pulse length modulation (PLM) system, which can also be referred to as the pulse width modulation system, to execute two 8-bit D/A PLM (pulse length modulation) conversions, with a choice of two repetition rates. The timer is also capable of generating periodic interrupts or indicating passage of an arbitrary multiple of four CPU cycles. A block diagram is shown in Figure 5-1, and timing diagrams are shown in Figure 5-2, Figure 5-3, Figure 5-4 and Figure 5-5.

The timer has a 16-bit architecture, hence each specific functional segment is represented by two 8-bit registers (except the PLMA and PLMB which use one 8-bit register for each). These registers contain the high and low byte of that functional segment. Accessing the low byte of a specific timer function allows full control of that function; however, an access of the high byte inhibits that specific timer function until the low byte is also accessed.

The 16-bit programmable timer is monitored and controlled by a group of sixteen registers, full details of which are contained in this section.

Note: A problem may arise if an interrupt occurs in the time between the high and low bytes being accessed. To prevent this, the I-bit in the condition code register (CCR) should be set while manipulating both the high and low byte register of a specific timer function, ensuring that an interrupt does not occur.

5.1 Counter

The key element in the programmable timer is a 16-bit, free-running counter or counter register, preceded by a prescaler that divides the internal processor clock by four. The prescaler gives the timer a resolution of 2μs if the internal bus clock is 2 MHz. The counter is incremented during the low portion of the internal bus clock. Software can read the counter at any time without affecting its value.

6.10 SCI synchronous transmission

The SCI transmitter allows the user to control a one way synchronous serial transmission. The SCLK pin is the clock output of the SCI transmitter. No clocks are sent to that pin during start bit and stop bit. Depending on the state of the LBCL bit (bit 0 of SCCR1), clocks will or will not be activated during the last valid data bit (address mark). The CPOL bit (bit 2 of SCCR1) allows the user to select the clock polarity, and the CPHA bit (bit 1 of SCCR1) allows the user to select the phase of the external clock (see Figure 6-8, Figure 6-9 and Figure 6-10).

During idle, preamble and send break, the external SCLK clock is not activated.

These options allow the user to serially control peripherals which consist of shift registers, without losing any functions of the SCI transmitter which can still talk to other SCI receivers. These options do not affect the SCI receiver which is independent of the transmitter.

The SCLK pin works in conjunction with the TDO pin. When the SCI transmitter is disabled (TE = 0), the SCLK and TDO pins go to the high impedance state.

Note: The LBCL, CPOL and CPHA bits have to be selected before enabling the transmitter to ensure that the clocks function correctly. These bits should not be changed while the transmitter is enabled.

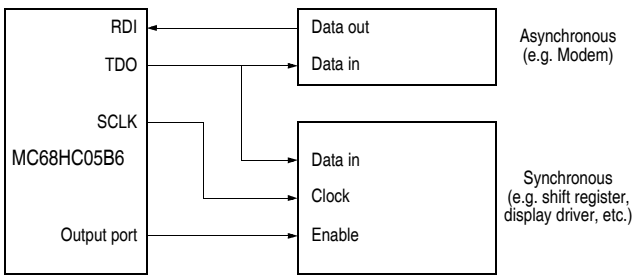

Figure 6-8 SCI example of synchronous and asynchronous transmission

ADON — A/D converter on

The ADON bit allows the user to enable/disable the A/D converter.

1 (set) – A/D converter is switched on.

0 (clear) – A/D converter is switched off.

When the A/D converter is switched on, it takes a time t_{ADON} for the current sources to stabilize (see Table 11-6 and Table 11-7). Using the A/D converter before this time has elapsed may result in the incorrect operation of the A/D, even after t_{ADON} has elapsed. In this case ADON would have to be cleared and set again.

Power-on or external reset will clear the ADON bit, thus disabling the A/D converter.

CH3–CH0 — A/D channels 3, 2, 1 and 0

The CH3–CH0 bits allow the user to determine which channel of the A/D converter multiplexer is selected. See Table 8-2 for channel selection.

Reset clears the CH0–CH3 bits.

Table 8-2 A/D channel assignment

CH3	CH2	CH1	CH0	Channel selected
0	0	0	0	AN0
0	0	0	1	AN1
0	0	1	0	AN2
0	0	1	1	AN3
0	1	0	0	AN4
0	1	0	1	AN5
0	1	1	0	AN6
0	1	1	1	AN7
1	0	0	0	VRH pin (high)
1	0	0	1	(VRH + VRL) / 2
1	0	1	0	VRL pin (low)
1	0	1	1	VRL pin (low)
1	1	0	0	VRL pin (low)
1	1	0	1	VRL pin (low)
1	1	1	0	VRL pin (low)
1	1	1	1	VRL pin (low)

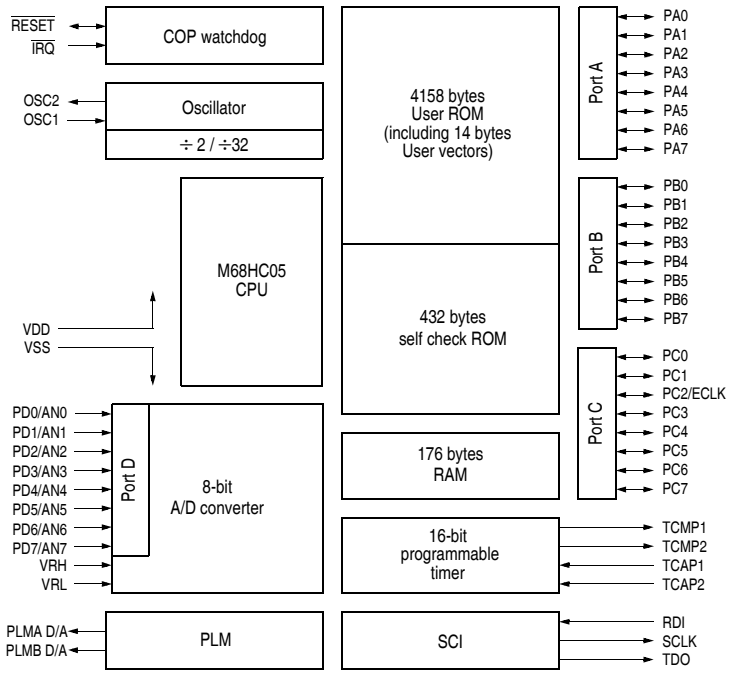

Figure A-1 MC68HC05B4 block diagram

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Table D-1 Mode of operation selection

$\overline{IRQ}$ pin	TCAP1 pin	PD3	PD4	Mode
V_{SS} to V_{DD}	V_{SS} to V_{DD}	X	X	Single chip
$2V_{DD}$	V_{DD}	0	X	Self check
$2V_{DD}$	V_{DD}	1	0	Serial RAM loader
$2V_{DD}$	V_{DD}	1	1	Jump to any address

D.2 Self-check routines

The self-check routines for the MC68HC05B16 are identical to those of the MC68HC05B4 with the following exception.

The count byte on the MC68HC05B16 can be any value up to 256 ($00). The first 176 bytes are loaded into RAM I and the remainder is loaded into RAM II starting at $0250.

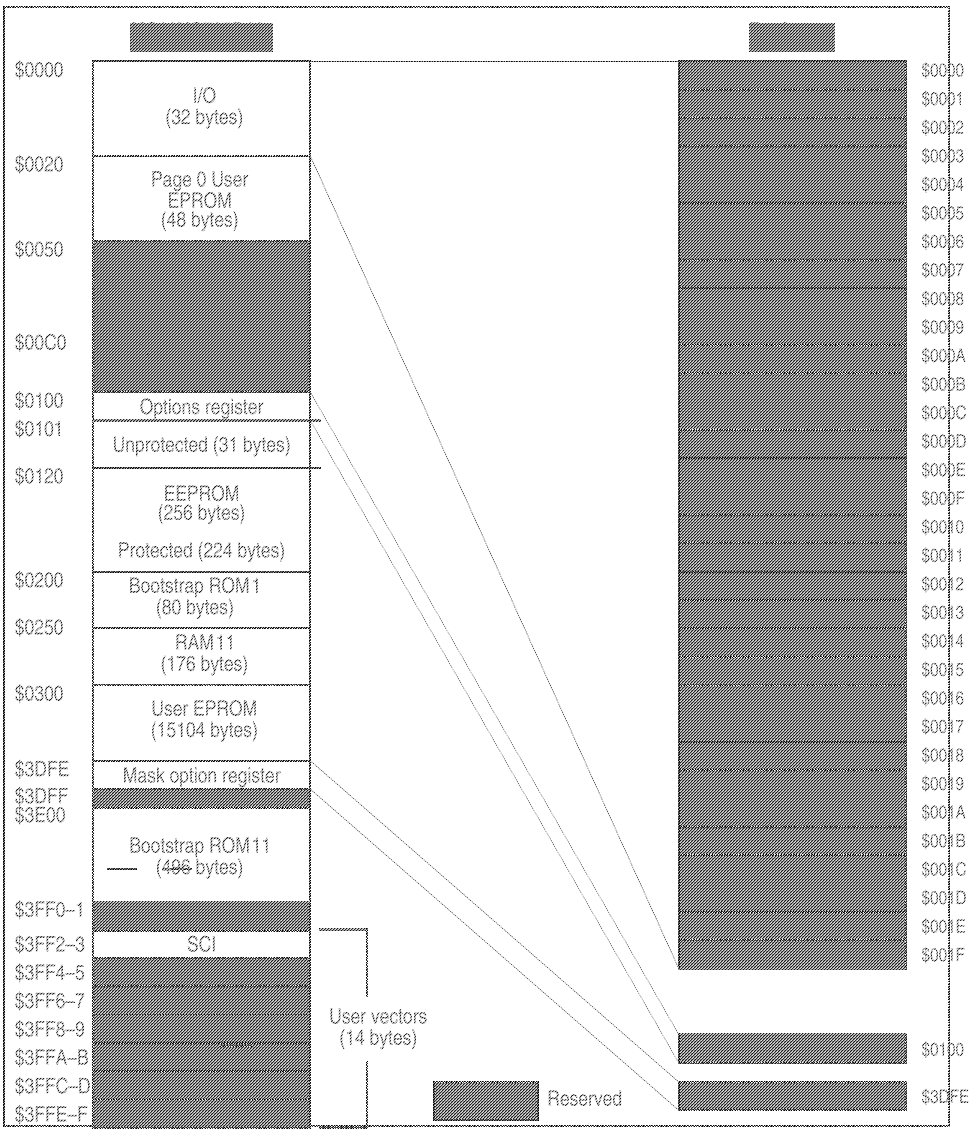
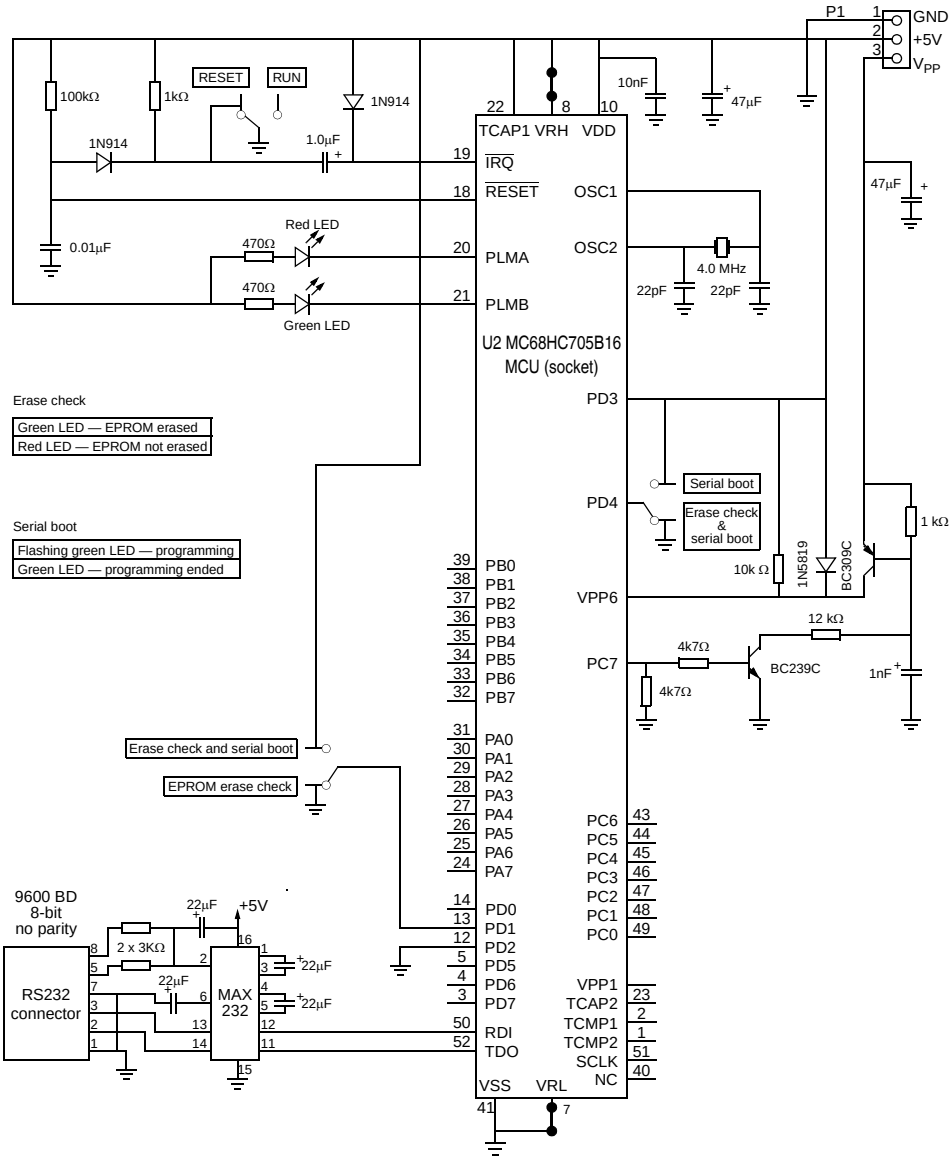


Figure E-2 Memory map of the MC68HC705B16



Note: A minimum V_{DD} voltage must be applied to the VPP6 pin at all times, including power-on, as a lower voltage could damage the device. Unless otherwise stated, EPROM programming is guaranteed at ambient (25°C) temperature only

Figure E-8 RAM/EPROM/EEPROM serial bootstrap schematic diagram

E.7 A/D converter characteristics

Table E-9 A/D characteristics for 5V operation

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Parameter	Min	Max	Unit
Resolution	Number of bits resolved by the A/D	8	—	Bit
Non-linearity	Max deviation from the best straight line through the A/D transfer characteristics ($V_{RH} = V_{DD}$ and V_{RL} = 0V)	—	± 0.5	LSB
Quantization error	Uncertainty due to converter resolution	—	± 0.5	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale equivalent of the binary code output code for all errors	—	± 1	LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
V_{RH}	Maximum analog reference voltage	V_{RL}	V_{DD} + 0.1	V
V_{RL}	Minimum analog reference voltage	V_{SS} – 0.1	V_{RH}	V
ΔV_R(1)	Minimum difference between V_{RH} and V_{RL}	3	—	V
Conversion time	Total time to perform a single analog to digital conversion a. External clock (OSC1, OSC2) b. Internal RC oscillator	 — —	 32 32	 t_{CYC} µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	GUARANTEED		
Zero input reading	Conversion result when $V_{IN} = V_{RL}$	00	—	Hex
Full scale reading	Conversion result when $V_{IN} = V_{RH}$	—	FF	Hex
Sample acquisition time	Analog input acquisition sampling a. External clock (OSC1, OSC2) b. Internal RC oscillator(2)	 — —	 12 12	 t_{CYC} µs
Sample/hold capacitance	Input capacitance on PD0/AN0–PD7/AN7	—	12	pF
Input leakage(3)	Input leakage on A/D pins PD0/AN0–PD7/AN7, VRL, VRH	—	1	µA

(1) Performance verified down to 2.5V ΔVR, but accuracy is tested and guaranteed at ΔVR = 5V±10%.

(2) Source impedances greater than 10kΩ will adversely affect internal charging time during input sampling.

(3) The external system error caused by input leakage current is approximately equal to the product of R source and input current. Input current to A/D channel will be dependent on external source impedance (see Figure 8-2).

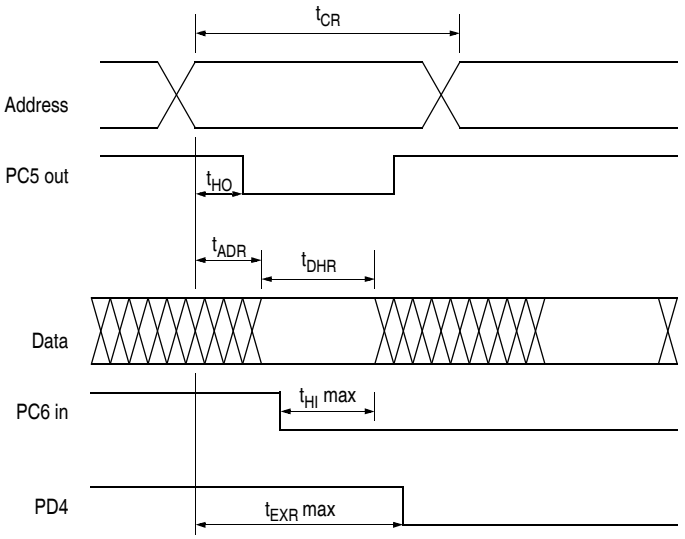
E.8 Control timing

Table E-11 Control timing for 5V operation

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation				
Crystal option	f_{OSC}	—	4.2	MHz
External clock option	f_{OSC}	dc	4.2	MHz
Internal operating frequency (f_{OSC}/2)				
Using crystal	f_{OP}	dc	2.1	MHz
Using external clock	f_{OP}	dc	2.1	MHz
Cycle time (see Figure 9-1)	t_{CYC}	480	—	ns
Crystal oscillator start-up time (see Figure 9-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
RC oscillator stabilization time	t_{ADRC}		5	µs
A/D converter stabilization time	t_{ADON}		500	µs
External RESET input pulse width	t_{RL}	1.5	—	t_{CYC}
Power-on RESET output pulse width				
4064 cycle	t_{PORL}	4064	—	t_{CYC}
16 cycle	t_{PORL}	16	—	t_{CYC}
Watchdog RESET output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EEPROM byte erase time				
0 to 70 (standard)	t_{ERA}	10	—	ms
– 40 to 85 (extended)	t_{ERA}	10	—	ms
– 40 to 105 (industrial)	t_{ERA}	10	—	ms
– 40 to 125 (automotive)	t_{ERA}	10	—	ms
EEPROM byte program time(1)				
0 to 70 (standard)	t_{PROG}	10	—	ms
– 40 to 85 (extended)	t_{PROG}	10	—	ms
– 40 to 105 (industrial)	t_{PROG}	15	—	ms
– 40 to 125 (automotive)	t_{PROG}	20	—	ms
Timer (see Figure E-11)				
Resolution(2)	t_{RESL}	4	—	t_{CYC}
Input capture pulse width	t_{TH}, t_{TL}	125	—	ns
Input capture pulse period	t_{TLTL}	—(3)	—	t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	125	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width(5)	t_{OH}, t_{OL}	90	—	ns
Write/Erase endurance(6)(7)	—	10000		cycles
Data retention(6)(7)	—	10		years

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.
(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{CYC}), this is the limiting factor in determining the timer resolution.
(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.
(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.
(5) t_{OH} and t_{OL} should not total less than 238ns.
(6) At a temperature of 85°C
(7) Refer to Reliability Monitor Report (current quarterly issue) for current failure rate information.



t_{ADR} max (address to data delay; PC6=PC5)	16 machine cycles
t_{DHR} min (data hold time)	4 machine cycles
t_{CR} (load cycle time; PC6=PC5)	49 machine cycles
t_{HO} (PC5 handshake out delay)	5 machine cycles
t_{HI} max (PC6 handshake in, data hold time)	10 machine cycles
t_{EXR} max (max delay for transition to be recognised during this cycle; PC6=PC5	30 machine cycles

1 machine cycle = $1/(2f_0(Xtal))$

Figure F-9 Parallel RAM loader timing diagram

Table G-1 Register outline

Register name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data (PORTA)	$0000									Undefined
Port B data (PORTB)	$0001									Undefined
Port C data (PORTC)	$0002						PC2/ ECLK			Undefined
Port D data (PORTD)	$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Undefined
Port A data direction (DDRA)	$0004									0000 0000
Port B data direction (DDRB)	$0005									0000 0000
Port C data direction (DDRC)	$0006									0000 0000
EEPROM/ECLK control	$0007	0	0	0	0	ECLK	E1ERA	E1LAT	E1PGM	0000 0000
A/D data (ADDATA)	$0008									0000 0000
A/D status/control (ADSTAT)	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000
Pulse length modulation A (PLMA)	$000A									0000 0000
Pulse length modulation B (PLMB)	$000B									0000 0000
Miscellaneous	$000C	POR(1)	INTP	INTN	INTE	SFA	SFB	SM	WDOG(2)	?001 000?
SCI baud rate (BAUD)	$000D	SPC1	SPC0	SCT1	SCT0	SCT0	SCR2	SCR1	SCR0	00uu uuuu
SCI control 1 (SCCR1)	$000E	R8	T8		M	WAKE	CPOL	CPHA	LBCL	Undefined
SCI control 2 (SCCR2)	$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000
SCI status (SCSR)	$0010	TDRE	TC	RDRF	IDLE	OR	NF	FE		1100 000u
SCI data (SCDR)	$0011									0000 0000
Timer control (TCR)	$0012	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLVL1	0000 00u0
Timer status (TSR)	$0013	ICF1	OCF1	TOF	ICF2	OCF2				Undefined
Input capture high 1	$0014									Undefined
Input capture low 1	$0015									Undefined
Output compare high 1	$0016									Undefined
Output compare low 1	$0017									Undefined
Timer counter high	$0018									1111 1111
Timer counter low	$0019									1111 1100
Alternate counter high	$001A									1111 1111
Alternate counter low	$001B									1111 1100
Input capture high 2	$001C									Undefined
Input capture low 2	$001D									Undefined
Output compare high 2	$001E									Undefined
Output compare low 2	$001F									Undefined
Options (OPTR)(3)	$0100							EE1P	SEC	Not affected
Mask option register (MOR)(4)	$7FDE				RTIM	RWAT	WWAT	PBPD	PCPD	Not affected

(1) This bit is set each time there is a power-on reset.

(2) The state of the WDOG bit after reset is dependent upon the mask option selected; 1 = watchdog enabled, 0 = watchdog disabled.

(3) This register is implemented in EEPROM; therefore reset has no effect on the individual bits.

(4) This register is implemented in ROM; therefore reset has no effect on the individual bits.

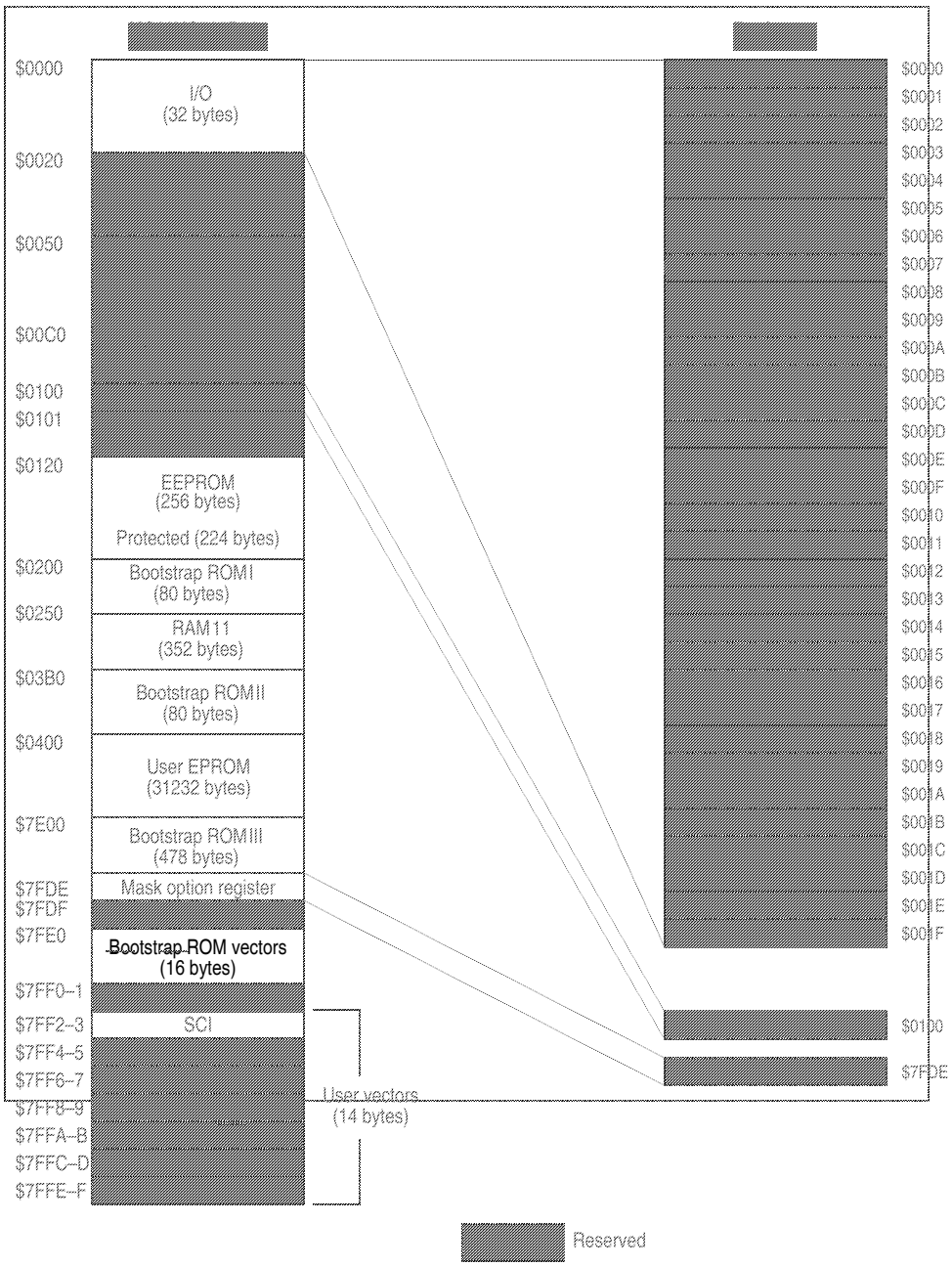


Figure H-2 Memory map of the MC68HC705B32

GLOSSARY

This section contains abbreviations and specialist words used in this data sheet and throughout the industry. Further information on many of the terms may be gleaned from Freescale's ***M68HC11 Reference Manual, M68HC11RM/AD***, or from a variety of standard electronics text books.

$xxxx	The digits following the '$' are in hexadecimal format.
%xxxx	The digits following the '%' are in binary format.
A/D, **ADC**	Analog-to-digital (converter).
Bootstrap mode	In this mode the device automatically loads its internal memory from an external source on reset and then allows this program to be executed.
Byte	Eight bits.
CCR	Condition codes register; an integral part of the CPU.
CERQUAD	A ceramic package type, principally used for EPROM and high temperature devices.
Clear	'0' — the logic zero state; the opposite of 'set'.
CMOS	Complementary metal oxide semiconductor. A semiconductor technology chosen for its low power consumption and good noise immunity.
COP	Computer operating properly. *aka* 'watchdog'. This circuit is used to detect device runaway and provide a means for restoring correct operation.
CPU	Central processing unit.
D/A, DAC	Digital-to-analog (converter).
EEPROM	Electrically erasable programmable read only memory. *aka* 'EEROM'.
EPROM	Erasable programmable read only memory. This type of memory requires exposure to ultra-violet wavelengths in order to erase previous data. *aka* 'PROM'.
ESD	Electrostatic discharge.
Expanded mode	In this mode the internal address and data bus lines are connected to external pins. This enables the device to be used in much more complex systems, where there is a need for external memory for example.