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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	256 x 8
RAM Size	528 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	56-SDIP (0.600", 15.24mm)
Supplier Device Package	56-PSDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/xc705b32cbe

MC68HC05B6

High-density Complementary Metal Oxide Semiconductor (HCMOS) Microcomputer Unit

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Table 3-2 Register outline

Register name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data (PORTA)	$0000									Undefined
Port B data (PORTB)	$0001									Undefined
Port C data (PORTC)	$0002						PC2/ ECLK			Undefined
Port D data (PORTD)	$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Undefined
Port A data direction (DDRA)	$0004									0000 0000
Port B data direction (DDRB)	$0005									0000 0000
Port C data direction (DDRC)	$0006									0000 0000
EEPROM/ECLK control	$0007	0	0	0	0	ECLK	E1ERA	E1LAT	E1PGM	0000 0000
A/D data (ADDATA)	$0008									0000 0000
A/D status/control (ADSTAT)	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000
Pulse length modulation A (PLMA)	$000A									0000 0000
Pulse length modulation B (PLMB)	$000B									0000 0000
Miscellaneous	$000C	POR(1)	INTP	INTN	INTE	SFA	SFB	SM	WDOG(2)	?001 000?
SCI baud rate (BAUD)	$000D	SPC1	SPC0	SCT1	SCT0	SCT0	SCR2	SCR1	SCR0	00uu uuuu
SCI control 1 (SCCR1)	$000E	R8	T8		M	WAKE	CPOL	CPHA	LBCL	Undefined
SCI control 2 (SCCR2)	$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000
SCI status (SCSR)	$0010	TDRE	TC	RDRF	IDLE	OR	NF	FE		1100 000u
SCI data (SCDR)	$0011									0000 0000
Timer control (TCR)	$0012	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLVL1	0000 00u0
Timer status (TSR)	$0013	ICF1	OCF1	TOF	ICF2	OCF2				Undefined
Input capture high 1	$0014									Undefined
Input capture low 1	$0015									Undefined
Output compare high 1	$0016									Undefined
Output compare low 1	$0017									Undefined
Timer counter high	$0018									1111 1111
Timer counter low	$0019									1111 1100
Alternate counter high	$001A									1111 1111
Alternate counter low	$001B									1111 1100
Input capture high 2	$001C									Undefined
Input capture low 2	$001D									Undefined
Output compare high 2	$001E									Undefined
Output compare low 2	$001F									Undefined
Options (OPTR)(3)	$0100							EE1P	SEC	Not affected

(1) The POR bit is set each time there is a power-on reset.

(2) The state of the WDOG bit after reset is dependent on the mask option selected; 1=watchdog enabled, 0=watchdog disabled.

(3) This register is implemented in EEPROM; therefore reset has no effect on the individual bits.

ICF2 — Input capture flag 2

This bit is set when a negative edge is detected by the input capture edge detector 2 at TCAP2; an input capture interrupt will be generated if ICIE is set. ICF2 is cleared by reading the TSR and then the input capture low register 2 ($1D).

1 (set) – A valid (negative) input capture has occurred.

0 (clear) – No input capture has occurred.

OCF2 — Output compare flag 2

This bit is set when the output compare 2 register contents match those of the free-running counter; an output compare interrupt will be generated if OCIE is set. OCF2 is cleared by reading the TSR and then reading or writing the output compare 2 low register ($1F).

1 (set) – A valid output compare has occurred.

0 (clear) – No output compare has occurred.

5.3 Input capture

'Input capture' is a technique whereby an external signal is used to trigger a read of the free running counter. In this way it is possible to relate the timing of an external signal to the internal counter value, and hence to elapsed time.

There are two input capture registers: input capture register 1 (ICR1) and input capture register 2 (ICR2).

The same input capture interrupt enable bit (ICIE) is used for the two input captures.

5.3.1 Input capture register 1 (ICR1)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Input capture high 1	$0014									Undefined
Input capture low 1	$0015									Undefined

The two 8-bit registers that make up the 16-bit input capture register 1 are read-only, and are used to latch the value of the free-running counter after the input capture edge detector circuit 1 senses a valid transition at TCAP1. The level transition that triggers the counter transfer is defined by the input edge bit (IEDG1). When an input capture 1 occurs, the corresponding flag ICF1 in TSR is set. An interrupt can also accompany an input capture 1 provided the ICIE bit in TCR is set. The 8 most significant bits are stored in the input capture high 1 register at $14, the 8 least significant bits in the input capture low 1 register at $15.

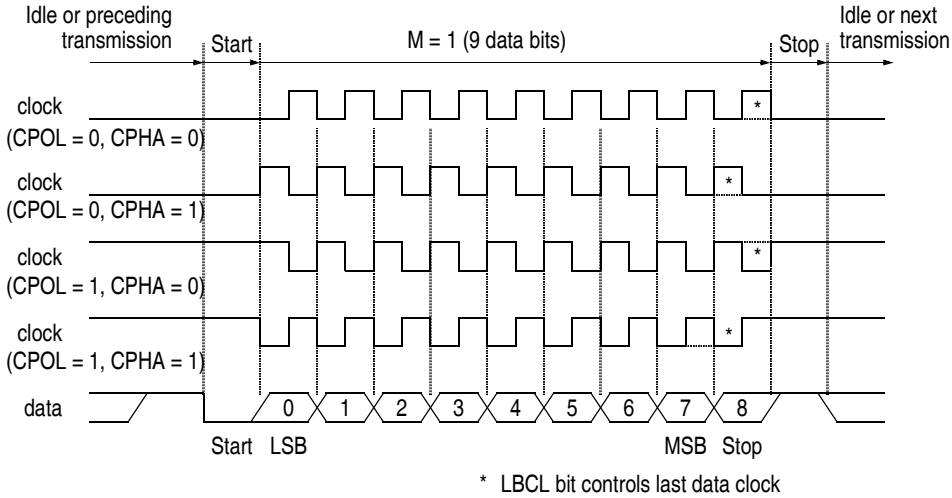


Figure 6-10 SCI data clock timing diagram (M=1)

LBCL – Last bit clock

This bit allows the user to select whether the clock associated with the last data bit transmitted (MSB) has to be output to the SCLK pin. The clock of the last data bit is output to the SCLK pin if the LBCL bit is a logic one, and is not output if it is a logic zero.

The last bit is the 8th or 9th data bit transmitted depending on the 8 or 9 bit format selected by M-bit (seeTable 6-2).

This bit should not be manipulated while the transmitter is enabled.

Table 6-2 SCI clock on SCLK pin

Data format	M-bit	LBCL bit	Number of clocks on SCLK pin
8 bit	0	0	7
8 bit	0	1	8
9 bit	1	0	8
9 bit	1	1	9

Table 6-6 SCI baud rate selection

							Crystal frequency – f_{OSC} (MHz)				
SCP1	**SCP0**	**SCT/R2**	**SCT/R1**	**SCT/R0**	**NP**	**NT/NR**	**4.194304**	**4.00**	**2.4576**	**2.00**	**1.8432**
0	0	0	0	0	1	1	131072	125000	76800	62500	57600
0	0	0	0	1	1	2	65536	62500	38400	31250	28800
0	0	0	1	0	1	4	32768	31250	19200	15625	14400
0	0	0	1	1	1	8	16384	15625	9600	7813	7200
0	0	1	0	0	1	16	8192	7813	4800	3906	3600
0	0	1	0	1	1	32	4096	3906	2400	1953	1800
0	0	1	1	0	1	64	2048	1953	1200	977	900
0	0	1	1	1	1	128	1024	977	600	488	450
0	1	0	0	0	3	1	43691	41667	25600	20833	19200
0	1	0	0	1	3	2	21845	20833	12800	10417	9600
0	1	0	1	0	3	4	10923	10417	6400	5208	4800
0	1	0	1	1	3	8	5461	5208	3200	2604	2400
0	1	1	0	0	3	16	2731	2604	1600	1302	1200
0	1	1	0	1	3	32	1365	1302	800	651	600
0	1	1	1	0	3	64	683	651	400	326	300
0	1	1	1	1	3	128	341	326	200	163	150
1	0	0	0	0	4	1	32768	31250	19200	15625	14400
1	0	0	0	1	4	2	16384	15625	9600	7813	7200
1	0	0	1	0	4	4	8192	7813	4800	3906	3600
1	0	0	1	1	4	8	4096	3906	2400	1953	1800
1	0	1	0	0	4	16	2048	1953	1200	977	900
1	0	1	0	1	4	32	1024	977	600	488	450
1	0	1	1	0	4	64	512	488	300	244	225
1	0	1	1	1	4	128	256	244	150	122	113
1	1	0	0	0	13	1	10082	9615	5908	4808	4431
1	1	0	0	1	13	2	5041	4808	2954	2404	2215
1	1	0	1	0	13	4	2521	2404	1477	1202	1108
1	1	0	1	1	13	8	1260	1202	738	601	554
1	1	1	0	0	13	16	630	601	369	300	277
1	1	1	0	1	13	32	315	300	185	150	138
1	1	1	1	0	13	64	158	150	92	75	69
1	1	1	1	1	13	128	79	75	46	38	35

Note: The examples shown above do not apply when the part is operating in slow mode (see Section 2.4.3).

10.3.4 Extended

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode byte. Instructions with extended addressing mode are capable of referencing arguments anywhere in memory with a single three-byte instruction. When using the Freescale assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler automatically selects the short form of the instruction.

EA = (PC+1):(PC+2); PC ← PC+3
Address bus high ← (PC+1); Address bus low ← (PC+2)

10.3.5 Indexed, no offset

In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. This addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is often used to move a pointer through a table or to hold the address of a frequently referenced RAM or I/O location.

EA = X; PC ← PC+1
Address bus high ← 0; Address bus low ← X

10.3.6 Indexed, 8-bit offset

In the indexed, 8-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the unsigned byte following the opcode. Therefore the operand can be located anywhere within the lowest 511 memory locations. This addressing mode is useful for selecting the mth element in an n element table.

EA = X+(PC+1); PC ← PC+2
Address bus high ← K; Address bus low ← X+(PC+1)
where K = the carry from the addition of X and (PC+1)

10.3.7 Indexed, 16-bit offset

In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This address mode can be used in a manner similar to indexed, 8-bit offset except that this three-byte instruction allows tables to be anywhere in memory. As with direct and extended addressing, the Freescale assembler determines the shortest form of indexed addressing.

EA = X+[(PC+1):(PC+2)]; PC ← PC+3
Address bus high ← (PC+1)+K; Address bus low ← X+(PC+2)
where K = the carry from the addition of X and (PC+2)

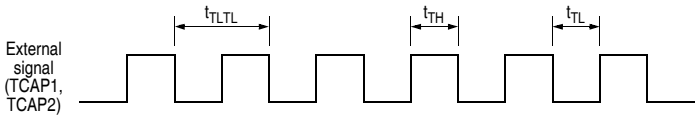
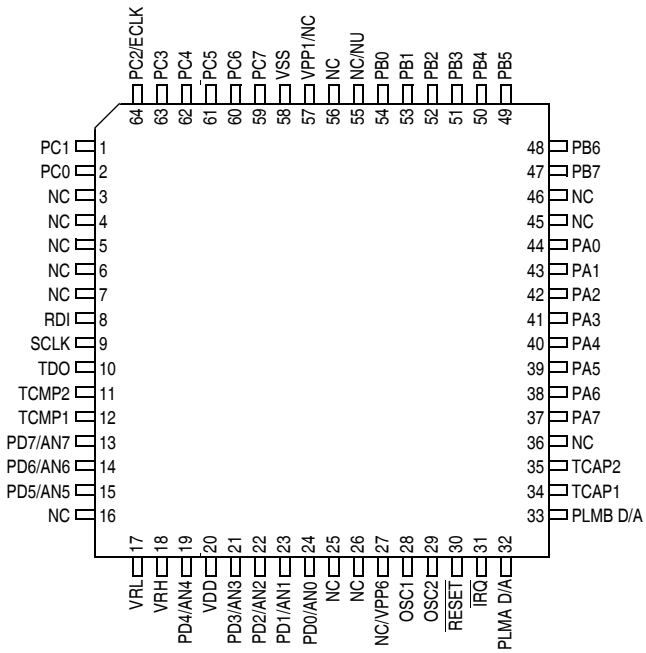


Figure 11-13 Timer relationship

12.1.2 64-pin quad flat pack (QFP)



Device	Pin 27	Pin 55	Pin 57
MC68HC05B4	NC	NC	NC
MC68HC05B6 MC68HC05B8 MC68HC05B16 MC68HC05B32	NC	NC	VPP1
MC68HC705B5	Not available in this package		
MC68HC705B16	VPP6	NU	VPP1
MC68HC705B16N	VPP6	NU	VPP1
MC68HC705B32	VPP6	NC	VPP1

NC = Not connected

NU = Non-user pin (Should be tied to V_{SS} in an electrically noisy environment)

Figure 12-2 64-pin QFP pinout for the MC68HC05B6

C.4 Options register (OPTR)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Options (OPTR)(1)	$1EFE		EPP	0	RTIM	RWAT	WWAT	PBPD	PCPD	Not affected

(1) This register is implemented in EPROM, therefore reset has no effect on the state of the individual bits.

Note: This register can only be written to while the device is in bootloader mode.

Bit 7 — Factory use only

Warning: This bit is strictly for factory use only and will always read zero to avoid accidental damage to the device. Any attempt to write to this bit could result in physical damage.

EPP — EPROM protect

This bit protects the contents of the main EPROM against accidental modification; it has no effect on reading or executing code in the EPROM.

1 (set) – EPROM contents are protected.

0 (clear) – EPROM contents are not protected.

RTIM — Reset time

This bit can modify t_{PORL}, i.e. the time that the $\overline{\text{RESET}}$ pin is kept low following a power-on reset. This feature is handled in the ROM part via a mask option.

1 (set) – t_{PORL} = 16 cycles.

0 (clear) – t_{PORL} = 4064 cycles.

RWAT — Watchdog after reset

This bit can modify the status of the watchdog counter after reset.

1 (set) – The watchdog will be active immediately following power-on or external reset (except in bootstrap mode).

0 (clear) – The watchdog system will be disabled after power-on or external reset.

WWAT — Watchdog during WAIT mode

This bit can modify the status of the watchdog counter during WAIT mode.

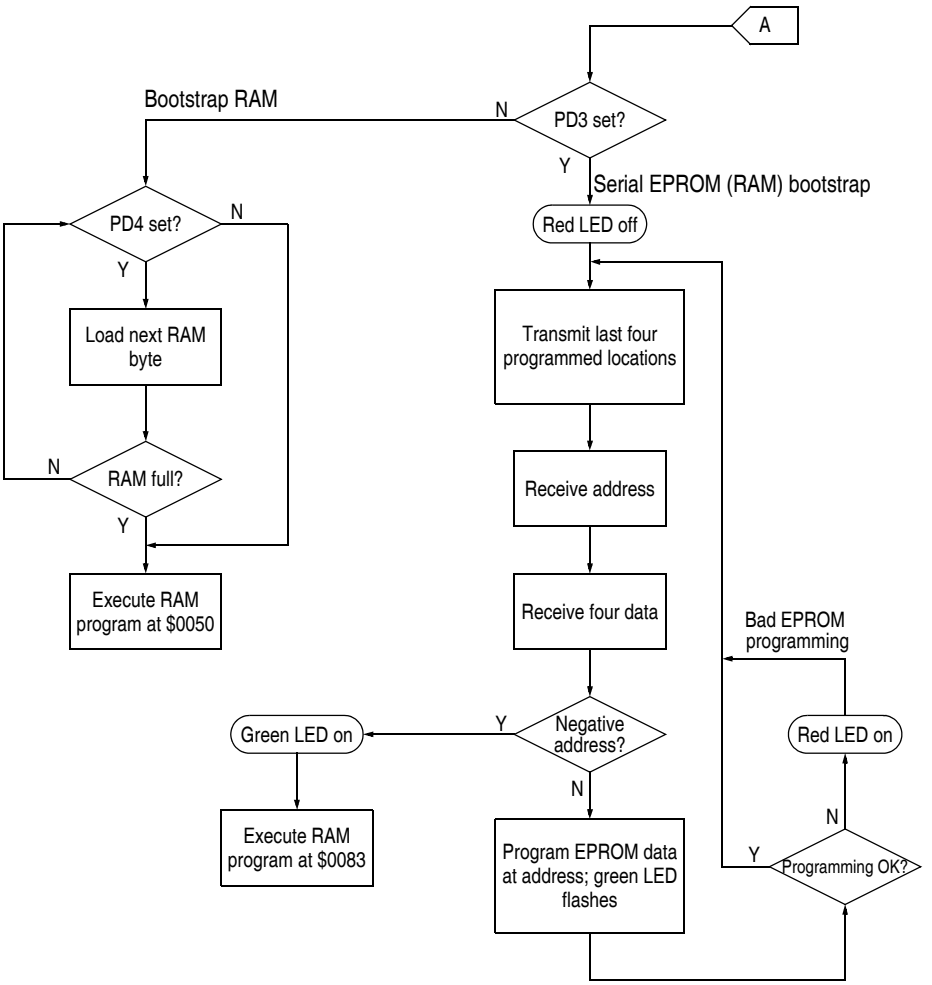
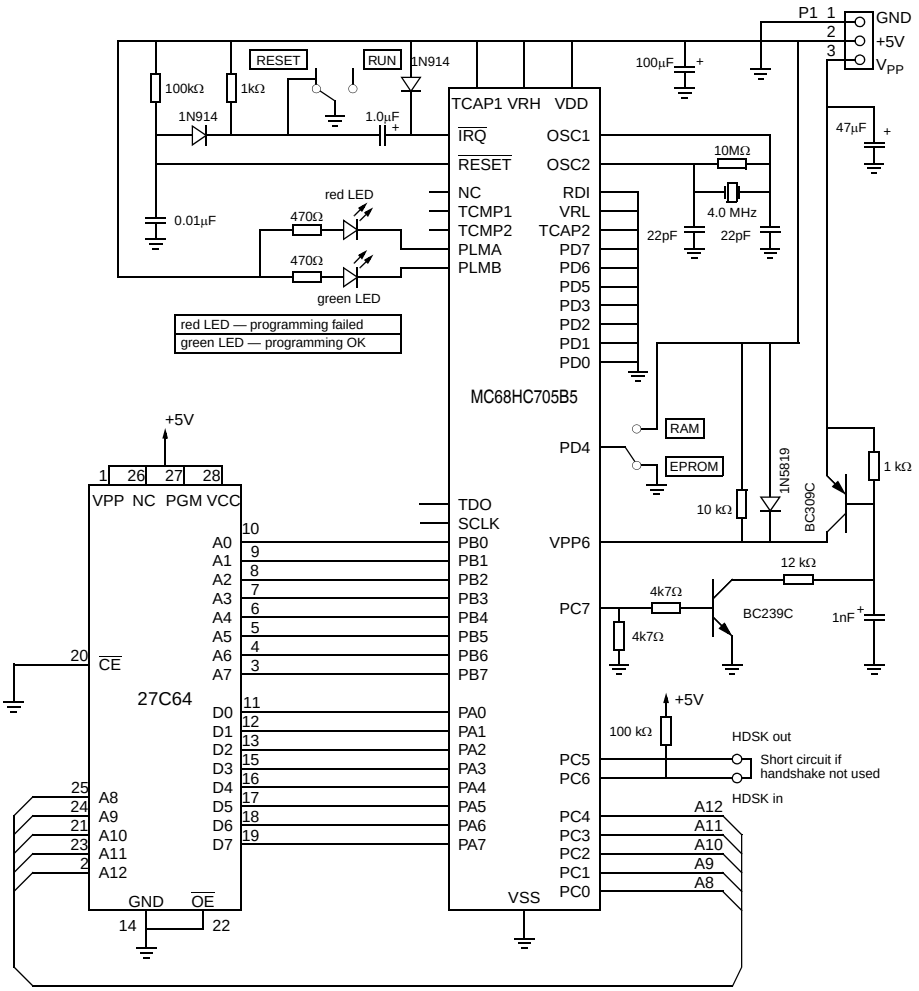


Figure C-4 Modes of operation flow chart (2 of 2)



Note: This circuit is recommended for programming only at 25°C and not for use in the end application, or at temperatures other than 25°C. If used in the end application, VPP6 should be tied to VDD to avoid damaging the device.

Figure C-6 EPROM(RAM) parallel bootstrap schematic diagram

4) The exchange of data continues until the MC68HC705B16 has sent the four data bytes and the host has sent the 2 address data bytes and 4 data bytes.
5) If the data is different from $00 for EPROM or $FF for EEPROM, it is programmed at the address provided, while the next address and bytes are received and the previous data is echoed.
6) Loop to 1.

After reset, the MC68HC705B16 serial bootstrap routine will first echo two blocks of four bytes at $00, as no data is programmed yet.

If the data received is $00 for EPROM locations or $FF for EEPROM locations, no programming in the EPROM and EEPROM1 takes place, and the contents of the accessed location are returned as a prompt. The entire EPROM/EEPROM memory can be read in this fashion (serial dump).

Warning: When using this function with a programmed device, the device must be placed into RAM/EPROM/EEPROM serial bootstrap mode without EPROM erase check (PD4 = 1).

Serial RAM loading and execute can be accomplished in this mode. A RAM byte will be written if the address sent by the host in the serial protocol points to the RAM.

RAM bytes $008B–$00E3 and $0250–$02ED are available for user test programs. A 10-byte stack resides at the top of RAM1, allowing, for example, one interrupt and two sub-routine levels. The RAM addresses between $0050 and $008A are used by the loader and are therefore not available to the user during serial loading/executing.

If the SEC bit is at ‘1’, program execution is triggered by sending a negative (bit 7 set) high address; execution starts at address XADR ($008B).

In the RAM bootloader mode, all interrupt vectors are mapped to pseudo-vectors in RAM (see Table E-5). This allows programmers to use their own service-routine addresses. Each pseudo-vector is allowed three bytes of space rather than the two bytes for normal vectors, because an explicit jump (JMP) opcode is needed to cause the desired jump to the user’s service routine address.

Table E-5 Bootstrap vector targets in RAM

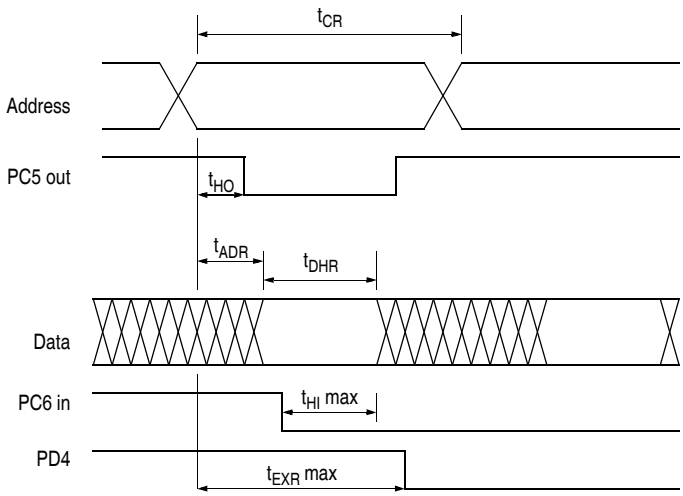
Vector targets in RAM	
SCI interrupt	$02EE
Timer overflow	$02F1
Timer output compare	$02F4
Timer input capture	$02F7
$\overline{\text{IRQ}}$	$02FA
SWI	$02FD

E.4.4 RAM parallel bootstrap

The program first checks the state of the security bit. If the SEC bit is active, i.e. ‘0’, the program will not enter the RAM bootstrap mode and the red LED will flash. Otherwise the RAM bootstrap program will start loading the RAM with external data (e.g. from a 2564 or 2764 EPROM). Before loading a new byte the state of the PD4/AN4 pin is checked. If this pin goes to level ‘0’, or if the RAM is full, then control is given to the loaded program at address $0050. See Figure E-3 and Figure E-4.

If the data is supplied by a parallel interface, handshaking will be provided by PC5 and PC6 according to Figure E-9. If the data comes from an external EPROM, the handshake can be disabled by connecting together PC5 and PC6.

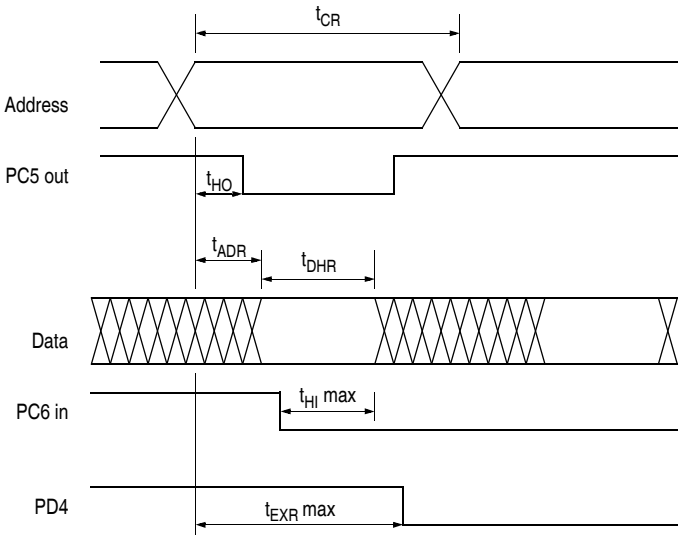
Figure E-10 provides a schematic diagram of a circuit that can be used to load the RAM with short test programs. Up to 8 programs can be loaded in turn from the EPROM. Selection is accomplished by means of the switches connected to the EPROM higher address lines (A8 through A10). If the user program sets PC0 to level ‘1’, this will disable the external EPROM, thus rendering both port A output and port B input available. The EPROM parallel bootstrap loader schematic can also be used (Figure E-7), provided VPP is at V_{DD} level. The high order address lines will be at zero. The LEDs will stay off.



t_{ADR} max (address to data delay; PC6=PC5)	16 machine cycles
t_{DHR} min (data hold time)	4 machine cycles
t_{CR} (load cycle time; PC6=PC5)	49 machine cycles
t_{HO} (PC5 handshake out delay)	5 machine cycles
t_{HI} max (PC6 handshake in, data hold time)	10 machine cycles
t_{EXR} max (max delay for transition to be recognised during this cycle; PC6=PC5	30 machine cycles

1 machine cycle = $1/(2f_0(Xtal))$

Figure E-9 Parallel RAM loader timing diagram



t_{ADR} max (address to data delay; PC6=PC5)	16 machine cycles
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t_{CR} (load cycle time; PC6=PC5)	49 machine cycles
t_{HO} (PC5 handshake out delay)	5 machine cycles
t_{HI} max (PC6 handshake in, data hold time)	10 machine cycles
t_{EXR} max (max delay for transition to be recognised during this cycle; PC6=PC5	30 machine cycles

1 machine cycle = $1/(2f_0(Xtal))$

Figure F-9 Parallel RAM loader timing diagram

H

MC68HC705B32

Maskset errata

This errata section outlines the differences between two previously available masksets (D59J and D40J) and all other masksets. Unless otherwise stated, the main body of Appendix G refers to all these other masksets with any differences being noted in this errata section.

- For the D59J and D40J masksets, the MCU only requires that a logic zero is applied to the $\overline{\text{RESET}}$ input for 1.5 t_{CYC}.
- For D59J, 16 cycle POR delay option (t_{PORL}) is not available
- For the D59J maskset, oscillator divide ratio DIV10 is forced in Bootstrap mode. On all other revisions DIV2 is forced.

For the D59J:

The STOP Idd is greater than the expected value of 120μA at 5 volts Vdd at a temperature of 20°C with the CAN module enabled and in SLEEP mode. Typically the STOP Idd is in the region of 2.0 milliamps at 20°C.

The fault lies with the design of the EPROM array. When the STOP instruction is executed, the next opcode in memory is present on the data bus. A fault in the EPROM write data latch circuitry causes a latch to be driven to logic 0 on both sides when the data bus for that bit is logic 1. This results in increasing STOP Idd of 450μA per data bus bit set to a logic 1. If all data bus bits are set to logic 1 (i.e. next opcode is $FF, STX 0,X) the STOP Idd shall be in the region of 3.6mA.

The minimum STOP Idd is achieved by ensuring the opcode immediately following the STOP instruction is data $00. This corresponds to BRSET 0,ADDRESS,LABEL. If the label points to the next sequential instruction in memory then this has the effect of a 5 cycle NOP but note that the carry bit in the condition code register may be altered by the BRSET instruction.

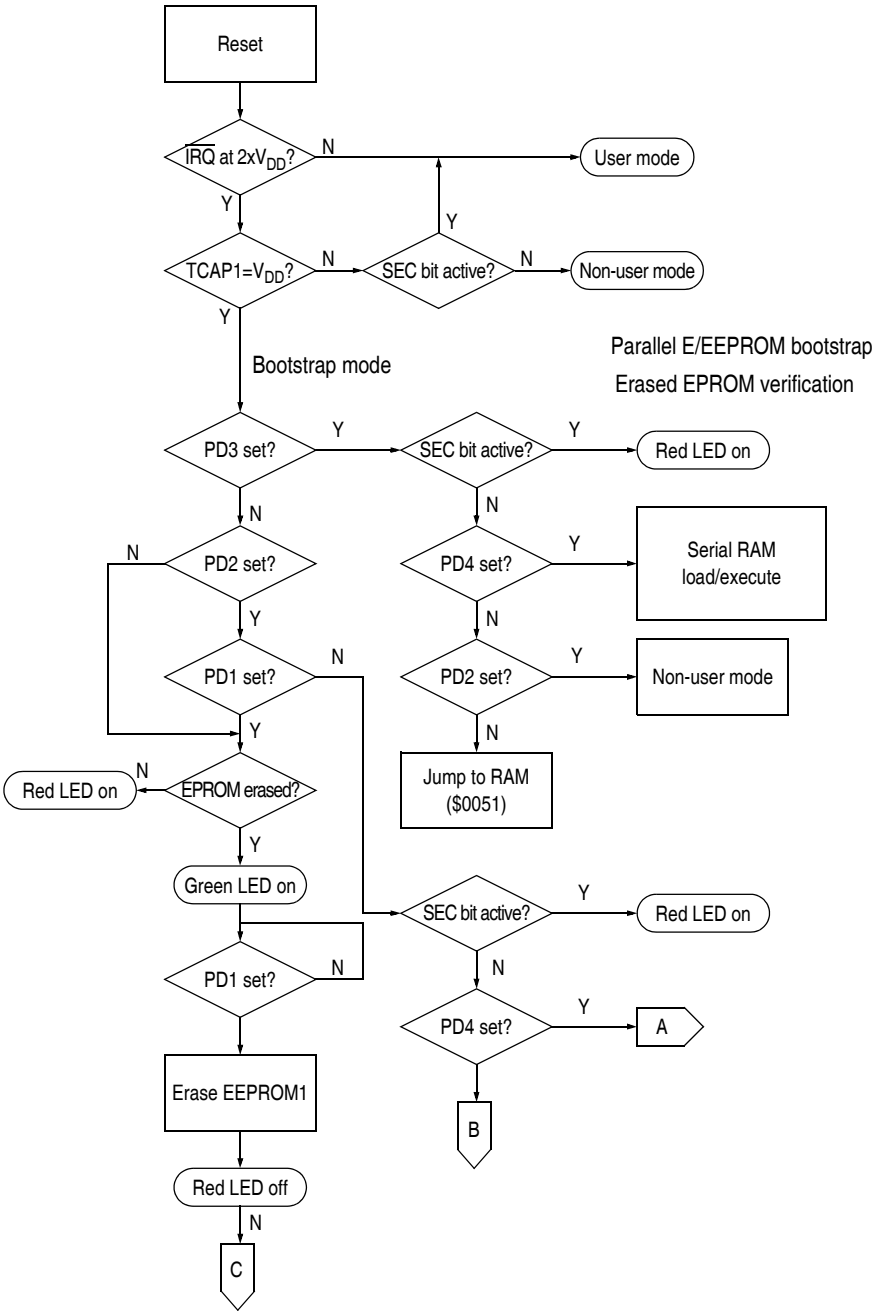

Figure H-3 Modes of operation flow chart (1 of 2)

H.7 DC electrical characteristics

Table H-7 DC electrical characteristics for 5V operation

(V_{DD} = 5 Vdc ± 10%, V_{SS} = 0 Vdc, –40 to +85°C)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{LOAD} = – 10 µA I_{LOAD} = +10 µA	 V_{OH} V_{OL}	 V_{DD} – 0.1 —	 — —	 — 0.1	V
Output high voltage (I_{LOAD} = 0.8mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2 Output high voltage (I_{LOAD} = 1.6mA) TDO, SCLK, PLMA, PLMB Output high voltage (I_{LOAD} = -300µA) OSC2	 V_{OH} V_{OH} V_{OH}	 V_{DD} – 0.8 V_{DD} – 0.8 V_{DD} – 0.8	 V_{DD} – 0.4 V_{DD} – 0.4 V_{DD} – 0.3	 — — —	V
Output low voltage (I_{LOAD} = 1.6mA) PA0–7, PB0–7, PC0–7, TCMP1, TCMP2, TDO, SCLK, PLMA, PLMB Output low voltage (I_{LOAD} = 1.6mA) $\overline{RESET}$ Output low voltage (I_{LOAD} = -100µA) OSC2	 V_{OL} V_{OL} V_{OL}	 — — —	 0.1 0.4 TBD	 0.4 1 —	V
Input high voltage PA0–7, PB0–7, PC0–7, PD0–7, OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IH}	0.7V_{DD}	—	V_{DD}	V
Input low voltage PA0–7, PB0–7, PC0–7, PD0–7,OSC1, $\overline{IRQ}$, $\overline{RESET}$, TCAP1, TCAP2, RDI	V_{IL}	V_{SS}	—	0.2V_{DD}	V
Supply current[3] (For Guidance Only) RUN (SM = 0) (See Figure 11-1) RUN (SM = 1) (See Figure 11-2) WAIT (SM = 0) (See Figure 11-3) WAIT (SM = 1) (See Figure 11-4) STOP 0 to 70 (standard) – 40 to 85 (extended)	 I_{DD} I_{DD} I_{DD} I_{DD} I_{DD} I_{DD}	 — — — — — —	 6 1.5 2 1 10 10	 TBD TBD TBD TBD TBD TBD	 mA mA mA mA µA µA
High-Z leakage current PA0–7, PB0–7, PC0–7, TDO, $\overline{RESET}$, SCLK	I_{IL}	—	±0.2	±1	µA
Input current Port B and port C pull-down (V_{IN}=V_{IH})	I_{RPD}		80		µA
Input current (0 to 70) $\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	±0.2	±1	µA
Input current (– 40 to 85) $\overline{IRQ}$, OSC1, TCAP1, TCAP2, RDI, PD0/AN0-PD7/AN7 (channel not selected)	I_{IN}	—	—	±5	µA
Capacitance Ports (as input or output), $\overline{RESET}$, TDO, SCLK $\overline{IRQ}$, TCAP1, TCAP2, OSC1, RDI PD0/AN0–PD7/AN7 (A/D off) PD0/AN0–PD7/AN7 (A/D on)	 C_{OUT} C_{OUT} C_{IN} C_{IN}	 — — — —	 — — 12 22	 12 8 — —	 pF pF pF pF

(1) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs (see Section 2).

(2) Typical values are at mid point of voltage range and at 25°C only.

H.9 Control timing

Table H-11 Control timing for 5V operation

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40 to +85°C)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation Crystal option External clock option	 f_{OSC} f_{OSC}	 — dc	 4.2 4.2	 MHz MHz
Internal operating frequency (f_{OSC}/2) Using crystal Using external clock	 f_{OP} f_{OP}	 — dc	 2.1 2.1	 MHz MHz
Cycle time (see Figure 9-1)	t_{CYC}	476	—	ns
Crystal oscillator start-up time (see Figure 9-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
RC oscillator stabilization time	t_{ADRC}		5	µs
A/D converter stabilization time	t_{ADON}		500	µs
External RESET input pulse width	t_{RL}	3.0	—	t_{CYC}
Power-on RESET output pulse width 4064 cycle 16 cycle	 t_{PORL} t_{PORL}	 4064 16	 — —	 t_{CYC} t_{CYC}
Watchdog RESET output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EEPROM byte erase time 0 to 70 (standard) – 40 to 85 (extended)	 t_{ERA} t_{ERA}	 10 10	 — —	 ms ms
EEPROM byte program time(1) 0 to 70 (standard) – 40 to 85 (extended)	 t_{PROG} t_{PROG}	 10 10	 — —	 ms ms
Timer (see Figure H-10) Resolution(2) Input capture pulse width Input capture pulse period	 t_{RESL} t_{TH}, t_{TL} t_{TLTL}	 4 125 —(3)	 — — —	 t_{CYC} ns t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	125	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width(5)	t_{OH}, t_{OL}	90	—	ns
Write/Erase endurance(6)(7)	—	10000		cycles
Data retention(6)(7)	—	10		years

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.

(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{CYC}), this is the limiting factor in determining the timer resolution.

(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.

(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.

(5) t_{OH} and t_{OL} should not total less than 238ns.

(6) At a temperature of 85°C

(7) Refer to Reliability Monitor Report (current quarterly issue) for current failure rate information.

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