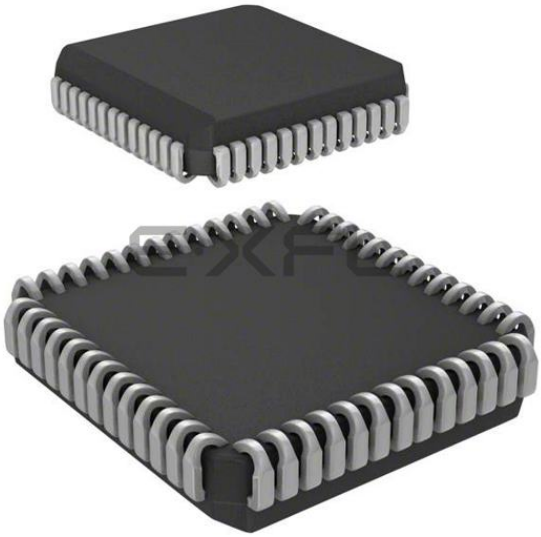

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	256 x 8
RAM Size	528 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LCC (J-Lead)
Supplier Device Package	52-PLCC (19.1x19.1)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/xc705b32cfne

D
MC68HC05B16

E
MC68HC705B16

F
MC68HC705B16N

LIST OF FIGURES

3.4 Self-check ROM

There are two areas of self-check ROM (ROMI and ROMII) located from $0200 to $02BF (192 bytes) and $1F00 to $1FEF (240 bytes) respectively.

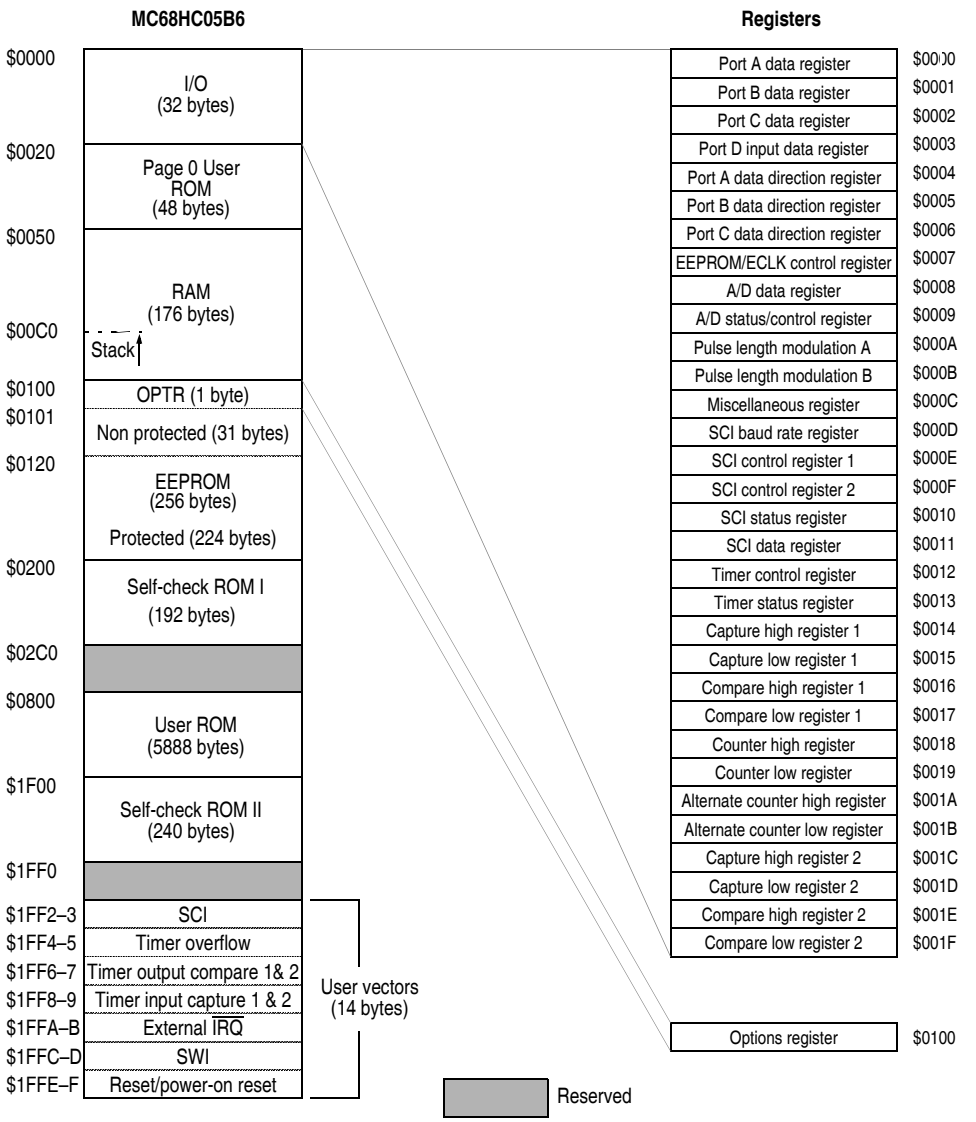

Figure 3-1 Memory map of the MC68HC05B6

The purpose of this procedure is to prevent the OCF1 bit from being set between the time it is read and the write to the corresponding output compare register.

All bits of the output compare register are readable and writable and are not altered by the timer hardware or reset. If the compare function is not needed, the two bytes of the output compare register can be used as storage locations.

5.4.3 Software force compare

A software force compare is required in many applications. To achieve this, bit 3 (FOLV1 for OCR1) and bit 4 (FOLV2 for OCR2) in the timer control register are used. These bits always read as ‘zero’, but a write to ‘one’ causes the respective OLVL1 or OLVL2 values to be copied to the respective output level (TCMP1 and TCMP2 pins).

Internal logic is arranged such that in a single instruction, one can change OLVL1 and/or OLVL2, at the same time causing a forced output compare with the new values of OLVL1 and OLVL2. In conjunction with normal compare, this function allows a wide range of applications including fixed frequency generation.

Note: A software force compare will affect the corresponding output pin TCMP1 and/or TCMP2, but will not affect the compare flag, thus it will not generate an interrupt.

5.5 Pulse Length Modulation (PLM)

The programmable timer works in conjunction with the PLM system to execute two 8-bit D/A PLM conversions, with a choice of two repetition rates (see Section 7).

5.5.1 Pulse length modulation registers A and B (PLMA/PLMB)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Pulse length modulation A (PLMA)	$000A									0000 0000

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Pulse length modulation B (PLMB)	$000B									0000 0000

CPOL – Clock polarity

This bit allows the user to select the polarity of the clocks to be sent to the SCLK pin. It works in conjunction with the CPHA bit to produce the desired clock-data relation (see Figure 6-9 and Figure 6-10).

1 (set) – Steady high value at SCLK pin outside transmission window.

0 (clear) – Steady low value at SCLK pin outside transmission window.

This bit should not be manipulated while the transmitter is enabled.

CPHA – Clock phase

This bit allows the user to select the phase of the clocks to be sent to the SCLK pin. This bit works in conjunction with the CPOL bit to produce the desired clock-data relation (see Figure 6-9 and Figure 6-10).

1 (set) – SCLK clock line activated at beginning of data bit.

0 (clear) – SCLK clock line activated in middle of data bit.

This bit should not be manipulated while the transmitter is enabled.

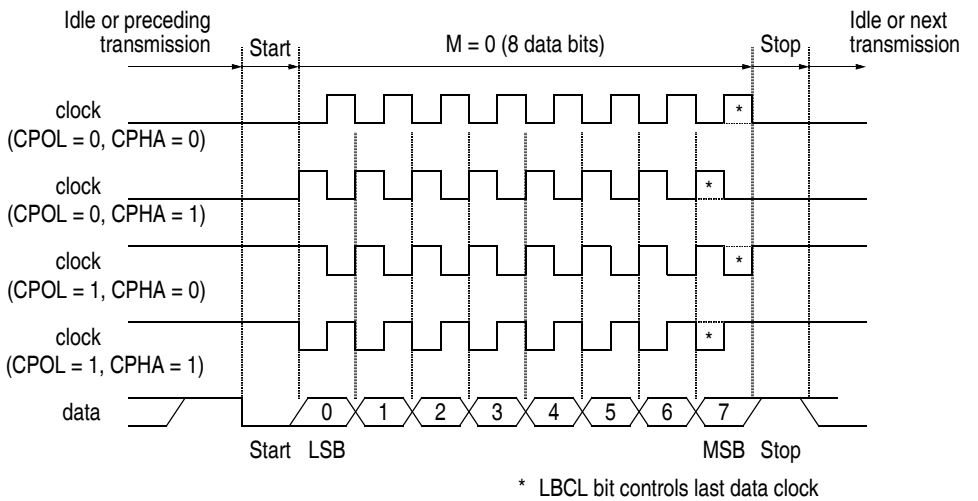

Figure 6-9 SCI data clock timing diagram (M=0)

SCR2, SCR1, SCR0 — SCI rate select bits (receiver)

These three read/write bits select the baud rates for the receiver. The prescaler output described above is divided by the factors shown in Table 6-5.

Table 6-5 Second prescaler stage (receiver)

SCR2	SCR1	SCR0	Receiver division ratio (NR)
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

The following equations are used to calculate the receiver and transmitter baud rates:

$$\text{baudTx} = \frac{f_{op}}{16 \bullet NP \bullet NT}$$

$$\text{baudRx} = \frac{f_{op}}{16 \bullet NP \bullet NR}$$

where:

NP = prescaler divide ratio

NT = transmitter baud rate divide ratio

NR = receiver baud rate divide ratio

baudTx = transmitter baud rate

baudRx = receiver baud rate

f_{OSC} = oscillator frequency

6.12 Baud rate selection

The flexibility of the baud rate generator allows many different baud rates to be selected. A particular baud rate may be generated in several ways by manipulating the various prescaler and division ratio bits. Table 6-6 shows the baud rates that can be achieved, for five typical crystal frequencies. These are effectively the highest baud rates which can be achieved using a given crystal.

Table 10-1 MUL instruction

Operation	**X:A ← X*A**			
Description	Multiplies the eight bits in the index register by the eight bits in the accumulator and places the 16-bit result in the concatenated accumulator and index register.			
Condition codes	H : Cleared I : Not affected N : Not affected Z : Not affected C : Cleared			
Source	MUL			
Form	Addressing mode	Cycles	Bytes	Opcode
	Inherent	11	1	$42

Table 10-2 Register/memory instructions

		Addressing modes																	
		Immediate			Direct			Extended			Indexed (no offset)			Indexed (8-bit offset)			Indexed (16-bit offset)		
Function	**Mnemonic**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**
Load A from memory	LDA	A6	2	2	B6	2	3	C6	3	4	F6	1	3	E6	2	4	D6	3	5
Load X from memory	LDX	AE	2	2	BE	2	3	CE	3	4	FE	1	3	EE	2	4	DE	3	5
Store A in memory	STA				B7	2	4	C7	3	5	F7	1	4	E7	2	5	D7	3	6
Store X in memory	STX				BF	2	4	CF	3	5	FF	1	4	EF	2	5	DF	3	6
Add memory to A	ADD	AB	2	2	BB	2	3	CB	3	4	FB	1	3	EB	2	4	DB	3	5
Add memory and carry to A	ADC	A9	2	2	B9	2	3	C9	3	4	F9	1	3	E9	2	4	D9	3	5
Subtract memory	SUB	A0	2	2	B0	2	3	C0	3	4	F0	1	3	E0	2	4	D0	3	5
Subtract memory from A with borrow	SBC	A2	2	2	B2	2	3	C2	3	4	F2	1	3	E2	2	4	D2	3	5
AND memory with A	AND	A4	2	2	B4	2	3	C4	3	4	F4	1	3	E4	2	4	D4	3	5
OR memory with A	ORA	AA	2	2	BA	2	3	CA	3	4	FA	1	3	EA	2	4	DA	3	5
Exclusive OR memory with A	EOR	A8	2	2	B8	2	3	C8	3	4	F8	1	3	E8	2	4	D8	3	5
Arithmetic compare A with memory	CMP	A1	2	2	B1	2	3	C1	3	4	F1	1	3	E1	2	4	D1	3	5
Arithmetic compare X with memory	CPX	A3	2	2	B3	2	3	C3	3	4	F3	1	3	E3	2	4	D3	3	5
Bit test memory with A (logical compare)	BIT	A5	2	2	B5	2	3	C5	3	4	F5	1	3	E5	2	4	D5	3	5
Jump unconditional	JMP				BC	2	2	CC	3	3	FC	1	2	EC	2	3	DC	3	4
Jump to subroutine	JSR				BD	2	5	CD	3	6	FD	1	5	ED	2	6	DD	3	7

Table 10-8 Instruction set (2 of 2)

Mnemonic	Addressing modes										Condition codes				
	INH	IMM	DIR	EXT	REL	IX	IX1	IX2	BSC	BTB	H	I	N	Z	C
COM											•	•	Þ	Þ	1
CPX											•	•	Þ	Þ	Þ
DEC											•	•	Þ	Þ	•
EOR											•	•	Þ	Þ	•
INC											•	•	Þ	Þ	•
JMP											•	•	•	•	•
JSR											•	•	•	•	•
LDA											•	•	Þ	Þ	•
LDX											•	•	Þ	Þ	•
LSL											•	•	Þ	Þ	Þ
LSR											•	•	0	Þ	Þ
MUL											0	•	•	•	0
NEG											•	•	Þ	Þ	Þ
NOP											•	•	•	•	•
ORA											•	•	Þ	Þ	•
ROL											•	•	Þ	Þ	Þ
ROR											•	•	Þ	Þ	Þ
RSP											•	•	•	•	•
RTI											?	?	?	?	?
RTS											•	•	•	•	•
SBC											•	•	Þ	Þ	Þ
SEC											•	•	•	•	1
SEI											•	1	•	•	•
STA											•	•	Þ	Þ	•
STOP											•	0	•	•	•
STX											•	•	Þ	Þ	•
SUB											•	•	Þ	Þ	Þ
SWI											•	1	•	•	•
TAX											•	•	•	•	•
TST											•	•	Þ	Þ	•
TXA											•	•	•	•	•
WAIT											•	0	•	•	•

Address mode abbreviations

BSC	Bit set/clear	IMM	Immediate
BTB	Bit test & branch	IX	Indexed (no offset)
DIR	Direct	IX1	Indexed, 1 byte offset
EXT	Extended	IX2	Indexed, 2 byte offset
INH	Inherent	REL	Relative

Not implemented

Condition code symbols

H	Half carry (from bit 3)	Þ	Tested and set if true, cleared otherwise
I	Interrupt mask	•	Not affected
N	Negate (sign bit)	?	Load CCR from stack
Z	Zero	0	Cleared
C	Carry/borrow	1	Set

Table A-2 Register outline

Register name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data (PORTA)	$0000									Undefined
Port B data (PORTB)	$0001									Undefined
Port C data (PORTC)	$0002						PC2/ ECLK			Undefined
Port D data (PORTD)	$0003	PD7/ AN7	PD6/ AN6	PD5/ AN5	PD4/ AN4	PD3/ AN3	PD2/ AN2	PD1/ AN1	PD0/ AN0	Undefined
Port A data direction (DDRA)	$0004									0000 0000
Port B data direction (DDRB)	$0005									0000 0000
Port C data direction (DDRC)	$0006									0000 0000
ECLK control	$0007	0	0	0	0	ECLK	0	0	0	0000 0000
A/D data (ADDATA)	$0008									0000 0000
A/D status/control (ADSTAT)	$0009	COCO	ADRC	ADON	0	CH3	CH2	CH1	CH0	0000 0000
Pulse length modulation A (PLMA)	$000A									0000 0000
Pulse length modulation B (PLMB)	$000B									0000 0000
Miscellaneous	$000C	POR(1)	INTP	INTN	INTE	SFA	SFB	SM	WDOG (2)	?001 000?
SCI baud rate (BAUD)	$000D	SPC1	SPC0	SCT1	SCT0	SCT0	SCR2	SCR1	SCR0	00uu uuuu
SCI control 1 (SCCR1)	$000E	R8	T8		M	WAKE	CPOL	CPHA	LBCL	uuuu uuuu
SCI control 2 (SCCR2)	$000F	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	0000 0000
SCI status (SCSR)	$0010	TDRE	TC	RDRF	IDLE	OR	NF	FE		1100 000u
SCI data (SCDR)	$0011									0000 0000
Timer control (TCR)	$0012	ICIE	OCIE	TOIE	FOLV2	FOLV1	OLV2	IEDG1	OLVL1	0000 00u0
Timer status (TSR)	$0013	ICF1	OCF1	TOF	ICF2	OCF2				uuuu uuuu
Input capture high 1	$0014									Undefined
Input capture low 1	$0015									Undefined
Output compare high 1	$0016									Undefined
Output compare low 1	$0017									Undefined
Timer counter high	$0018									1111 1111
Timer counter low	$0019									1111 1100
Alternate counter high	$001A									1111 1111
Alternate counter low	$001B									1111 1100
Input capture high 2	$001C									Undefined
Input capture low 2	$001D									Undefined
Output compare high 2	$001E									Undefined
Output compare low 2	$001F									Undefined

(1) This bit is set each time there is a power-on reset.

(2) The state of the WDOG bit after reset is dependent upon the mask option selected; 1=watchdog enabled, 0=watchdog disabled.

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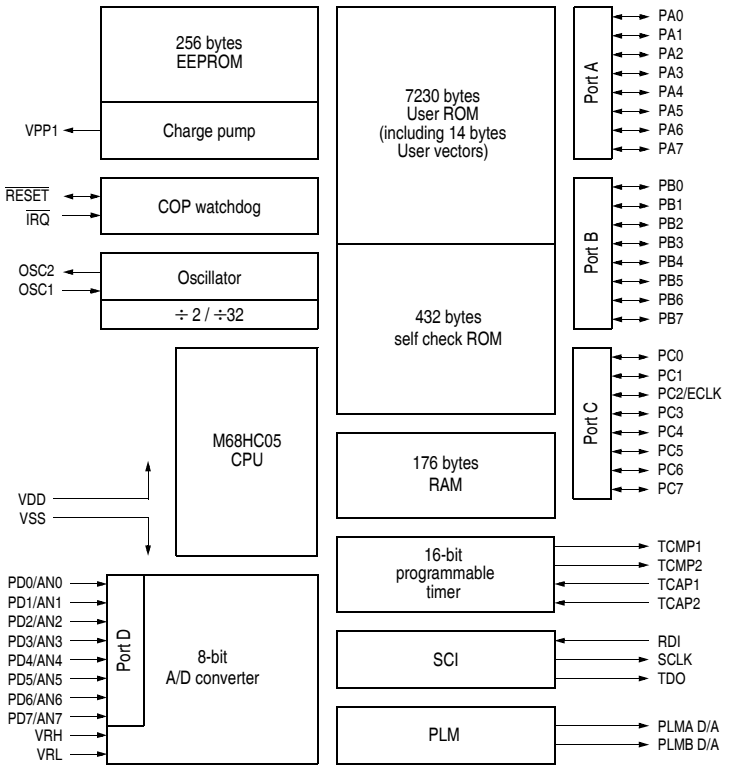


Figure B-1 MC68HC05B8 block diagram

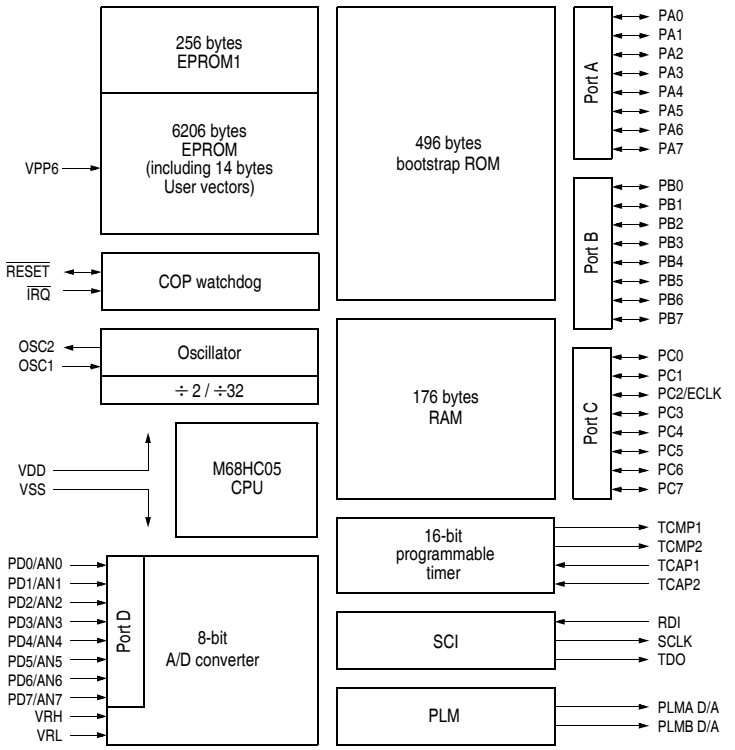


Figure C-1 MC68HC705B5 block diagram

C.4 Options register (OPTR)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Options (OPTR)(1)	$1EFE		EPP	0	RTIM	RWAT	WWAT	PBPD	PCPD	Not affected

(1) This register is implemented in EPROM, therefore reset has no effect on the state of the individual bits.

Note: This register can only be written to while the device is in bootloader mode.

Bit 7 — Factory use only

Warning: This bit is strictly for factory use only and will always read zero to avoid accidental damage to the device. Any attempt to write to this bit could result in physical damage.

EPP — EPROM protect

This bit protects the contents of the main EPROM against accidental modification; it has no effect on reading or executing code in the EPROM.

1 (set) – EPROM contents are protected.

0 (clear) – EPROM contents are not protected.

RTIM — Reset time

This bit can modify t_{PORL}, i.e. the time that the $\overline{\text{RESET}}$ pin is kept low following a power-on reset. This feature is handled in the ROM part via a mask option.

1 (set) – t_{PORL} = 16 cycles.

0 (clear) – t_{PORL} = 4064 cycles.

RWAT — Watchdog after reset

This bit can modify the status of the watchdog counter after reset.

1 (set) – The watchdog will be active immediately following power-on or external reset (except in bootstrap mode).

0 (clear) – The watchdog system will be disabled after power-on or external reset.

WWAT — Watchdog during WAIT mode

This bit can modify the status of the watchdog counter during WAIT mode.

Table E-12 Control timing for 3.3V operation

(V_{DD} = 3.3Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation				
Crystal option	f_{OSC}	—	2.0	MHz
External clock option	f_{OSC}	dc	2.0	MHz
Internal operating frequency (f_{OSC}/2)				
Using crystal	f_{OP}	—	1.0	MHz
Using external clock	f_{OP}	dc	1.0	MHz
Cycle time (see Figure 9-1)	t_{CYC}	1000	—	ns
Crystal oscillator start-up time (see Figure 9-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
RC oscillator stabilization time	t_{ADRC}		5	µs
A/D converter stabilization time	t_{ADON}		500	µs
External $\overline{\text{RESET}}$ input pulse width	t_{RL}	1.5	—	t_{CYC}
Power-on $\overline{\text{RESET}}$ output pulse width				
4064 cycle	t_{PORL}	4064	—	t_{CYC}
16 cycle	t_{PORL}	16	—	t_{CYC}
Watchdog $\overline{\text{RESET}}$ output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EEPROM byte erase time				
0 to 70 (standard)	t_{ERA}	30	—	ms
– 40 to 85 (extended)	t_{ERA}	30	—	ms
– 40 to 105 (industrial)	t_{ERA}	30	—	ms
– 40 to 125 (automotive)	t_{ERA}	30	—	ms
EEPROM byte program time(1)				
0 to 70 (standard)	t_{PROG}	30	—	ms
– 40 to 85 (extended)	t_{PROG}	30	—	ms
– 40 to 105 (industrial)	t_{PROG}	30	—	ms
– 40 to 125 (automotive)	t_{PROG}	30	—	ms
Timer (see Figure E-11)				
Resolution(2)	t_{RESL}	4	—	t_{CYC}
Input capture pulse width	t_{TH}, t_{TL}	250	—	ns
Input capture pulse period	t_{TLTL}	—(3)	—	t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	250	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width(5)	t_{OH}, t_{OL}	200	—	ns
Write/Erase endurance(6)(7)	—	10000		cycles
Data retention(6)(7)	—	10		years

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.
(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{CYC}), this is the limiting factor in determining the timer resolution.
(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.
(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.
(5) t_{OH} and t_{OL} should not total less than 500ns.
(6) At a temperature of 85°C
(7) Refer to Reliability Monitor Report (current quarterly issue) for current failure rate information.

F
MC68HC705B16N

The MC68HC705B16N is a new device identical to the MC68HC705B16 in its memory map and functionality, except for the following:

- Bootloader
- Reset pulse width
- Reset twice issue
- Electrical characteristics

On the MC68HC705B16 there was a requirement to reset the device a second time after power-on. On the MC68HC705B16N this reset twice action is now not required. The interrupt service routine for the vector at address $3FF0–$3FF1 is no longer required, as the vector will never be fetched. However, the interrupt service routine and vector contents required for the MC68HC705B16 (see Section E, page E–1) can also be kept on the MC68HC705B16N with no detrimental effect, although they will never be used.

The MC68HC705B16N is a device similar to the MC68HC05B6, but with increased RAM and 15 kbytes of EPROM instead of 6 kbytes of ROM. In addition, the self-check routines available in the MC68HC05B6 are replaced by bootstrap firmware. The MC68HC705B16N is an OTPROM (one-time programmable ROM) version of the MC68HC05B16, meaning that once the application program has been loaded in the EPROM it can never be erased. The entire MC68HC05B6 data sheet applies to the MC68HC705B16N, with the exceptions outlined in this appendix.

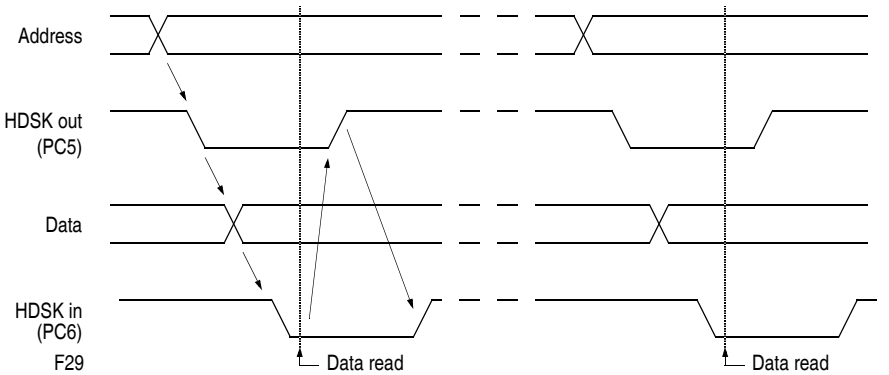
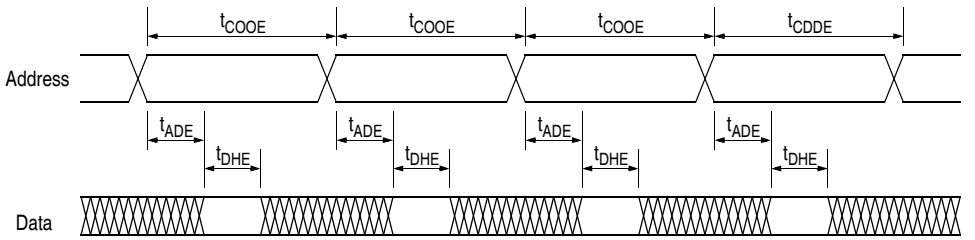


Figure F-5 Timing diagram with handshake



t_{ADE} max (address to data delay)	5 machine cycles
t_{DHA} min (data hold time)	14 machine cycles
t_{COOE} (load cycle time)	117 machine cycles < t_{COOE} < 150 machine cycles
t_{CDDE} (programming cycle time)	t_{COOE} + t_{PROG} (10 ms nominal for EPROM; 10ms for EEPROM1))

1 machine cycle = $1/(2f_0(Xtal))$

Figure F-6 Parallel EPROM loader timing diagram

Table F-12 Control timing for 3.3V operation

(V_{DD} = 3.3Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation				
Crystal option	f_{OSC}	—	2.0	MHz
External clock option	f_{OSC}	dc	2.0	MHz
Internal operating frequency ($f_{OSC}/2$)				
Using crystal	f_{OP}	—	1.0	MHz
Using external clock	f_{OP}	dc	1.0	MHz
Cycle time (see Figure 9-1)	t_{CYC}	1000	—	ns
Crystal oscillator start-up time (see Figure 9-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
RC oscillator stabilization time	t_{ADRC}		5	µs
A/D converter stabilization time	t_{ADON}		500	µs
External $\overline{\text{RESET}}$ input pulse width	t_{RL}	3.0	—	t_{CYC}
Power-on $\overline{\text{RESET}}$ output pulse width				
4064 cycle	t_{PORL}	4064	—	t_{CYC}
16 cycle	t_{PORL}	16	—	t_{CYC}
Watchdog $\overline{\text{RESET}}$ output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EEPROM byte erase time				
0 to 70 (standard)	t_{ERA}	30	—	ms
– 40 to 85 (extended)	t_{ERA}	30	—	ms
– 40 to 105 (industrial)	t_{ERA}	30	—	ms
– 40 to 125 (automotive)	t_{ERA}	30	—	ms
EEPROM byte program time(1)				
0 to 70 (standard)	t_{PROG}	30	—	ms
– 40 to 85 (extended)	t_{PROG}	30	—	ms
– 40 to 105 (industrial)	t_{PROG}	30	—	ms
– 40 to 125 (automotive)	t_{PROG}	30	—	ms
Timer (see Figure F-10)				
Resolution(2)	t_{RESL}	4	—	t_{CYC}
Input capture pulse width	t_{TH}, t_{TL}	250	—	ns
Input capture pulse period	t_{TLTL}	—(3)	—	t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	250	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width(5)	t_{OH}, t_{OL}	200	—	ns
Write/Erase endurance(6)(7)	—	10000		cycles
Data retention(6)(7)	—	10		years

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.
(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{CYC}), this is the limiting factor in determining the timer resolution.
(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.
(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.
(5) t_{OH} and t_{OL} should not total less than 500ns.
(6) At a temperature of 85°C
(7) Refer to Reliability Monitor Report (current quarterly issue) for current failure rate information.

H.5.3 Serial RAM loader

This mode is similar to the RAM load/execute program for the MC68HC05B6 described in Section 2.2, with the additional features listed below. Table H-4 shows the entry conditions required for this mode.

If the first byte is less than $B0, the bootloader behaves exactly as the MC68HC05B6, i.e. count byte followed by data stored in $0050 to $00FF. If the count byte is larger than RAM I (176 bytes) then the code continues to fill RAM II then RAM III. In this case the count byte is ignored and the program execution begins at $0051 once the total RAM area is filled or if no data is received for 5 milliseconds.

The user must take care when using branches or jumps as his code will be relocated in RAM I, II and III. If the user intends to use the stack in his program, he should send NOP's to fill the desired stack area.

In the RAM bootloader mode, all interrupt vectors are mapped to pseudo-vectors in RAM (see Table H-5). This allows programmers to use their own service-routine addresses. Each pseudo-vector is allowed three bytes of space rather than the two bytes for normal vectors, because an explicit jump (JMP) opcode is needed to cause the desired jump to the users service-routine address.

Table H-5 Bootstrap vector targets in RAM

Vector targets in RAM	
SCI interrupt	$0063
Timer overflow	$0060
Timer output compare	$005D
Timer input capture	$005A
$\overline{\text{IRQ}}$	$0057
SWI	$0054

H.5.3.1 Jump to start of RAM ($0051)

The Jump to start of RAM program will be executed when bring the device out of reset with PD2 and PD3 at '1' and PD4 at '0'.

I.3 Control timing for 5V operation

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40 to +85°C)

Characteristic	Symbol	Min	Max	Unit
Frequency of operation Crystal option External clock option	 f_{OSC} f_{OSC}	 — dc	 8.0 8.0	 MHz MHz
Internal operating frequency (f_{OSC}/2) Crystal External clock	 f_{OP} f_{OP}	 — dc	 4.0 4.0	 MHz MHz
Cycle time (see Figure 9-1)	t_{CYC}	250	—	ns
Crystal oscillator start-up time (see Figure 9-1)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}		100	ms
External RESET input pulse width	t_{RL}	1.5	—	t_{CYC}
Power-on RESET output pulse width 4064 cycle 16 cycle	 t_{PORL} t_{PORL}	 4064 16	 — —	 t_{CYC} t_{CYC}
Watchdog RESET output pulse width	t_{DOGL}	1.5	—	t_{CYC}
Watchdog time-out	t_{DOG}	6144	7168	t_{CYC}
EEPROM byte erase time 0 to 70 (standard) – 40 to 85 (extended)	 t_{ERA} t_{ERA}	 10 10	 — —	 ms ms
EEPROM byte program time(1) 0 to 70 (standard) – 40 to 85 (extended)	 t_{PROG} t_{PROG}	 10 10	 — —	 ms ms
Timer (see Figure I-1) Resolution(2) Input capture pulse width Input capture pulse period	 t_{RESL} t_{TH}, t_{TL} t_{TLTL}	 4 125 —(3)	 — — —	 t_{CYC} ns t_{CYC}
Interrupt pulse width (edge-triggered)	t_{ILIH}	125	—	ns
Interrupt pulse period	t_{ILIL}	—(4)	—	t_{CYC}
OSC1 pulse width	t_{OH}, t_{OL}	90	—	ns
Write/Erase endurance(5)(6)	—	10000		cycles
Data retention(5)(6)	—	10		years

(1) For bus frequencies less than 2 MHz, the internal RC oscillator should be used when programming the EEPROM.

(2) Since a 2-bit prescaler in the timer must count four external cycles (t_{CYC}), this is the limiting factor in determining the timer resolution.

(3) The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.

(4) The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.

(5) At a temperature of 85°C

(6) Refer to Reliability Monitor Report (current quarterly issue) for current failure rate information.