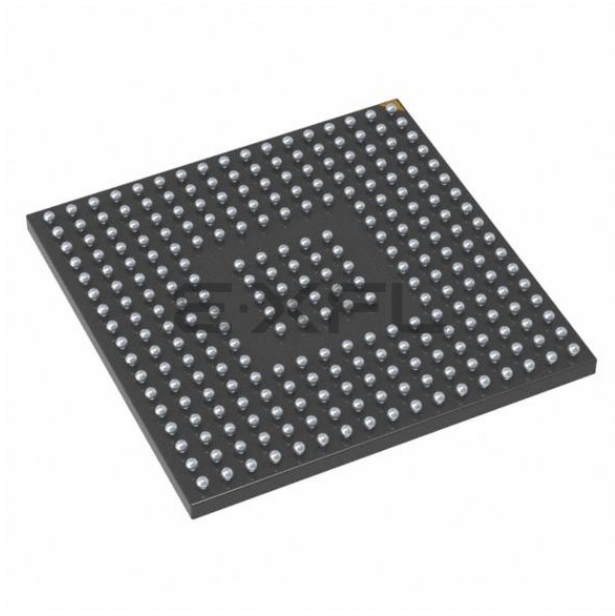

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	480MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MDIO, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 36x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UFBGA
Supplier Device Package	176+25UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32h750ibk6

2 Description

STM32H750xB devices are based on the high-performance Arm® Cortex®-M7 32-bit RISC core operating at up to 400 MHz. The Cortex® -M7 core features a floating point unit (FPU) which supports Arm® double-precision (IEEE 754 compliant) and single-precision data-processing instructions and data types. STM32H750xB devices support a full set of DSP instructions and a memory protection unit (MPU) to enhance application security.

STM32H750xB devices incorporate high-speed embedded memories with a Flash memory of 128 Kbytes, 1 Mbyte of RAM (including 192 Kbytes of TCM RAM, 864 Kbytes of user SRAM and 4 Kbytes of backup SRAM), as well as an extensive range of enhanced I/Os and peripherals connected to APB buses, AHB buses, 2x32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memory access.

All the devices offer three ADCs, two DACs, two ultra-low power comparators, a low-power RTC, a high-resolution timer, 12 general-purpose 16-bit timers, two PWM timers for motor control, five low-power timers, a true random number generator (RNG), and a cryptographic acceleration cell. The devices support four digital filters for external sigma-delta modulators (DFSDM). They also feature standard and advanced communication interfaces.

- Standard peripherals
  - Four I^2Cs
  - Four USARTs, four UARTs and one LPUART
  - Six SPIs, three I^2Ss in Half-duplex mode. To achieve audio class accuracy, the I^2S peripherals can be clocked by a dedicated internal audio PLL or by an external clock to allow synchronization.
  - Four SAI serial audio interfaces
  - One SPDIFRX interface
  - One SWPMI (Single Wire Protocol Master Interface)
  - Management Data Input/Output (MDIO) slaves
  - Two SDMMC interfaces
  - A USB OTG full-speed and a USB OTG high-speed interface with full-speed capability (with the ULPI)
  - One FDCAN plus one TT-CAN interface
  - An Ethernet interface
  - Chrom-ART Accelerator™
  - HDMI-CEC
- Advanced peripherals including
  - A flexible memory control (FMC) interface
  - A Quad-SPI Flash memory interface
  - A camera interface for CMOS sensors
  - An LCD-TFT display controller
  - A JPEG hardware compressor/decompressor

Refer to *Table 1: STM32H750xB features and peripheral counts* for the list of peripherals available on each part number.

Table 1. STM32H750xB features and peripheral counts (continued)

Peripherals	STM32H750VB	STM32H750IB	STM32H750XB
Operating temperatures	Ambient temperatures: –40 up to +85 °C(4)		
	Junction temperature: –40 to + 125 °C		
Package	LQFP100	UFBGA176+25	TFBGA240+25

1. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
2. Since the LQFP100 package does not feature the PDR_ON pin (tied internally to V_{DD}), the minimum V_{DD} value for this package is 1.71 V.
3. V_{DD}/V_{DDA} can drop down to 1.62 V by using an external power supervisor (see *Section 3.5.2: Power supply supervisor)* and connecting PDR_ON pin to V_{SS}. Otherwise the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.
4. The product junction temperature must be kept within the –40 to +125 °C temperature range.

3.41 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed two USB OTG high-speed (up to 480 Mbit/s) device/host/OTG peripheral. OTG-HS1 supports both full-speed and high-speed operations, while OTG-HS2 supports only full-speed operations. They both integrate the transceivers for full-speed operation (12 Mbit/s) and are able to operate from the internal HSI48 oscillator. OTG-HS1 features a UTMI low-pin interface (ULPI) for high-speed operation (480 Mbit/s). When using the USB OTG-HS1 in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripherals are compliant with the USB 2.0 specification and with the OTG 2.0 specification. They have software-configurable endpoint setting and supports suspend/resume. The USB OTG controllers require a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The main features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 9 bidirectional endpoints (including EP0)
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode (OTG_HS1 only)

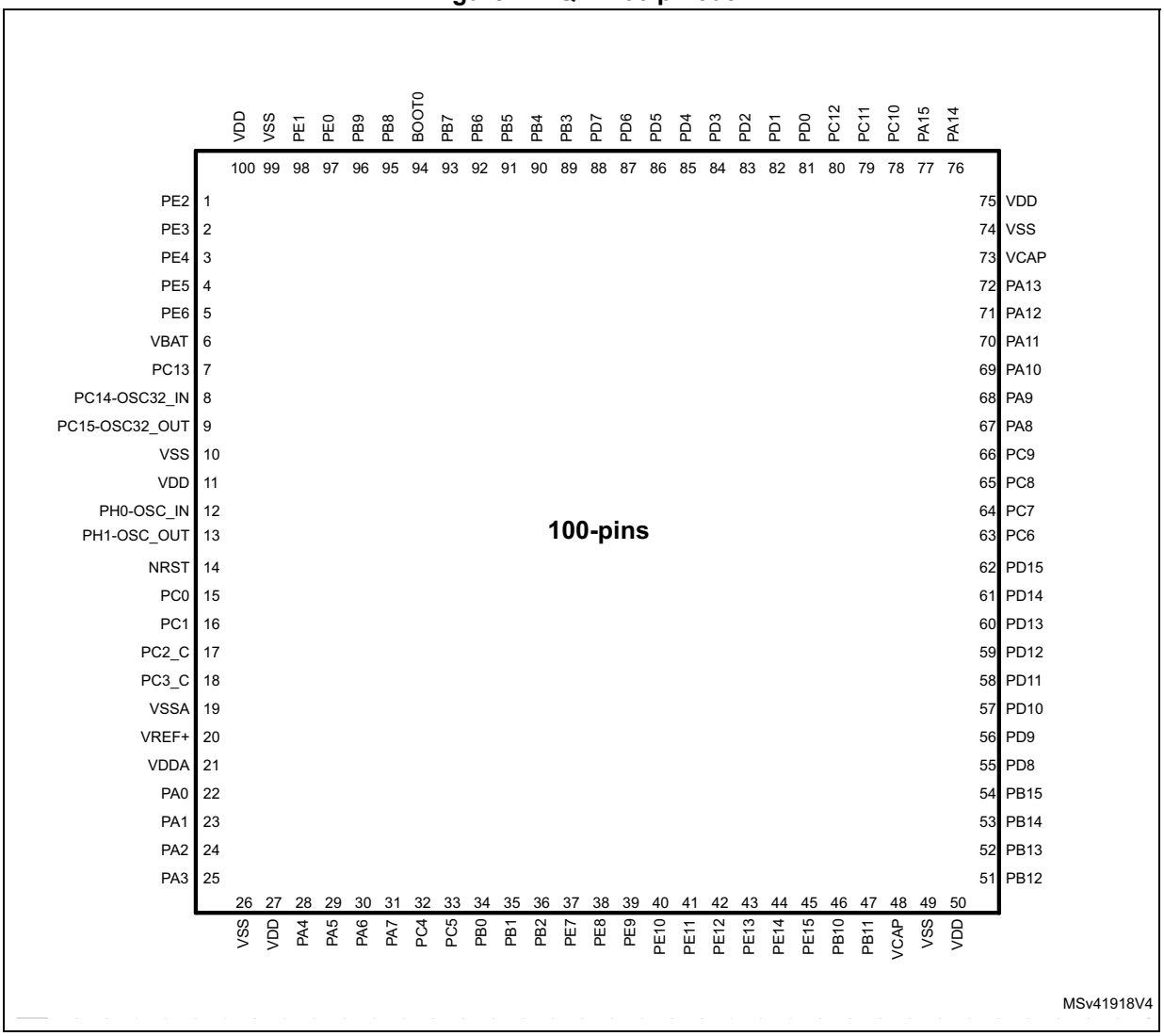
  The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.42 Ethernet MAC interface with dedicated DMA controller (ETH)

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

5 Pin descriptions

Figure 4. LQFP100 pinout



1. The above figure shows the package top view.

Table 7. STM32H750xB pin/ball definition (continued)

Pin/ball name			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	UFBGA176+25	TFBGA240 +25						
19	M1	P1	VSSA	S	-	-	-	-
-	N1	N1	VREF-	S	-	-	-	-
20	P1	M1	VREF+	S	-	-	-	-
21	R1	L1	VDDA	S	-	-	-	-
22	N3	N5(5)	PA0	I/O	FT_a	-	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, TIM15_BKIN, USART2_CTS_NSS, UART4_TX, SDMMC2_CMD, SAI2_SD_B, ETH_MII_CRS, EVENTOUT	ADC1_INP16, WKUP0
-	-	T1(5)	PA0_C	ANA	TT_a	-	-	ADC12_INN1, ADC12_INP0
23	N2	N4(5)	PA1	I/O	FT_ha	-	TIM2_CH2, TIM5_CH2, LPTIM3_OUT, TIM15_CH1N, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCK_B, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, LCD_R2, EVENTOUT	ADC1_INN16, ADC1_INP17
-	-	T2(5)	PA1_C	ANA	TT_a	-	-	ADC12_INP1
24	P2	N3	PA2	I/O	FT_a	-	TIM2_CH3, TIM5_CH3, LPTIM4_OUT, TIM15_CH1, USART2_TX, SAI2_SCK_B, ETH_MDIO, MDIOS_MDIO, LCD_R1, EVENTOUT	ADC12_INP14, WKUP1
-	F4	N2	PH2	I/O	FT_ha	-	LPTIM1_IN2, QUADSPI_BK2_IO0, SAI2_SCK_B, ETH_MII_CRS, FMC_SDCKE0, LCD_R0, EVENTOUT	ADC3_INP13
-	-	F5	VDD	S	-	-	-	-
-	J8	C16	VSS	S	-	-	-	-
-	G4	P2	PH3	I/O	FT_ha	-	QUADSPI_BK2_IO1, SAI2_MCK_B, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	ADC3_INN13, ADC3_INP14
-	H4	P3	PH4	I/O	FT_fa	-	I2C2_SCL, LCD_G5, OTG_HS_ULPI_NXT, LCD_G4, EVENTOUT	ADC3_INN14, ADC3_INP15
-	J4	P4	PH5	I/O	FT_fa	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	ADC3_INN15, ADC3_INP16

Table 9. Port B alternate functions (continued)

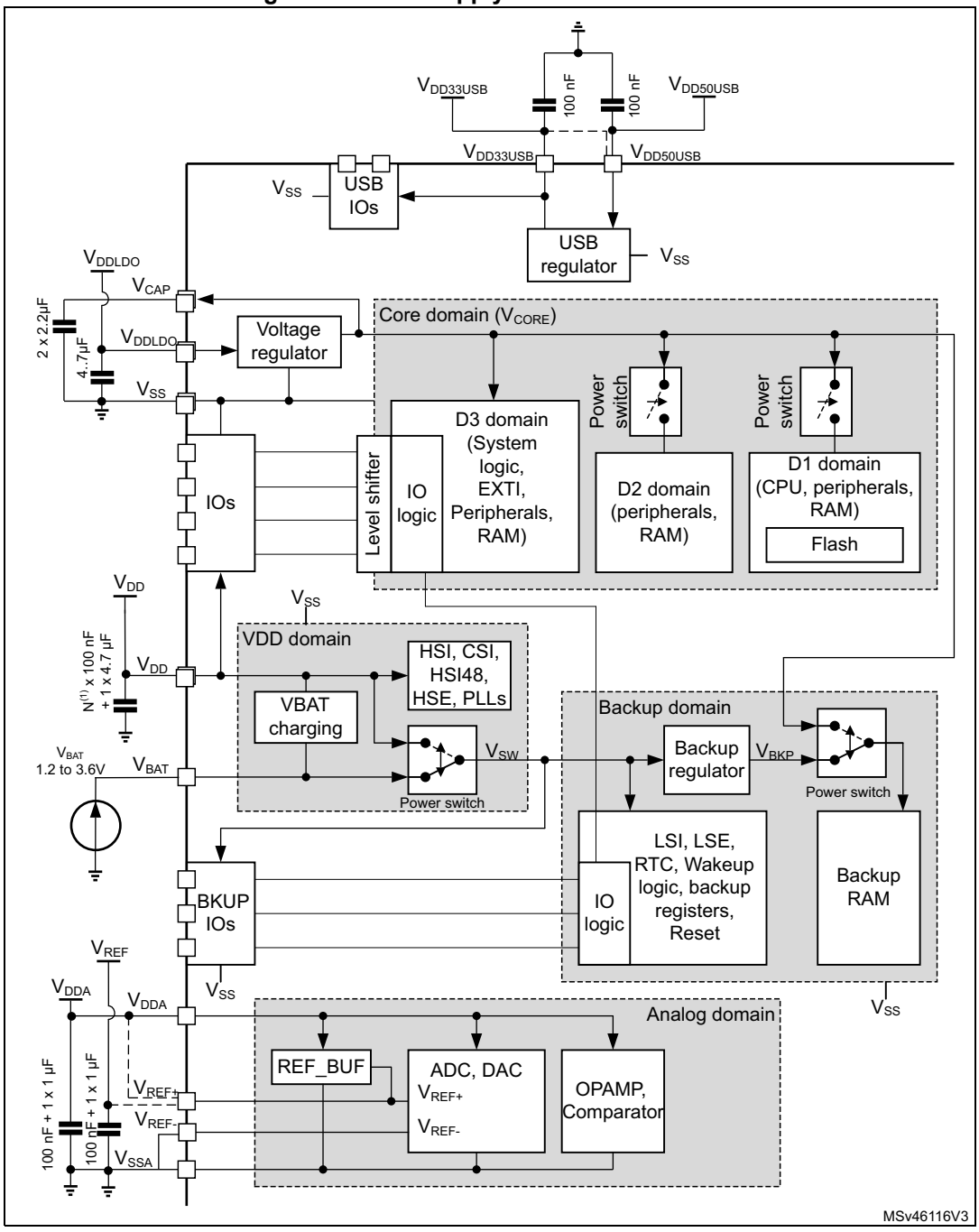
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port B	PB9	-	TIM17_CH1	TIM4_CH4	DFSDM_DATIN7	I2C1_SDA	SPI2_NSS/I2S2_WS	I2C4_SDA	SDMMC1_CDIR	UART4_TX	FDCAN1_TX	SDMMC2_D5	I2C4_SMBA	SDMMC1_D5	DCMI_D7	LCD_B7	EVENT-OUT
	PB10	-	TIM2_CH3	HRTIM_SCOUT	LPTIM2_IN1	I2C2_SCL	SPI2_SCK/I2S2_CK	DFSDM_DATIN7	USART3_TX	-	QUADSPI_BK1_NCS	OTG_HS_ULPI_D3	ETH_MII_RX_ER	-	-	LCD_G4	EVENT-OUT
	PB11	-	TIM2_CH4	HRTIM_SCIN	LPTIM2_ETR	I2C2_SDA	-	DFSDM_CKIN7	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH_MII_TX_EN/ETH_RMII_TX_EN	-	-	LCD_G5	EVENT-OUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS/I2S2_WS	DFSDM_DATIN1	USART3_CK	-	FDCAN2_RX	OTG_HS_ULPI_D5	ETH_MII_TXD0/ETH_RMII_TXD0	OTG_HS_ID	TIM1_BKIN_COMP12	UART5_RX	EVENT-OUT
	PB13	-	TIM1_CH1N	-	LPTIM2_OUT	-	SPI2_SCK/I2S2_CK	DFSDM_CKIN1	USART3_CTS_NSS	-	FDCAN2_TX	OTG_HS_ULPI_D6	ETH_MII_TXD1/ETH_RMII_TXD1	-	-	UART5_TX	EVENT-OUT
	PB14	-	TIM1_CH2N	TIM12_CH1	TIM8_CH2N	USART1_TX	SPI2_MISO/I2S2_SDI	DFSDM_DATIN2	USART3_RTS	UART4_RTS	SDMMC2_D0	-	-	OTG_HS_DM	-	-	EVENT-OUT
	PB15	RTC_REFIN	TIM1_CH3N	TIM12_CH2	TIM8_CH3N	USART1_RX	SPI2_MOSI/I2S2_SDO	DFSDM_CKIN2	-	UART4_CTS	SDMMC2_D1	-	-	OTG_HS_DP	-	-	EVENT-OUT

Table 11. Port D alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port D	PD0	-	-	-	DFSDM_CKIN6	-	-	SAI3_SCK_A	-	UART4_RX	FDCAN1_RX	-	-	FMC_D2/FMC_DA2	-	-	EVENT-OUT
	PD1	-	-	-	DFSDM_DATIN6	-	-	SAI3_SD_A	-	UART4_TX	FDCAN1_TX	-	-	FMC_D3/FMC_DA3	-	-	EVENT-OUT
	PD2	TRACED2	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	-	-	SDMMC1_CMD	DCMI_D11	-	EVENT-OUT
	PD3	-	-	-	DFSDM_CKOUT	-	SPI2_SCK/I2S2_CK	-	USART2_CTS_NSS	-	-	-	-	FMC_CLK	DCMI_D5	LCD_G7	EVENT-OUT
	PD4	-	-	HRTIM_FLT3	-	-	-	SAI3_FS_A	USART2_RTS	-	FDCAN1_RXFD_MODE	-	-	FMC_NOE	-	-	EVENT-OUT
	PD5	-	-	HRTIM_EEV3	-	-	-	-	USART2_TX	-	FDCAN1_TXFD_MODE	-	-	FMC_NWE	-	-	EVENT-OUT
	PD6	-	-	SAI1_D1	DFSDM_CKIN4	DFSDM_DATIN1	SPI3_MOSI/I2S3_SDO	SAI1_SD_A	USART2_RX	SAI4_SD_A	FDCAN2_RXFD_MODE	SAI4_D1	SDMMC2_CK	FMC_NWAIT	DCMI_D10	LCD_B2	EVENT-OUT
	PD7	-	-	-	DFSDM_DATIN4	-	SPI1_MOSI/I2S1_SDO	DFSDM_CKIN1	USART2_CK	-	SPDIFRX_IN0	-	SDMMC2_CMD	FMC_NE1	-	-	EVENT-OUT
	PD8	-	-	-	DFSDM_CKIN3	-	-	SAI3_SCK_B	USART3_TX	-	SPDIFRX_IN1	-	-	FMC_D13/FMC_DA13	-	-	EVENT-OUT
	PD9	-	-	-	DFSDM_DATIN3	-	-	SAI3_SD_B	USART3_RX	-	FDCAN2_RXFD_MODE	-	-	FMC_D14/FMC_DA14	-	-	EVENT-OUT
	PD10	-	-	-	DFSDM_CKOUT	-	-	SAI3_FS_B	USART3_CK	-	FDCAN2_TXFD_MODE	-	-	FMC_D15/FMC_DA15	-	LCD_B3	EVENT-OUT
	PD11	-	-	-	LPTIM2_IN2	I2C4_SMBA	-	-	USART3_CTS_NSS	-	QUADSPI_BK1_IO0	SAI2_SD_A	-	FMC_A16	-	-	EVENT-OUT
	PD12	-	LPTIM1_IN1	TIM4_CH1	LPTIM2_IN1	I2C4_SCL	-	-	USART3_RTS	-	QUADSPI_BK1_IO1	SAI2_FS_A	-	FMC_A17	-	-	EVENT-OUT
	PD13	-	LPTIM1_OUT	TIM4_CH2	-	I2C4_SDA	-	-		-	QUADSPI_BK1_IO3	SAI2_SCK_A	-	FMC_A18	-	-	EVENT-OUT
	PD14	-	-	TIM4_CH3	-	-	-	SAI3_MCLK_B	-	UART8_CTS	-	-	-	FMC_D0/FMC_DA0	-	-	EVENT-OUT
	PD15	-	-	TIM4_CH4	-	-	-	SAI3_MCLK_A	-	UART8_RTS	-	-	-	FMC_D1/FMC_DA1	-	-	EVENT-OUT

6.1.6 Power supply scheme

Figure 9. Power supply scheme



1. N corresponds to the number of VDD pins available on the package..

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

Table 36. Typical and maximum current consumption in VBAT mode

Symbol	Parameter	Conditions		Typ(1)				Max (3 V)				Unit
		Backup SRAM	RTC & LSE	1.2 V	2 V	3 V	3.4 V	T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 125°C	
I_{DD} (VBAT)	Supply current in standby mode	OFF	OFF	0.024	0.035	0.062	0.096	0.5(1)	4.1(1)	10(1)	24(1)	µA
		ON	OFF	1.4	1.6	1.8	1.8	4.4(1)	22(1)	48(1)	87(1)	
		OFF	ON	0.24	0.45	0.62	0.73	-	-	-	-	
		ON	ON	1.97	2.37	2.57	2.77	-	-	-	-	

1. Guaranteed by characterization results.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 58: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 37: Peripheral current consumption in Run mode*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDx} \times f_{SW} \times C_L$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDx} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C_L is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The I/O compensation cell is enabled.
- $f_{rcc\_c\_ck}$ is the CPU clock. $f_{PCLK} = f_{rcc\_c\_ck}/4$, and $f_{HCLK} = f_{rcc\_c\_ck}/2$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - $f_{rcc\_c\_ck}$ = 400 MHz (Scale 1), $f_{rcc\_c\_ck}$ = 300 MHz (Scale 2), $f_{rcc\_c\_ck}$ = 200 MHz (Scale 3)
- The ambient operating temperature is 25 °C and V_{DD}=3.3 V.

6.3.8 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O.

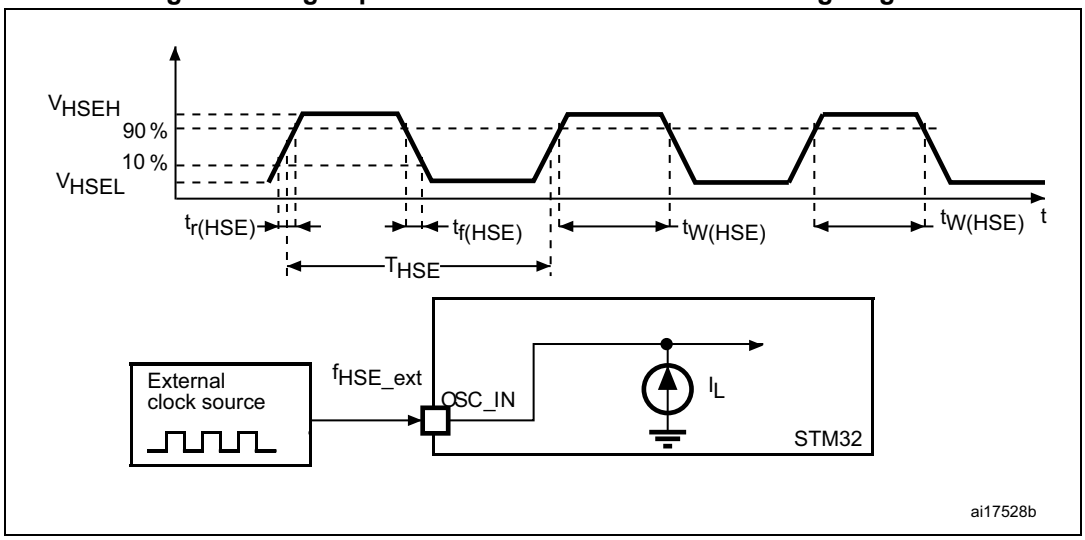
The external clock signal has to respect the *Table 58: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 12*.

Table 40. High-speed external user clock characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	4	25	50	MHz
V_{SW} (V_{HSEH}–V_{HSEL})	OSC_IN amplitude	$0.7V_{DD}$	-	V_{DD}	V
V_{DC}	OSC_IN input voltage	V_{SS}	-	$0.3V_{SS}$	
$t_{W(HSE)}$	OSC_IN high or low time	7	-	-	ns

1. Guaranteed by design.

Figure 12. High-speed external clock source AC timing diagram



Output buffer timing characteristics (HSLV option disabled)

The HSLV bit of SYSCFG_CCCSR register can be used to optimize the I/O speed when the product voltage is below 2.5 V.

Table 60. Output timing characteristics (HSLV OFF)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	12	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	12	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	16	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	4	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	16.6	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	33.3	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	13.3	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	25	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	20	
01	F_{max}(2)	Maximum frequency	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	60	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	15	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	80	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	15	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	110	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	20	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	5.2	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	4.2	
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	7.5	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	2.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	5.2	

Output buffer timing characteristics (HSLV option enabled)

Table 61. Output timing characteristics (HSLV ON)(1)

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	11	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	9	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	6.6	
01	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	50	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	58	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	66	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	6.6	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	4.8	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	3	
10	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	55	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	80	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	133	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	5.8	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	4	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	2.4	
11	F_{max}(2)	Maximum frequency	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	60	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	90	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	175	
	t_r/t_f(3)	Output high to low level fall time and output low to high level rise time	C=50 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	5.3	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	3.6	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V(4)	-	1.9	

1. Guaranteed by design.
2. The maximum frequency is defined with the following conditions:
   (t_r+t_f) ≤ 2/3 T
   Skew ≤ 1/20 T
   45%<Duty cycle<55%
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

Figure 25. Synchronous non-multiplexed PSRAM write timings

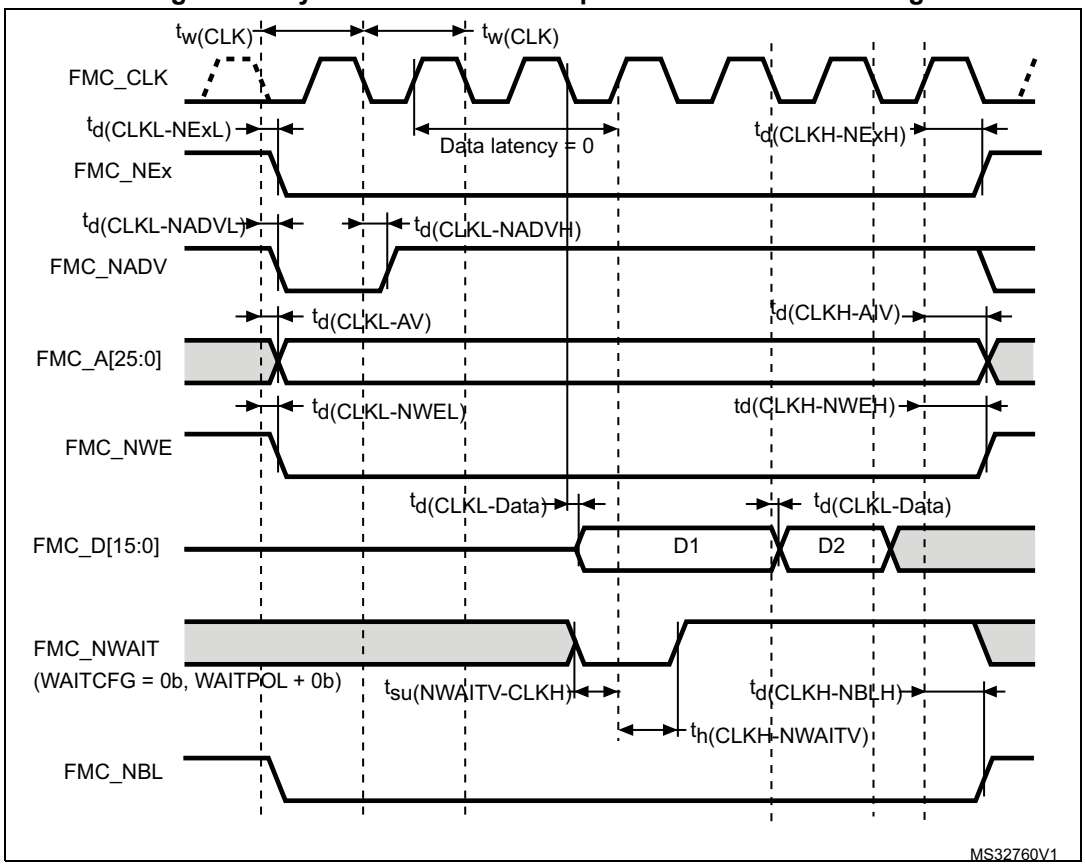
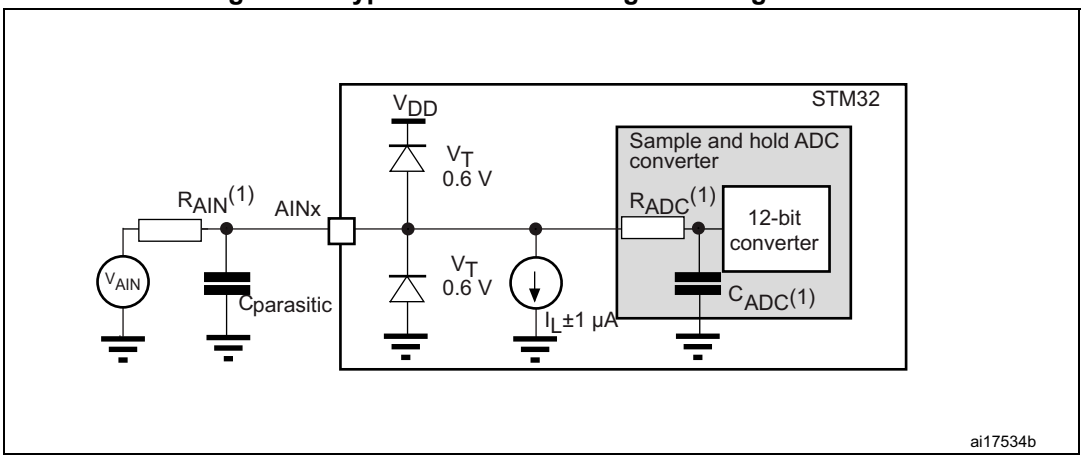


Table 74. Synchronous non-multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period	$2T_{fmc\_ker\_ck} - 1$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc\_ker\_ck}$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{fmc\_ker\_ck} + 1$	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{fmc\_ker\_ck} + 1$	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

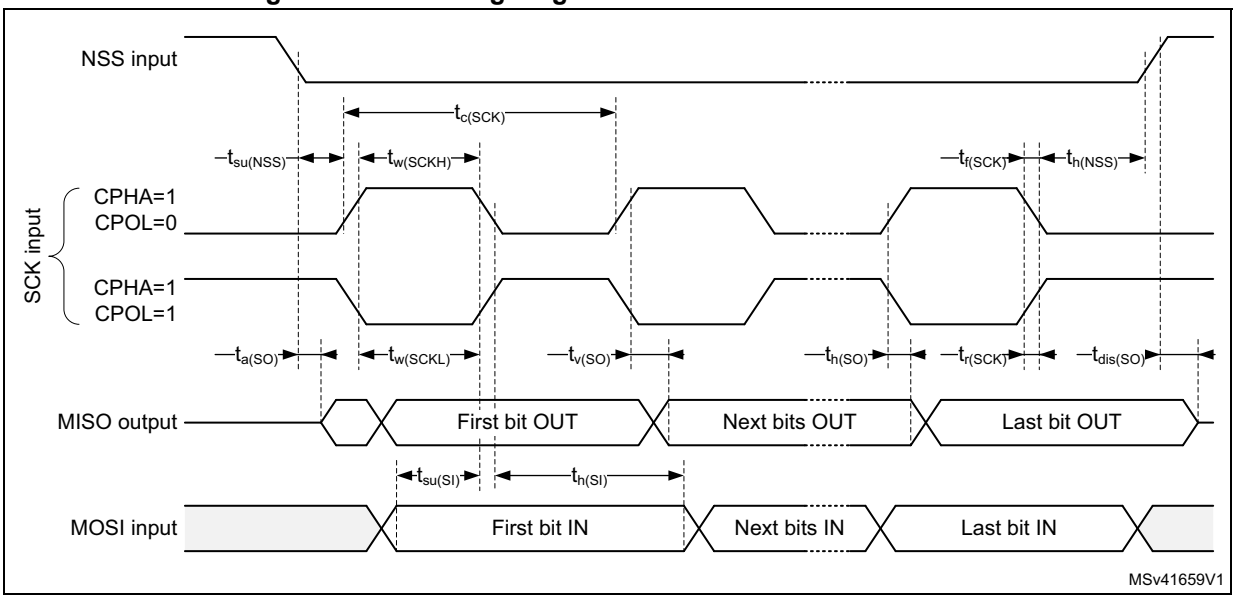
1. Guaranteed by characterization results.

Figure 35. Typical connection diagram using the ADC



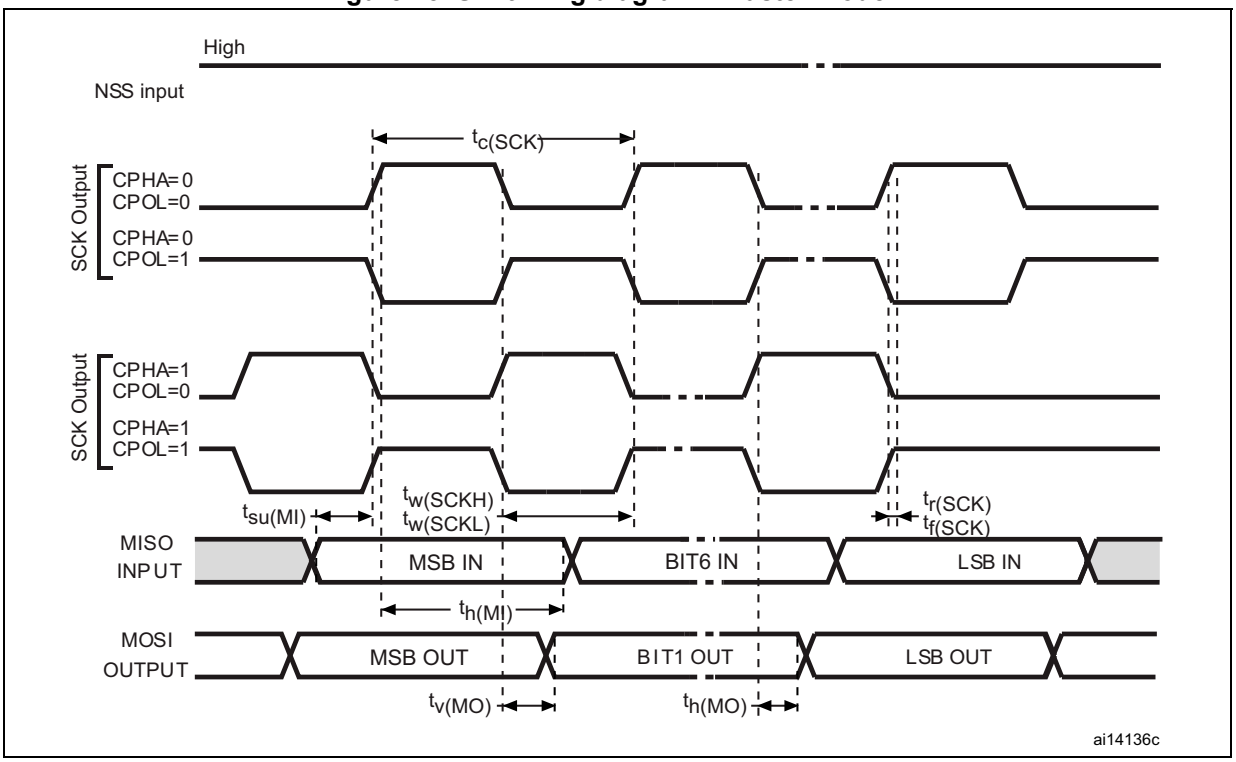
1. Refer to *Table 84* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

Figure 44. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 45. SPI timing diagram - master mode(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

USB OTG_FS characteristics

The USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 108. USB OTG_FS electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{DD33USB}$	USB transceiver operating voltage	-	3.0(1)	-	3.6	V
R_{PUI}	Embedded USB_DP pull-up value during idle	-	900	1250	1600	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception	-	1400	2300	3200	
Z_{DRV}	Output driver impedance(2)	Driver high and low	28	36	44	

1. The USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7 to 3.0 V voltage range.
2. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

USB OTG_HS characteristics

Unless otherwise specified, the parameters given in *Table 109* for ULPI are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output characteristics.

Table 109. Dynamic characteristics: USB ULPI(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SC}	Control in (ULPI_DIR, ULPI_NXT) setup time	-	0.5	-	-	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	-	6.5	-	-	
t_{SD}	Data in setup time	-	2.5	-	-	
t_{HD}	Data in hold time	-	0	-	-	
t_{DC}/t_{DD}	Data/control output delay	2.7 V < V_{DD} < 3.6 V, C_L = 20 pF	-	6.5	8.5	
		-	-	6.5	13	
		1.7 V < V_{DD} < 3.6 V, C_L = 15 pF	-			

1. Guaranteed by characterization results.

Table 115. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.