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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	480MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MDIO, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 36x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32h750vbt6

3.15 Flexible memory controller (FMC)

The FMC controller main features are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (4 memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-,16-,32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is the FMC kernel clock divided by 2.

3.16 Quad-SPI memory interface (QUADSPI)

All devices embed a Quad-SPI memory interface, which is a specialized communication interface targeting Single, Dual or Quad-SPI Flash memories. It supports both single and double datarate operations.

It can operate in any of the following modes:

- Direct mode through registers
- External Flash status register polling mode
- Memory mapped mode.

Up to 256 Mbytes of external Flash memory can be mapped, and 8-, 16- and 32-bit data accesses are supported as well as code execution.

The opcode and the frame format are fully programmable.

3.17 Analog-to-digital converters (ADCs)

The STM32H750xB devices embed three analog-to-digital converters, which resolution can be configured to 16, 14, 12, 10 or 8 bits. The sampling rates are respectively 3.6 MSPS, 4 MSPS, 4.5 MSPS, 5 MSPS and 6 MSPS when the ADC frequency (f_{ADC}) is 36 MHz.

Each ADC shares up to 20 external channels, performing conversions in the Single-shot or Scan mode. In Scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller, thus allowing to automatically transfer ADC converted values to a destination location without any software action.

3.29.2 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (Edge- or Center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

3.29.3 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32H750xB devices (see *Table 4* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The devices include 4 full-featured general-purpose timers: TIM2, TIM3, TIM4 and TIM5. TIM2 and TIM5 are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler while TIM3 and TIM4 are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. All timers feature 4 independent channels for input capture/output compare, PWM or One-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  TIM2, TIM3, TIM4 and TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM12, TIM13, TIM14, TIM15, TIM16, TIM17**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13, TIM14, TIM16 and TIM17 feature one independent channel, whereas TIM12 and TIM15 have two independent channels for input capture/output compare, PWM or One-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers or used as simple timebases.

All USART have a clock domain independent from the CPU clock, allowing the USARTx to wake up the MCU from Stop mode.The wakeup from Stop mode is programmable and can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Specific TXFIFO/RXFIFO status when FIFO mode is enabled.

All USART interfaces can be served by the DMA controller.

Table 5. USART features

USART modes/features(1)	USART1/2/3/6	UART4/5/7/8
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode (Master/Slave)	X	-
Smartcard mode	X	-
Single-wire Half-duplex communication	X	X
IrDA SIR ENDEC block	X	X
LIN mode	X	X
Dual clock domain and wakeup from low power mode	X	X
Receiver timeout interrupt	X	X
Modbus communication	X	X
Auto baud rate detection	X	X
Driver Enable	X	X
USART data length	7, 8 and 9 bits	
Tx/Rx FIFO	X	X
Tx/Rx FIFO size	16	

1. X = supported.

3.33 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-Power UART (LPUART1). The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUARTs embed a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

Figure 6. TFBGA240+25 ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS	PI6	PI5	PI4	PB5	VDD LDO	VCAP	PK5	PG10	PG9	PD5	PD4	PC10	PA15	PI1	PI0	VSS
B	VBAT	VSS	PI7	PE1	PB6	VSS	PB4	PK4	PG11	PJ15	PD6	PD3	PC11	PA14	PI2	PH15	PH14
C	PC15-OSC32_OUT	PC14-OSC32_IN	PE2	PE0	PB7	PB3	PK6	PK3	PG12	VSS	PD7	PC12	VSS	PI3	PA13	VSS	VDD LDO
D	PE5	PE4	PE3	PB9	PB8	PG15	PK7	PG14	PG13	PJ14	PJ12	PD2	PD0	PA10	PA9	PH13	VCAP
E	NC	PI9	PC13	PI8	PE6	VDD	PDR_ON	BOOT0	VDD	PJ13	VDD	PD1	PC8	PC9	PA8	PA12	PA11
F	NC	NC	PI10	PI11	VDD								PC7	PC6	PG8	PG7	VDD33 USB
G	PF2	NC	PF1	PF0	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PG5	PG6	VSS	VDD50 USB
H	PI12	PI13	PI14	PF3	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PG4	PG3	PG2	PK2
J	PH0-OSC_OUT	PH0-OSC_IN	VSS	PF5	PF4		VSS	VSS	VSS	VSS	VSS		VDD	PK0	PK1	VSS	VSS
K	NRST	PF6	PF7	PF8	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PJ11	VSS	NC	NC
L	VDDA	PC0	PF10	PF9	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PJ10	VSS	NC	NC
M	VREF+	PC1	PC2	PC3	VDD								VDD	PJ9	VSS	NC	NC
N	VREF-	PH2	PA2	PA1	PA0	PJ0	VDD	VDD	PE10	VDD	VDD	VDD	PJ8	PJ7	PJ6	VSS	NC
P	VSSA	PH3	PH4	PH5	PI15	PJ1	PF13	PF14	PE9	PE11	PB10	PB11	PH10	PH11	PD15	PD14	VDD
R	PC2_C	PC3_C	PA6	VSS	PA7	PB2	PF12	VSS	PF15	PE12	PE15	PJ5	PH9	PH12	PD11	PD12	PD13
T	PA0_C	PA1_C	PA5	PC4	PB1	PJ2	PF11	PG0	PE8	PE13	PH6	VSS	PH8	PB12	PB15	PD10	PD9
U	VSS	PA3	PA4	PC5	PB0	PJ3	PJ4	PG1	PE7	PE14	VCAP	VDD LDO	PH7	PB13	PB14	PD8	VSS

MSv41911V2

1. The above figure shows the package top view.

Table 7. STM32H750xB pin/ball definition (continued)

Pin/ball name			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	UFBGA176+25	TFBGA240 +25						
-	F9	U17	VSS	S	-	-	-	-
58	N14	R15	PD11	I/O	FT_h	-	LPTIM2_IN2, I2C4_SMBA, USART3_CTS_NSS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16, EVENTOUT	-
59	N13	R16	PD12	I/O	FT_fh	-	LPTIM1_IN1, TIM4_CH1, LPTIM2_IN1, I2C4_SCL, USART3_RTS, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17, EVENTOUT	-
60	M15	R17	PD13	I/O	FT_fh	-	LPTIM1_OUT, TIM4_CH2, I2C4_SDA, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT	-
-	K8	T12	VSS	S	-	-	-	-
-	J13	N11	VDD	S	-	-	-	-
61	M14	P16	PD14	I/O	FT_h	-	TIM4_CH3, SAI3_MCLK_B, UART8_CTS, FMC_D0/FMC_DA0, EVENTOUT	-
62	L14	P15	PD15	I/O	FT_h	-	TIM4_CH4, SAI3_MCLK_A, UART8_RTS, FMC_D1/FMC_DA1, EVENTOUT	-
-	-	N15	PJ6	I/O	FT	-	TIM8_CH2, LCD_R7, EVENTOUT	-
-	-	N14	PJ7	I/O	FT	-	TRGIN, TIM8_CH2N, LCD_G0, EVENTOUT	-
-	-	N10	VDD	S		-		-
-	F10	R8	VSS	S		-		-
-	-	N13	PJ8	I/O	FT	-	TIM1_CH3N, TIM8_CH1, UART8_TX, LCD_G1, EVENTOUT	-
-	-	M14	PJ9	I/O	FT	-	TIM1_CH3, TIM8_CH1N, UART8_RX, LCD_G2, EVENTOUT	-
-	-	L14	PJ10	I/O	FT	-	TIM1_CH2N, TIM8_CH2, SPI5_MOSI, LCD_G3, EVENTOUT	-
-	-	K14	PJ11	I/O	FT	-	TIM1_CH2, TIM8_CH2N, SPI5_MISO, LCD_G4, EVENTOUT	-
-	-	N8	VDD	S		-		-
-	G6	U1	VSS	S	-	-	-	-

Table 10. Port C alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/4/5/12/ HRTIM1	LPUART/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/ UART4/ DFSDM	SPI2/3/6/ USART1/2/3/6/UART7/ SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/ SDMMC1/ SPDIFRX	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX	SAI2/4/ TIM8/ QUADSPI/ SDMMC2/ OTG1_HS/ OTG2_FS/ LCD	I2C4/ UART7/ SWPMI1/ TIM1/8/ DFSDM/ SDMMC2/ MDIOS/ ETH	TIM1/8/FMC/SDMMC1/ MDIOS/ OTG1_FS/ LCD	TIM1/DCMI/LCD/ COMP	UART5/ LCD	SYS
Port C	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT-OUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT-OUT

Table 12. Port E alternate functions

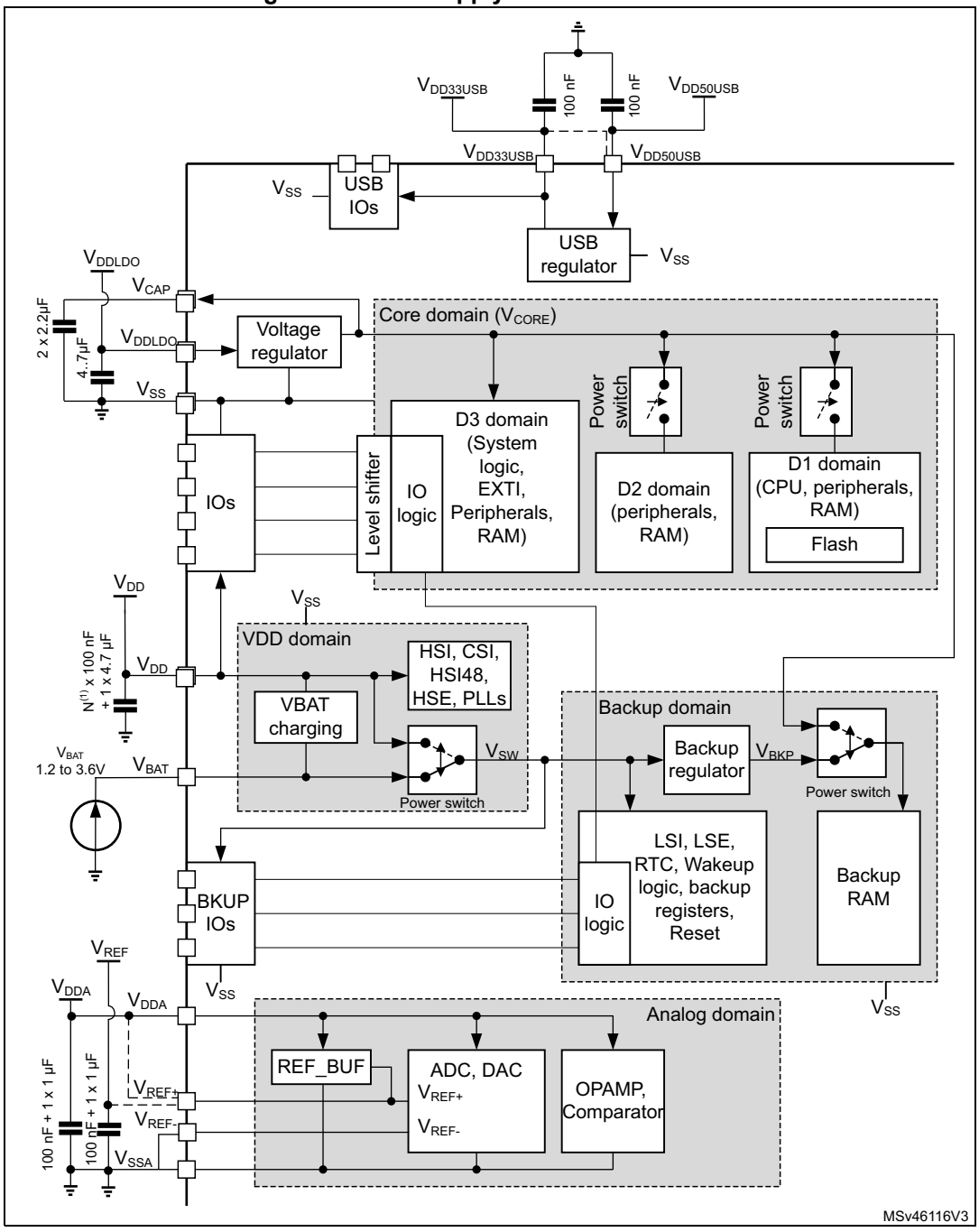
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/ 4/5/12/ HRTIM1	LPUART/ TIM8/ LPTIM2/3/4 /5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/ 5/6/CEC	SPI2/3/SAI1 /3/I2C4/ UART4/ DFSDM	SPI2/3/6/ USART1/2/ 3/6/UART7/ SDMMC1	SPI6/SAI2/ 4/UART4/5/ 8/LPUART/ SDMMC1/ SPDIFRX	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX	SAI2/4/ TIM8/ QUADSPI/ SDMMC2/ OTG1_HS/ OTG2_FS/ LCD	I2C4/ UART7/ SWPMI1/ TIM1/8/ DFSDM/ SDMMC2/ MDIOS/ ETH	TIM1/8/FMC /SDMMC1/ MDIOS/ OTG1_FS/ LCD	TIM1/DCMI /LCD/ COMP	UART5/ LCD	SYS
Port E	PE0	-	LPTIM1_ ETR	TIM4_ETR	HRTIM_ SCIN	LPTIM2_ ETR	-	-	-	UART8_RX	FDCAN1_ RXFD_ MODE	SAI2_MCK _A	-	FMC_NBL0	DCMI_D2	-	EVENT-OUT
	PE1	-	LPTIM1_IN2	-	HRTIM_ SCOUT	-	-	-	-	UART8_TX	FDCAN1_ TXFD_ MODE	-	-	FMC_NBL1	DCMI_D3	-	EVENT-OUT
	PE2	TRACE CLK	-	SAI1_CK1	-	-	SPI4_SCK	SAI1_MCLK _A	-	SAI4_ MCLK_A	QUADSPI_ BK1_IO2	SAI4_CK1	ETH_MII_ TXD3	FMC_A23	-	-	EVENT-OUT
	PE3	TRACED0	-	-	-	TIM15_BKIN	-	SAI1_SD_B	-	SAI4_SD_ B	-	-	-	FMC_A19	-	-	EVENT-OUT
	PE4	TRACED1	-	SAI1_D2	DFSDM_ DATIN3	TIM15_CH1 N	SPI4_NSS	SAI1_FS_A	-	SAI4_FS_A	-	SAI4_D2	-	FMC_A20	DCMI_D4	LCD_B0	EVENT-OUT
	PE5	TRACED2	-	SAI1_CK2	DFSDM_ CKIN3	TIM15_CH1	SPI4_ MISO	SAI1_SCK_ A	-	SAI4_SCK _A	-	SAI4_CK2	-	FMC_A21	DCMI_D6	LCD_G0	EVENT-OUT
	PE6	TRACED3	TIM1_BKIN 2	SAI1_D1	-	TIM15_CH2	SPI4_ MOSI	SAI1_SD_A	-	SAI4_SD_ A	SAI4_D1	SAI2_MCK _B	TIM1_BKIN 2_COMP12	FMC_A22	DCMI_D7	LCD_G1	EVENT-OUT
	PE7	-	TIM1_ETR	-	DFSDM_ DATIN2	-	-	-	UART7_RX	-	-	QUADSPI_ BK2_IO0	-	FMC_D4/ FMC_DA4	-	-	EVENT-OUT
	PE8	-	TIM1_CH1N	-	DFSDM_ CKIN2	-	-	-	UART7_TX	-	-	QUADSPI_ BK2_IO1	-	FMC_D5/ FMC_DA5	COMP_2_ OUT	-	EVENT-OUT
	PE9	-	TIM1_CH1	-	DFSDM_ CKOUT	-	-	-	UART7_ RTS	-	-	QUADSPI_ BK2_IO2	-	FMC_D6/ FMC_DA6	-	-	EVENT-OUT
	PE10	-	TIM1_CH2N	-	DFSDM_ DATIN4	-	-	-	UART7_ CTS	-	-	QUADSPI_ BK2_IO3	-	FMC_D7/ FMC_DA7	-	-	EVENT-OUT
	PE11	-	TIM1_CH2	-	DFSDM_ CKIN4	-	SPI4_NSS	-	-	-	-	SAI2_SD_B	-	FMC_D8/ FMC_DA8	-	LCD_G3	EVENT-OUT
	PE12	-	TIM1_CH3N	-	DFSDM_ DATIN5	-	SPI4_SCK	-	-	-	-	SAI2_SCK_ B	-	FMC_D9/ FMC_DA9	COMP_1_ OUT	LCD_B4	EVENT-OUT
	PE13	-	TIM1_CH3	-	DFSDM_ CKIN5	-	SPI4_ MISO	-	-	-	-	SAI2_FS_B	-	FMC_D10/ FMC_DA10	COMP_2_ OUT	LCD_DE	EVENT-OUT
	PE14	-	TIM1_CH4	-	-	-	SPI4_ MOSI	-	-	-	-	SAI2_MCK _B	-	FMC_D11/ FMC_DA11	-	LCD_CLK	EVENT-OUT
	PE15	-	TIM1_BKIN	-	-	-	HDMI__ TIM1_BKIN	-	-	-	-		-	FMC_D12/ FMC_DA12	TIM1_BKIN _COMP12	LCD_R7	EVENT-OUT

Table 16. Port I alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS/I2S2_WS	-	-	-	FDCAN1_RXFD_MODE	-	-	FMC_D24	DCMI_D13	LCD_G5	EVENT-OUT
	PI1	-	-	-	TIM8_BKIN2	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	TIM8_BKIN2_COMP12	FMC_D25	DCMI_D8	LCD_G6	EVENT-OUT
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO/I2S2_SDI	-	-	-	-	-	-	FMC_D26	DCMI_D9	LCD_G7	EVENT-OUT
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI/I2S2_SDO	-	-	-	-	-	-	FMC_D27	DCMI_D10	-	EVENT-OUT
	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	SAI2_MCK_A	TIM8_BKIN_COMP12	FMC_NBL2	DCMI_D5	LCD_B4	EVENT-OUT
	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	SAI2_SCK_A	-	FMC_NBL3	DCMI_VSYNC	LCD_B5	EVENT-OUT
	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	SAI2_SD_A	-	FMC_D28	DCMI_D6	LCD_B6	EVENT-OUT
	PI7	-	-	-	TIM8_CH3	-	-	-	-	-	-	SAI2_FS_A	-	FMC_D29	DCMI_D7	LCD_B7	EVENT-OUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT-OUT
	PI9	-	-	-	-	-	-	-	-	UART4_RX	FDCAN1_RX	-	-	FMC_D30	-	LCD_VSYNC	EVENT-OUT
	PI10	-	-	-	-	-	-	-	-	-	FDCAN1_RXFD_MODE	-	ETH_MII_RX_ER	FMC_D31	-	LCD_HSYNC	EVENT-OUT
	PI11	-	-	-	-	-	-	-	-	-	LCD_G6	OTG_HS_ULPI_DIR	-	-	-	-	EVENT-OUT
	PI12	-	-	-	-	-	-	-	-	-	-	-	ETH_TX_ER	-	-	LCD_HSYNC	EVENT-OUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_VSYNC	EVENT-OUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK	EVENT-OUT
	PI15	-	-	-	-	-	-	-	-	-	LCD_G2	-	-	-	-	LCD_R0	EVENT-OUT

6.1.6 Power supply scheme

Figure 9. Power supply scheme

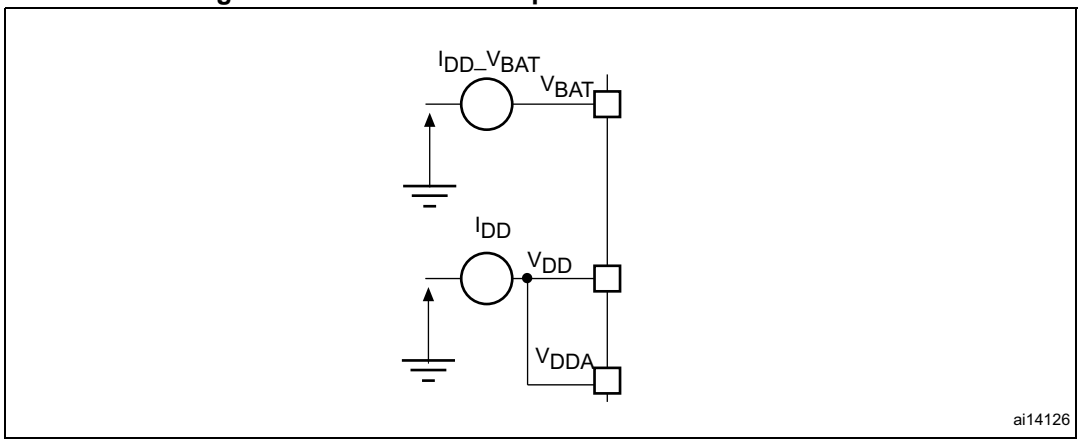


1. N corresponds to the number of VDD pins available on the package..

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

6.1.7 Current consumption measurement

Figure 10. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19: Voltage characteristics*, *Table 20: Current characteristics*, and *Table 21: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19. Voltage characteristics (1)

Symbols	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDLDO}, V_{DDA}, $V_{DD33USB}$, V_{BAT})	−0.3	4.0	V
V_{IN}(2)	Input voltage on FT_xxx pins	V_{SS}−0.3	Min(V_{DD}, V_{DDA}, $V_{DD33USB}$, V_{BAT}) +4.0(3)(4)	V
	Input voltage on TT_xx pins	V_{SS}-0.3	4.0	V
	Input voltage on BOOT0 pin	V_{SS}	9.0	V
	Input voltage on any other pins	V_{SS}-0.3	4.0	V
$\lvert\Delta V_{DDX}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV

1. All main power (V_{DD}, V_{DDA}, $V_{DD33USB}$, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 57* for the maximum allowed injected current values.
3. This formula has to be applied on power supplies related to the IO structure described by the pin definition table.
4. To sustain a voltage higher than 4V the internal pull-up/pull-down resistors must be disabled.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The I/O compensation cell is enabled.
- $f_{rcc\_c\_ck}$ is the CPU clock. $f_{PCLK} = f_{rcc\_c\_ck}/4$, and $f_{HCLK} = f_{rcc\_c\_ck}/2$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - $f_{rcc\_c\_ck}$ = 400 MHz (Scale 1), $f_{rcc\_c\_ck}$ = 300 MHz (Scale 2), $f_{rcc\_c\_ck}$ = 200 MHz (Scale 3)
- The ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 37. Peripheral current consumption in Run mode (continued)

Peripheral		I_{DD}(Typ)			Unit
		VOS1	VOS2	VOS3	
APB1 (continued)	UART5 registers	1.4	1.4	1	µA/MHz
	UART5 kernel	3.6	3.2	3.1	
	I2C1 registers	0.8	0.8	0.6	
	I2C1 kernel	2	1.8	1.7	
	I2C2 registers	0.7	0.7	0.4	
	I2C2 kernel	1.9	1.7	1.6	
	I2C3 registers	0.9	0.7	0.6	
	I2C3 kernel	2.1	1.9	1.9	
	HDMI-CEC registers	0.5	0.3	0.3	
	DAC1/2	1.4	1.1	0.9	
	USART7 registers	1.9	1.8	1.3	
	USART7 kernel	4	3.5	3.3	
	USART8 registers	1.6	1.5	1.2	
	USART8 kernel	4	3.6	3.3	
	CRS	3.4	3.1	2.9	
	SWPMI registers	2.3	2	2	
	SWPMI kernel	0.1	0.1	0.1	
	OPAMP	0.5	0.4	0.4	
	MDIO	2.7	2.4	2.3	
	FDCAN registers	16	15	14	
	FDCAN kernel	7.8	7.6	7.1	
	Bridge APB1	0.1	0.1	0.1	

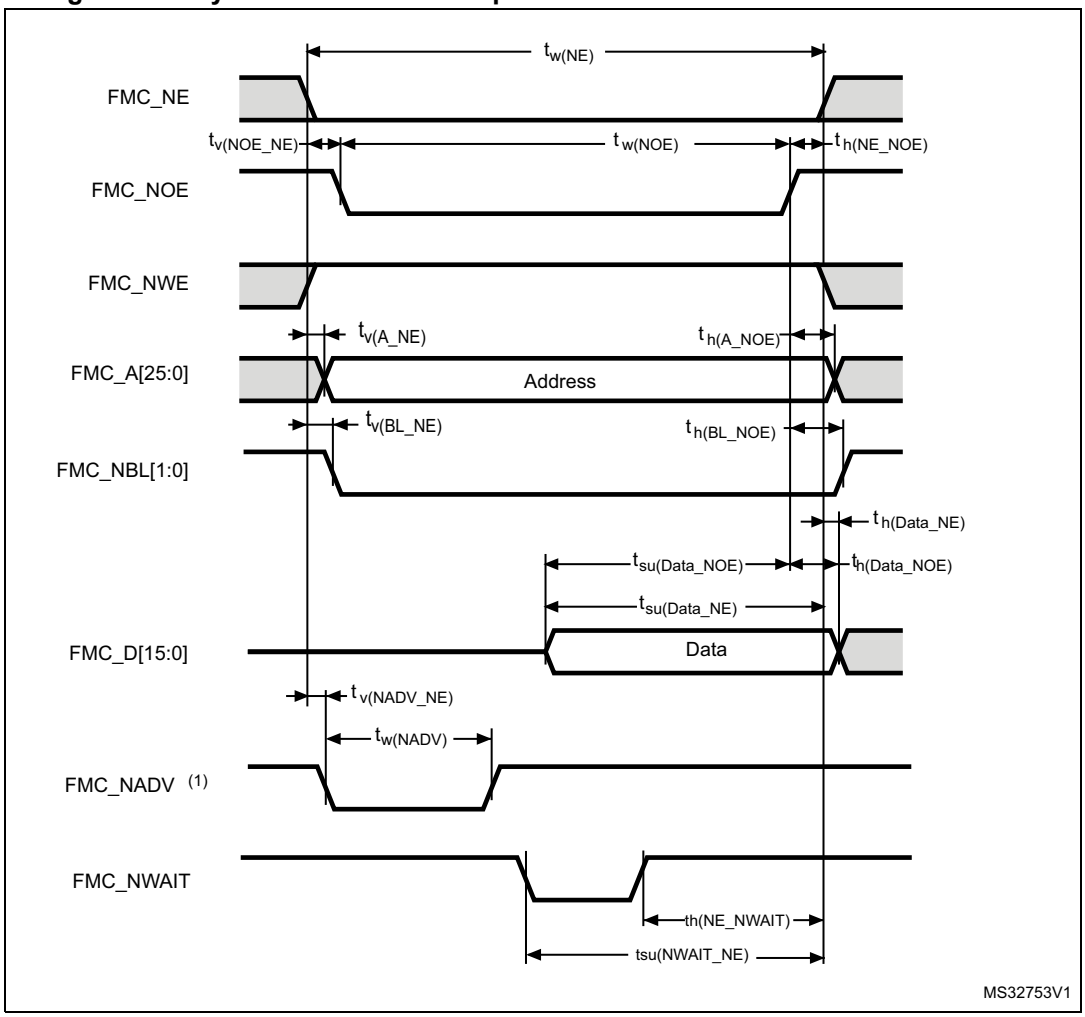
Table 37. Peripheral current consumption in Run mode (continued)

Peripheral		I_{DD}(Typ)			Unit
		VOS1	VOS2	VOS3	
APB4	SYSCFG	1	0.7	0.7	µA/MHz
	LPUART1 registers	1.1	1.1	1.1	
	LPUART1 kernel	2.6	2.4	2.1	
	SPI6 registers	1.6	1.5	1.4	
	SPI6 kernel	0.2	0.2	0.2	
	I2C4 registers	0.1	0.1	0.1	
	I2C4 kernel	2.4	2.1	2	
	LPTIM2 registers	0.5	0.5	0.5	
	LPTIM2 kernel	2.3	2.1	1.8	
	LPTIM3 registers	0.5	0.5	0.5	
	LPTIM3 kernel	2	2.1	1.5	
	LPTIM4 registers	0.5	0.5	0.5	
	LPTIM4 kernel	2	2	1.9	
	LPTIM5 registers	0.5	0.5	0.5	
	LPTIM5 kernel	2	1.8	1.5	
	COMP1/2	0.7	0.5	0.5	
	VREFBUF	0.6	0.4	0.4	
	RTC	1.2	1.1	1.1	
	SAI4 registers	1.6	1.5	1.4	
	SAI4 kernel	1.3	1.3	1.2	
	Bridge APB4	0.1	0.1	0.1	

Table 38. Peripheral current consumption in Stop, Standby and VBAT mode

Symbol	Parameter	Conditions	Typ	Unit
			3 V	
I_{DD}	RTC+LSE low drive	-	2.32	µA
	RTC+LSE medium-low drive	-	2.4	
	RTC+LSE medium-high drive	-	2.7	
	RTC+LSE High drive	-	3	

Figure 18. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

SDRAM waveforms and timings

In all timing tables, the $T_{fmc\_ker\_ck}$ is the fmc_ker_ck clock period, with the following FMC_SDCLK maximum values:

- For 1.8 V<V_{DD}<3.6V: FMC_CLK =100 MHz at 20 pF
- For 1.62 V<$_{DD}$<1.8 V, FMC_CLK =100 MHz at 30 pF

Figure 30. SDRAM read access waveforms (CL = 1)

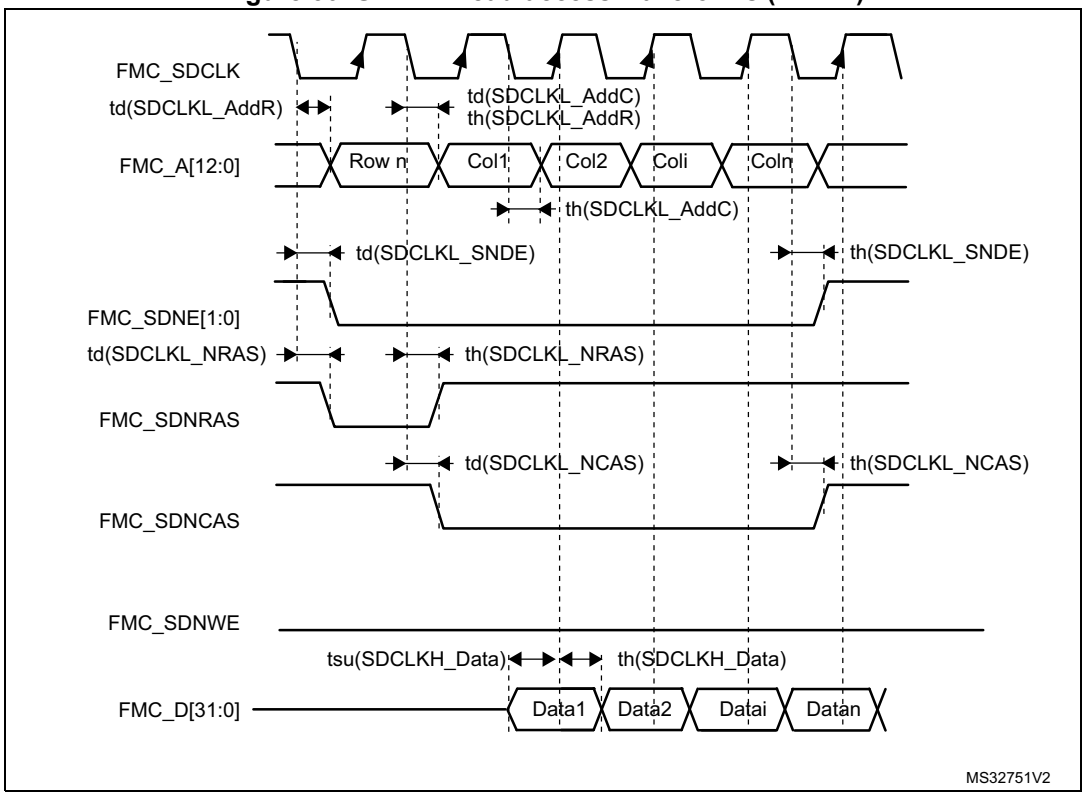


Table 77. SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck} - 1$	$2T_{fmc\_ker\_ck} + 0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	2	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	1	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL-SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0.5	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0.5	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

6.3.24 V_{BAT} monitoring characteristics

Table 91. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	26	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er(1)	Error on Q	–10	-	+10	%
t_{S_vbat}(1)	ADC sampling time when reading V_{BAT} input	9	-	-	µs

1. Guaranteed by design.

Table 92. V_{BAT} charging characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS in PWR_CR3= 0	-	5	-	KΩ
		VBRS in PWR_CR3= 1		1.5	-	

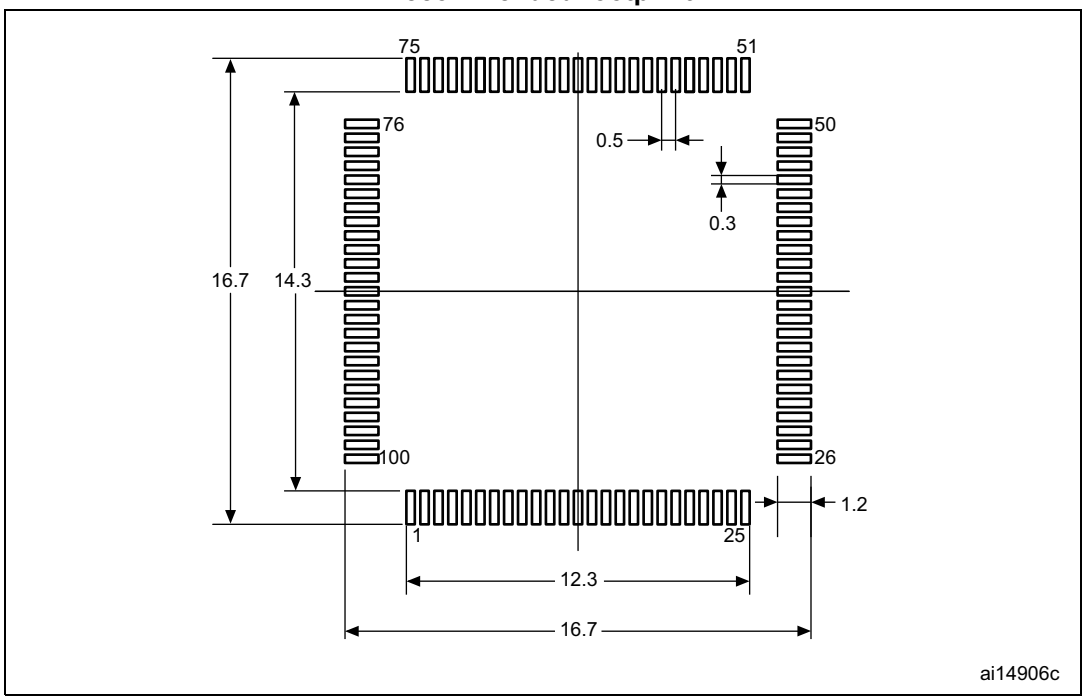
6.3.25 Voltage booster for analog switch

Table 93. Voltage booster for analog switch characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage	-	1.62	2-6	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	-	50	µs
$I_{DD(BOOST)}$	Booster consumption	1.62 V ≤ V_{DD} ≤ 2.7 V	-	-	125	µA
		2.7 V < V_{DD} < 3.6 V	-	-	250	

1. Guaranteed by characterization results.

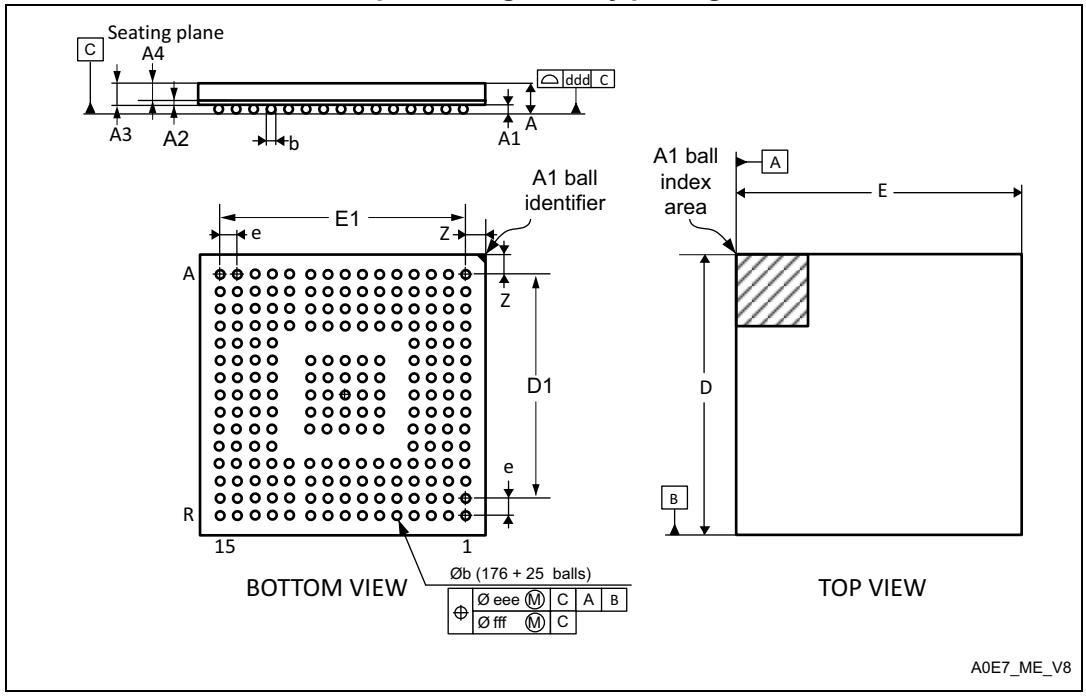
Figure 61. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

7.2 UFBGA176+25 package information

Figure 62. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline



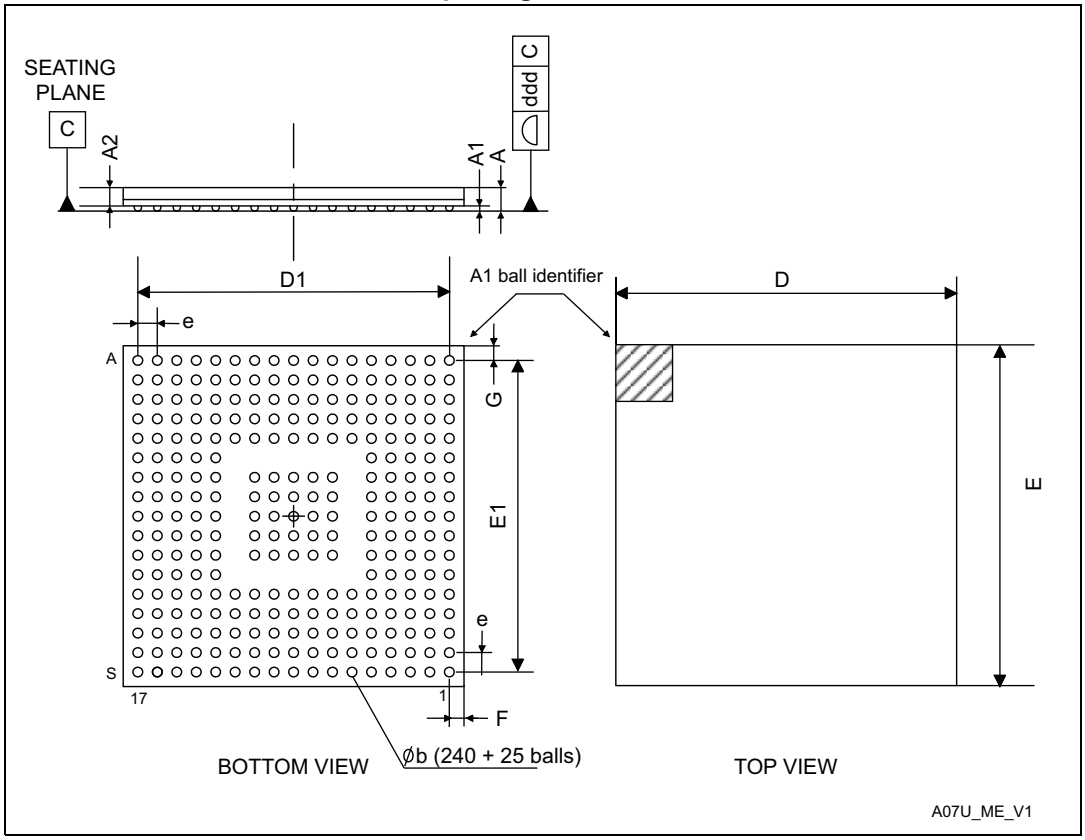
1. Drawing is not to scale.

Table 116. UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.130	-	-	0.0051	-
A3	-	0.450	-	-	0.0177	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

7.3 TFBGA240+25 package information

Figure 64. TFBGA - 240+25 ball, 14x14 mm, 0.8 mm pitch, fine pitch ball grid array package outline



1. Dimensions are expressed in millimeters.

7.4 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max × Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 120. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP100 - 14 x 14 mm /0.5 mm pitch	45.0	°C/W
	Thermal resistance junction-ambient UFBGA176+25 - 10 x 10 mm /0.65 mm pitch	37.4	
	Thermal resistance junction-ambient TFBGA240+25 - 14 x 14 mm / 0.8 mm pitch	36.6	

7.4.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.