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Renesas Electronics America Inc - R5S72670P144FP#VZ Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	EBI/EMI, I²C, IEBus, SCI, SIO, SPI, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	104
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1.5M x 8
Voltage - Supply (Vcc/Vdd)	1.15V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5s72670p144fp-vz

Peripheral Module	Setting Value for One Channel ({MID, RID})	MID	RID	Function
Compare match timer Channel 1	H'FF	B'111111	B'11	—
Renesas quad serial peripheral interface	H'A1	B'101000	B'01	Transmit
	H'A2		B'10	Receive

When MID or RID other than the values listed in table 10.3 is set, the operation of this LSI is not guaranteed. The transfer request from DMARS is valid only when the resource select bits (RS3 to RS0) in CHCR0 to CHCR15 have been set to B'1000. Otherwise, even if DMARS has been set, the transfer request source is not accepted.

Table 11.20 TIORL_0 (Channel 0)

				Description	
Bit 3 IOC3	**Bit 2 IOC2**	**Bit 1 IOC1**	**Bit 0 IOC0**	**TGRC_0 Function**	**TIOC0C Pin Function**
0	0	0	0	Output compare register*[2]	Output retained*[1]
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register*[2]	Input capture at rising edge
			1		Input capture at falling edge
		1	X		Input capture at both edges
	1	X	X		Capture input source is channel 1/count clock Input capture at TCNT_1 count-up/count-down

[Legend]

X: Don't care

Notes: 1. After power-on reset, 0 is output until TIOR is set.

2. When the BFA bit in TMDR_0 is set to 1 and TGRC_0 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 11.21 TIOR_1 (Channel 1)

				Description	
Bit 3 IOA3	Bit 2 IOA2	Bit 1 IOA1	Bit 0 IOA0	TGRA_1 Function	TIOC1A Pin Function
0	0	0	0	Output compare register	Output retained*
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	X		Input capture at both edges
	1	X	X		Input capture at generation of channel 0/TGRA_0 compare match/input capture

[Legend]

X: Don't care

Note: * After power-on reset, 0 is output until TIOR is set.

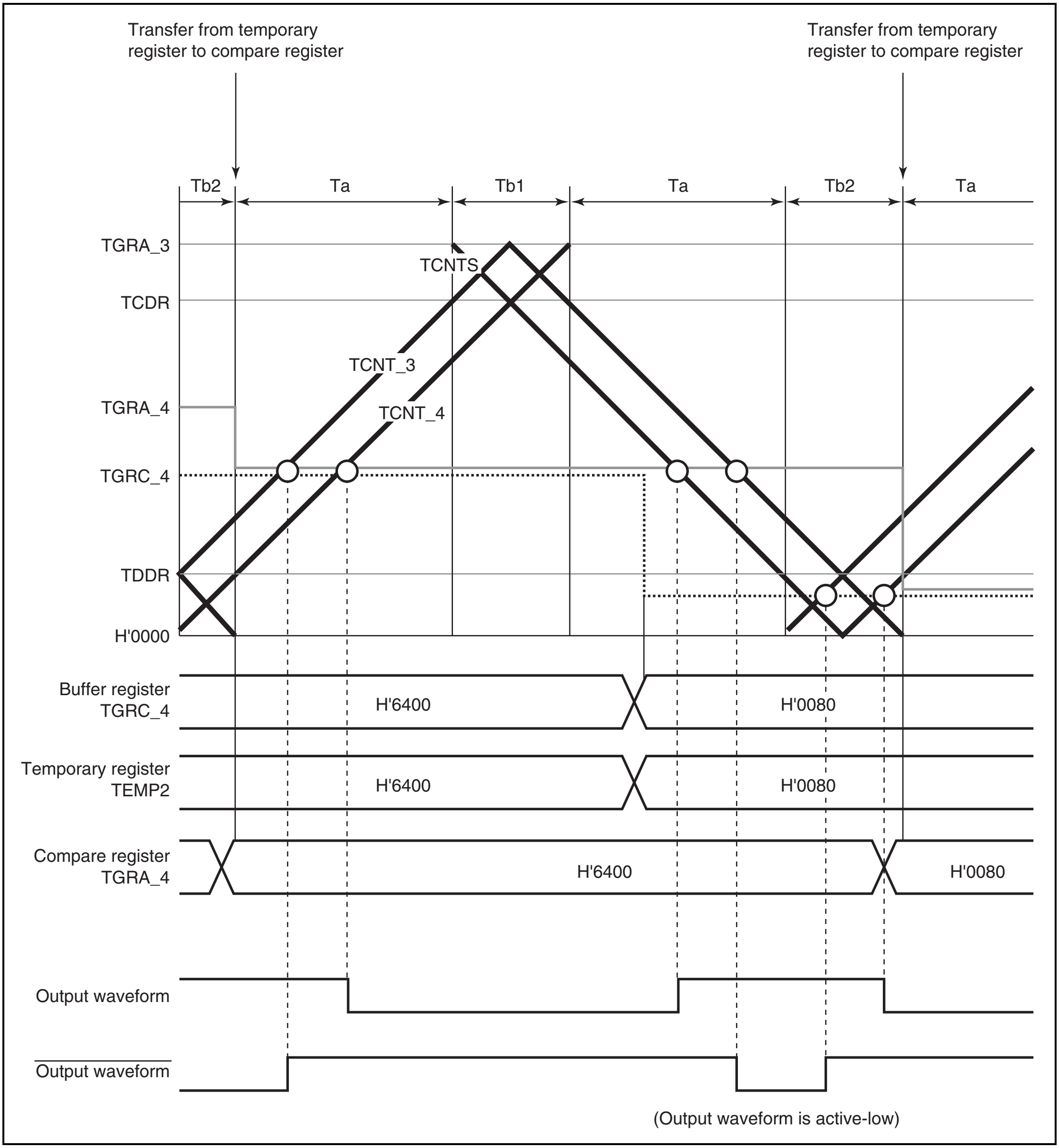


Figure 11.40 Example of Complementary PWM Mode Operation

Channel	Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
4	Serial mode register_4	SCSMR_4	R/W	H'0000	H'FFFEA000	16
	Bit rate register_4	SCBRR_4	R/W	H'FF	H'FFFEA004	8
	Serial control register_4	SCSCR_4	R/W	H'0000	H'FFFEA008	16
	Transmit FIFO data register_4	SCFTDR_4	W	Undefined	H'FFFEA00C	8
	Serial status register_4	SCFSR_4	R/(W)*[1]	H'0060	H'FFFEA010	16
	Receive FIFO data register_4	SCFRDR_4	R	Undefined	H'FFFEA014	8
	FIFO control register_4	SCFCR_4	R/W	H'0000	H'FFFEA018	16
	FIFO data count register_4	SCFDR_4	R	H'0000	H'FFFEA01C	16
	Serial port register_4	SCSPTR_4	R/W	H'0050	H'FFFEA020	16
	Line status register_4	SCLSR_4	R/(W)*[2]	H'0000	H'FFFEA024	16
	Serial extension mode register_4	SCEMR_4	R/W	H'0000	H'FFFEA028	16
5	Serial mode register_5	SCSMR_5	R/W	H'0000	H'FFFEA800	16
	Bit rate register_5	SCBRR_5	R/W	H'FF	H'FFFEA804	8
	Serial control register_5	SCSCR_5	R/W	H'0000	H'FFFEA808	16
	Transmit FIFO data register_5	SCFTDR_5	W	Undefined	H'FFFEA80C	8
	Serial status register_5	SCFSR_5	R/(W)*[1]	H'0060	H'FFFEA810	16
	Receive FIFO data register_5	SCFRDR_5	R	Undefined	H'FFFEA814	8
	FIFO control register_5	SCFCR_5	R/W	H'0000	H'FFFEA818	16
	FIFO data count register_5	SCFDR_5	R	H'0000	H'FFFEA81C	16
	Serial port register_5	SCSPTR_5	R/W	H'0050	H'FFFEA820	16
	Line status register_5	SCLSR_5	R/(W)*[2]	H'0000	H'FFFEA824	16
	Serial extension mode register_5	SCEMR_5	R/W	H’0000	H’FFFEA828	16

18.3 Register Descriptions

Table 18.2 shows the register configuration.

Table 18.2 Register Configuration

Channel	Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
0	I^{2}C bus control register 1	ICCR1_0	R/W	H'00	H'FFFEE000	8
	I^{2}C bus control register 2	ICCR2_0	R/W	H'7D	H'FFFEE001	8
	I^{2}C bus mode register	ICMR_0	R/W	H'38	H'FFFEE002	8
	I^{2}C bus interrupt enable register	ICIER_0	R/W	H'00	H'FFFEE003	8
	I^{2}C bus status register	ICSR_0	R/W	H'00	H'FFFEE004	8
	Slave address register	SAR_0	R/W	H'00	H'FFFEE005	8
	I^{2}C bus transmit data register	ICDRT_0	R/W	H'FF	H'FFFEE006	8
	I^{2}C bus receive data register	ICDRR_0	R/W	H'FF	H'FFFEE007	8
	NF2CYC register	NF2CYC_0	R/W	H'00	H'FFFEE008	8
1	I^{2}C bus control register 1	ICCR1_1	R/W	H'00	H'FFFEE400	8
	I^{2}C bus control register 2	ICCR2_1	R/W	H'7D	H'FFFEE401	8
	I^{2}C bus mode register	ICMR_1	R/W	H'38	H'FFFEE402	8
	I^{2}C bus interrupt enable register	ICIER_1	R/W	H'00	H'FFFEE403	8
	I^{2}C bus status register	ICSR_1	R/W	H'00	H'FFFEE404	8
	Slave address register	SAR_1	R/W	H'00	H'FFFEE405	8
	I^{2}C bus transmit data register	ICDRT_1	R/W	H'FF	H'FFFEE406	8
	I^{2}C bus receive data register	ICDRR_1	R/W	H'FF	H'FFFEE407	8
	NF2CYC register	NF2CYC_1	R/W	H'00	H'FFFEE408	8
2	I^{2}C bus control register 1	ICCR1_2	R/W	H'00	H'FFFEE800	8
	I^{2}C bus control register 2	ICCR2_2	R/W	H'7D	H'FFFEE801	8
	I^{2}C bus mode register	ICMR_2	R/W	H'38	H'FFFEE802	8
	I^{2}C bus interrupt enable register	ICIER_2	R/W	H'00	H'FFFEE803	8
	I^{2}C bus status register	ICSR_2	R/W	H'00	H'FFFEE804	8
	Slave address register	SAR_2	R/W	H'00	H'FFFEE805	8
	I^{2}C bus transmit data register	ICDRT_2	R/W	H'FF	H'FFFEE806	8
	I^{2}C bus receive data register	ICDRR_2	R/W	H'FF	H'FFFEE807	8
	NF2CYC register	NF2CYC_2	R/W	H'00	H'FFFEE808	8

(1) Message Control Field

STDID[10:0]: These bits set the identifier (standard identifier) of data frames and remote frames.

EXTID[17:0]: These bits set the identifier (extended identifier) of data frames and remote frames.

RTR (Remote Transmission Request bit): Used to distinguish between data frames and remote frames. This bit is overwritten by received CAN Frames depending on Data Frames or Remote Frames.

Important: Please note that, when ATX bit is set with the setting MBC = 001(bin), the RTR bit will never be set. When a Remote Frame is received, the CPU can be notified by the corresponding RFPR set or IRR[2] (Remote Frame Receive Interrupt), however, as this module needs to transmit the current message as a Data Frame, the RTR bit remains unchanged.

Important: In order to support automatic answer to remote frame when MBC = 001 (bin) is used and ATX = 1 the RTR flag must be programmed to zero to allow data frame to be transmitted.

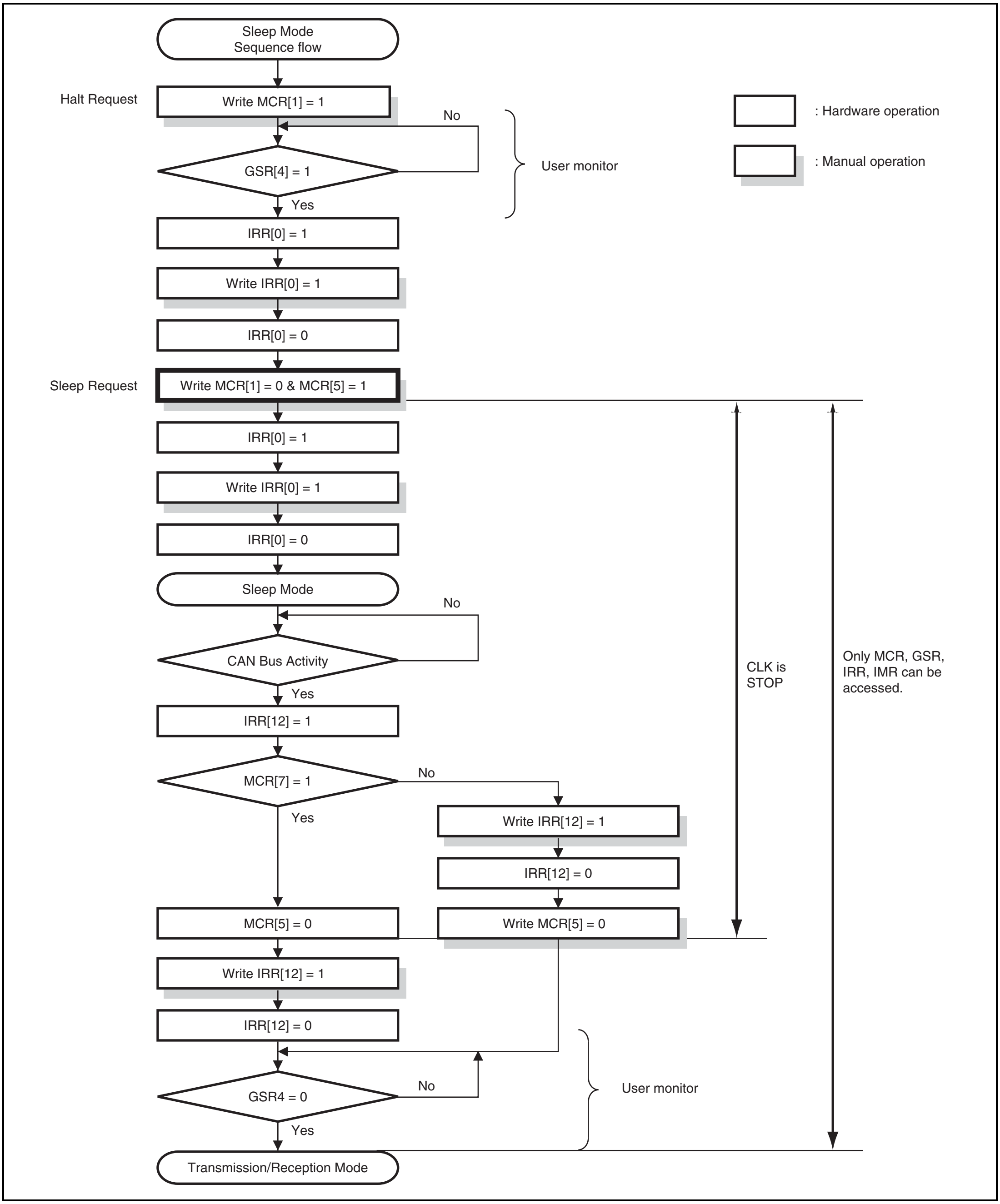
Note: When a Mailbox is configured to send a remote frame request the DLC used for transmission is the one stored into the Mailbox.

RTR	Description
0	Data frame
1	Remote frame

IDE (Identifier Extension bit): Used to distinguish between the standard format and extended format of CAN data frames and remote frames.

IDE	Description
0	Standard format
1	Extended format

The following diagram shows the flow to follow to move this module into sleep mode.



(3) Slave Address Field

The slave address field is a field to transmit an address (the slave address) of a unit (the slave unit) to be transmitted. The slave address field is comprised of slave address bits, a parity bit, and an acknowledge bit.

The slave address consists of 12 bits and the MSB is output first. The parity bit is output after the 12-bit slave address is transmitted to avoid receiving the slave address accidentally. The master unit then detects the acknowledgement from the slave unit to confirm that the slave unit exists on the bus. When the acknowledgement is detected, the master unit enters the control field output state. However, the master unit enters the control field output state without detecting the acknowledgement in broadcast communications.

The slave unit returns an acknowledgement when the slave addresses match and the parities of the master and slave addresses are correct. When the parity of either the master or slave address is incorrect, the slave unit decides that the master or slave address was not correctly received and does not return the acknowledgement. In this case, the master unit enters the waiting (monitor) state and communications ends.

In the case of broadcast communications, the slave address is used to identify the type of broadcast communications (group or general) as follows:

- When the slave address is H'FFF: General broadcast communications
- When the slave address is other than H'FFF: Group broadcast communications

Note: The group number is the upper 4-bit value of the slave address in group broadcast communications.

(4) Control Field

The control field is a field for transmitting the type and direction of the following data field. The control field is comprised of control bits, a parity bit, and an acknowledge bit.

The control bits consist of four bits and the MSB is output first.

The parity bit is output following the control bits. When the parity is correct, and the slave unit can implement the function required from the master unit, the slave unit returns an acknowledgement and enters the message length field output state. However, if the slave unit cannot implement the requirements from the master unit even though the parity is correct, or if the parity is not correct, the slave unit does not return an acknowledgement and returns to the waiting (monitor) state.

Bit	Bit Name	Initial Value	R/W	Description
0	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.

Note: * The controller is not capable of reading data in sector access mode.

(2) D0FIFOSEL, D1FIFOSEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCNT	REW	DCLRM	DREQE	MBW[1:0]		—	BIG END	—	—	—	—	CURPIPE[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W*	R/W	R/W	R/W	R/W	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	RCNT	0	R/W	Read Count Mode Specifies the read mode for the value in the DTLN bits in DnFIFOCTR. 0: The DTLN bit is cleared when all of the receive data has been read from the DnFIFO. (In double buffer mode, the DTLN bit value is cleared when all the data has been read from a single plane.) 1: The DTLN bit is decremented when the receive data is read from the DnFIFO. When accessing DnFIFO with the BFRE bit set to 1, set this bit to 0.
14	REW	0	R/W*	Buffer Pointer Rewind Specifies whether or not to rewind the buffer pointer. 0: The buffer pointer is not rewound. 1: The buffer pointer is rewound. When the selected pipe is in the receiving direction, setting this bit to 1 while the FIFO buffer is being read allows re-reading the FIFO buffer from the first data (in double buffer mode, re-reading the currently-read FIFO buffer plane from the first data is allowed). Do not set REW to 1 simultaneously with modifying the CURPIPE bits. Before setting REW to 1, be sure to check that FRDY is 1. To re-write to the FIFO buffer again from the first data for the pipe in the transmitting direction, use the BCLR bit.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	CURPIPE[3:0]	0000	R/W	FIFO Port Access Pipe Specification Specifies the pipe number for reading or writing data through the D0FIFO/D1FIFO port. 0000: No pipe specified 0001: Pipe 1 0010: Pipe 2 0011: Pipe 3 0100: Pipe 4 0101: Pipe 5 0110: Pipe 6 0111: Pipe 7 1000: Pipe 8 1001: Pipe 9 Other than above: Setting prohibited After writing to these bits, read these bits to check that the written value agrees with the read value before proceeding to the next process. Do not set the same pipe number to the CURPIPE bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL. Even if an attempt is made to modify the setting of these bits during access to the FIFO buffer, the current access setting is retained until the access is completed. Then, the modification becomes effective thus enabling continuous access.

Note: * Only 0 can be read and 1 can be written.

27.3.9 FIFO Port Control Registers (CFIFOCTR, D0FIFOCTR, D1FIFOCTR)

CFIFOCTR, D0FIFOCTR and D1FIFOCTR are registers that determine whether or not writing to the buffer memory has been finished, the buffer accessed from the CPU has been cleared, and the FIFO port is accessible. CFIFOCTR, D0FIFOCTR, and D1FIFOCTR are used for the corresponding FIFO ports.

These registers are initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BVAL	BCLR	FRDY	—	DTLN[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*2	R/W*1	R	R	R	R	R	R	R	R	R	R	R	R	R	R

(4) Setup of Data to be Transmitted using Isochronous Transfer when the Function Controller Function is Selected

With isochronous data transmission using this module in function controller function, after data has been written to the buffer memory, a data packet can be sent with the next frame in which an SOF packet is detected. This function is called the isochronous transfer transmission data setup function, and it makes it possible to designate the frame from which transmission began.

If a double buffer is used for the buffer memory, transmission will be enabled for only one of the two buffers even after the writing of data to both buffers has been completed, that buffer memory being the one to which the data writing was completed first. For this reason, even if multiple IN tokens are received, the only buffer memory that can be sent is one packet's worth of data.

When an IN token is received, if the buffer memory is in the transmission enabled state, this module transmits the data. If the buffer memory is not in the transmission enabled state, however, a zero-length packet is sent and an underrun error occurs.

Figure 27.20 shows an example of transmission using the isochronous transfer transmission data setup function with this module, when IITV = 0 (every frame) has been set.

28.7.21 Graphics Image Line Offset Registers (GROPSOFST1 and GROPSOFST2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	GROPSOFST[28:16]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GROPSOFST[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 0	GROPSOFST [28:0]	H'00000000	R/W	These bits specify the line offset for the graphics image. In 16-byte burst transfer: The lower four bits should always be 0000. In 128-byte burst transfer: The lower seven bits should always be 000_0000.

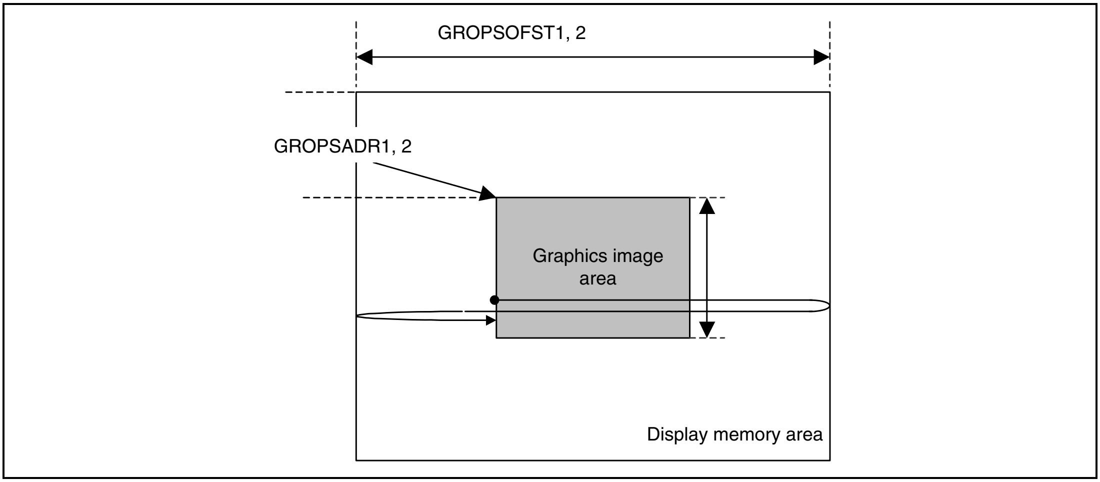


Figure 28.21 Graphics Image Memory Area Settings

The start (left side) address of line n is obtained by adding the base address register value (GROPSADR1 or GROPSADR2) and the line offset (GROPSOFST1 or GROPSOFST2) × n.

Bit	Bit Name	Initial Value	R/W	Description
8	CL	0	R/W	Internal Work Memory Clear Writing 1 to this bit clears the input FIFO, output FIFO, input buffer memory, intermediate memory, and accumulator. This bit is always read as 0. Even when SRCEN = 0, writing 1 to this bit clears the processing.
7 to 4	IFS[3:0]	All 0	R/W	Input Sampling Rate Specifies the input sampling rate. 0000: 8.0 kHz 0001: 11.025 kHz 0010: 12.0 kHz 0011: Setting prohibited 0100: 16.0 kHz 0101: 22.05 kHz 0110: 24.0 kHz 0111: Setting prohibited 1000: 32.0 kHz 1001: 44.1 kHz 1010: 48.0 kHz 1011: Setting prohibited 1100: Setting prohibited 1101: Setting prohibited 1110: Setting prohibited 1111: Setting prohibited Note: For channel 1, these bits are reserved and always read as 0. The write value should always be 0.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Port	Register Name	Abbreviation	R/W	Intial Value	Address	AccessSize
G	Port G port register 1	PGPR1	R	H'xxxx	H'FFFE38D8	8, 16, 32
	Port G port register 0	PGPR0	R	H'xxxx	H'FFFE38DA	8, 16
H	Port H control register 1	PHCR1	R/W	H'0000	H'FFFE38EC	8, 16, 32
	Port H control register 0	PHCR0	R/W	H'0000	H'FFFE38EE	8, 16
	Port H port register 0	PHPR0	R	H'xxxx	H'FFFE38FA	8, 16
J	Port J control register 1	PJCR1	R/W	H'0000	H'FFFE390C	8*[3], 16, 32
	Port J control register 0	PJCR0	R/W	H'0000	H'FFFE390E	8, 16
	Port J I/O register 0	PJIOR0	R/W	H'0000	H'FFFE3912	8, 16
	Port J data register 0	PJDR0	R/W	H'0000	H'FFFE3916	8, 16
	Port J port register 0	PJPR0	R	H'xxxx	H'FFFE391A	8, 16
—	Serial sound interface noise canceler control register	SNCR	R/W	H'0000	H'FFFE393E	8, 16

Notes: 1. The initial value depends on the boot mode of the LSI.

2. In 16- or 32-bit access, the register can be read but cannot be written to.

3. In 8-bit access, the register can be read but cannot be written to.

When deep standby mode is canceled by interrupts (NMI or realtime clock alarm) or changes on the pins for canceling, the deep standby cancel source flag register (DSFR) can be used to confirm which source has canceled the mode.

Pins retain the state immediately before the transition to deep standby mode. However, in system activation through the external memory, the retention of the states of the external memory control pins is cancelled so that programs can be fetched after cancellation of deep standby mode. Other pins, after cancellation of deep standby mode, continue to retain the pin states until writing 0 to the IOKEEP bit in DSFR after reading 1 from the same bit. In system activation from the on-chip data-retention RAM, after cancellation of deep standby mode, both the external memory control pins and other pins continues to retain the pin states until writing 0 to the IOKEEP bit in DSFR after reading 1 from the same bit. Reconfiguration of peripheral functions is required to return to the previous state of deep standby mode. Peripheral functions include all functions such as the clock pulse generator, interrupt controller, general I/O ports, and peripheral modules. After the reconfiguration, the retention of the pin state can be canceled and the LSI returns to the state prior to the transition to deep standby mode by reading 1 from the IOKEEP bit in DSFR and then writing 0 to it.

(4) Notes on Transition to Deep Standby Mode

If multiple canceling sources have been specified and multiple canceling sources are input, multiple cancel source flags will be set.

Section 34 User Debugging Interface

This LSI incorporates a user debugging interface for emulator support.

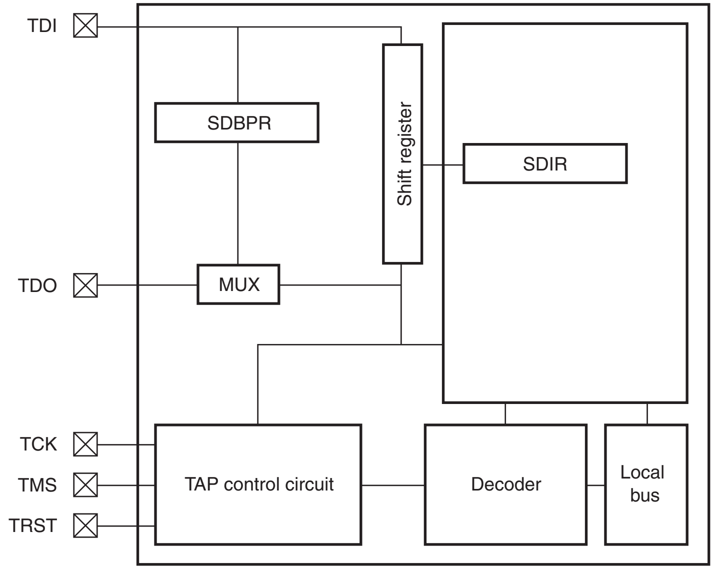
34.1 Features

The user debugging interface has reset and interrupt request functions.

The H-UDI in this LSI is used for emulator connection.

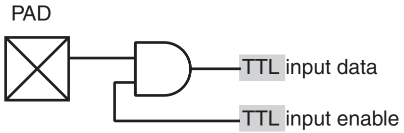
Refer to the emulator manual for the method of connecting the emulator.

Figure 34.1 shows a block diagram.



[Legend]
SDBPR: Bypass register
SDIR : Instruction register

Figure 34.1 Block Diagram

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>1.6 List of Pins
Table 1.4 List of Pins</td><td>35</td><td>Table amended
<table>
<tr><th rowspan="2">SH7266 Pin No.</th><th rowspan="2">SH7267 Pin No.</th><th colspan="2">Function 2</th></tr>
<tr><th>Symbol</th><th>I/O</th></tr>
<tr><td>138</td><td>166</td><td>$\overline{\mathrm{WE0}}$/DQML</td><td>O</td></tr>
<tr><td>139</td><td>167</td><td>$\overline{\mathrm{WE1}}$/DQMU/$\overline{\mathrm{WE}}$</td><td>O</td></tr>
<tr><td>140</td><td>168</td><td>$\overline{\mathrm{RAS}}$</td><td>O</td></tr>
</table></td></tr>
<tr><td>Figure 1.3 (2) Simplified Circuit Diagram (TTL AND Input Buffer)</td><td>37</td><td>Figure amended

</td></tr>
<tr><td>Table 9.19
Number of Idle Cycles Inserted between Access Cycles to Different Memory Types</td><td>343</td><td>Table amended
<table>
<tr><th></th><th colspan="8">Next Cycle</th></tr>
<tr><th>Previous Cycle</th><th>SRAM</th><th>Burst ROM (Asynchronous)</th><th>MPX-I/O</th><th>Byte SRAM (BAS = 0)</th><th>Byte SRAM (BAS = 1)</th><th>SDRAM</th><th>PCMCIA</th><th>Burst ROM (Synchronous)</th></tr>
<tr><td>SRAM</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0/1*1</td><td>0/1*1</td><td>0</td><td>0</td></tr>
<tr><td>Burst ROM (asynchronou s)</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0/1*1</td><td>0/1*1</td><td>0</td><td>0</td></tr>
<tr><td>MPX-I/O</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>Byte SRAM (BAS = 0)</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0/1*1</td><td>0/1*1</td><td>0</td><td>0</td></tr>
<tr><td>Byte SRAM (BAS = 1)</td><td>0/1*1</td><td>0/1*1</td><td>1/2*1</td><td>0/1*1</td><td>0</td><td>0</td><td>0/1*1</td><td>0/1*1</td></tr>
</table></td></tr>
<tr><td>11.1 Features</td><td>411</td><td>Description amended
• 25 interrupt sources</td></tr>
<tr><td>11.3.23 Timer Cycle Data Register (TCDR)</td><td>478</td><td>Description amended
TCDR is a 16-bit register used only in complementary PWM mode. Set half the PWM carrier sync value (a value of two times TDDR + 3 or greater) as the TCDR register value.</td></tr>
<tr><td>Figure 11.20 Cascaded Operation Setting Procedure</td><td>500</td><td>Description amended
[1] Set bits TPSC2 to TPSC0 in the channel 1 TCR to B'111 to select TCNT_2 overflow/underflow counting.</td></tr>
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