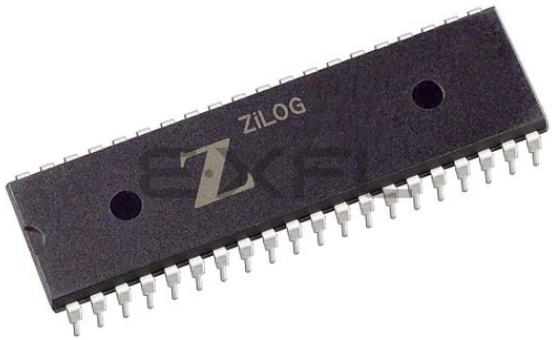


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	-
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e2304psc

GENERAL DESCRIPTION (Continued)

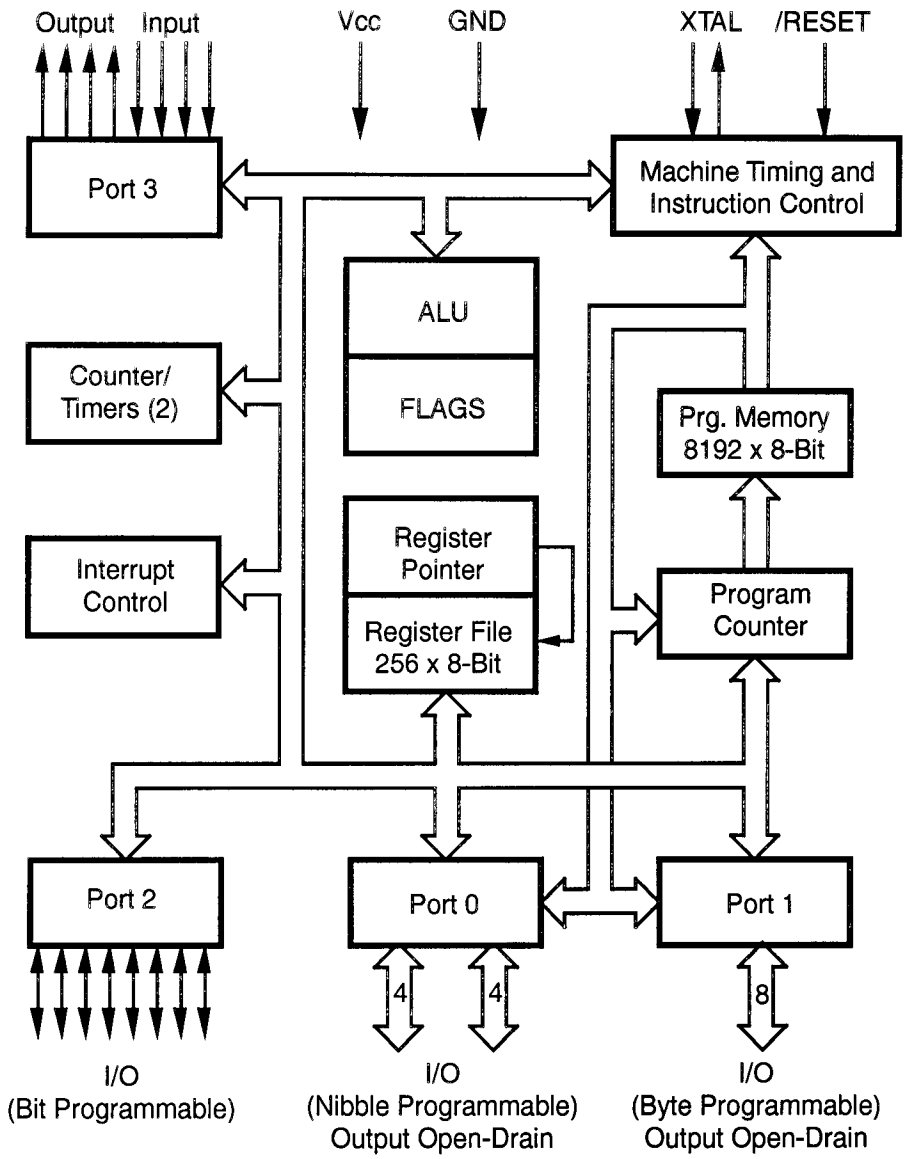


Figure 1. Functional Block Diagram

PIN DESCRIPTION (Continued)

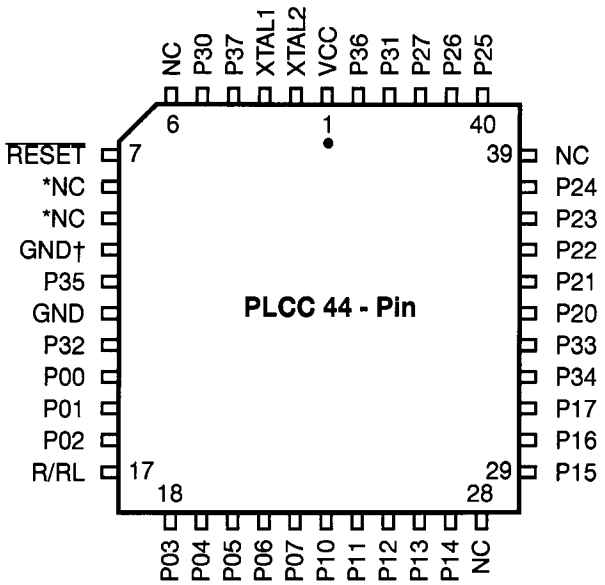


Figure 3. 44-Pin PLCC Pin Configuration

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	N/C	Not Connected	
7	$\overline{\text{RESET}}$	Reset	Input
8	*NC	Not Connected	
9	*NC	Not Connected	
10	GND†	Ground	
11	P35	Port 3, Pin 5	Output
12	GND	Ground	Input
13	P32	Port 3, Pin 2	Input
14-16	P00-P02	Port 0, Pins 0,1,2	In/Output
17	R/RL	ROM/ROMless Control	Input

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
18-22	P03-P07	Port 0, Pins 3,4,5,6,7	In/Output
23-27	P10-P14	Port 1, Pins 0,1,2,3,4	In/Output
28	NC	Not Connected	
29-31	P15-P17	Port 1, Pins 5,6,7	In/Output
32	P34	Port 3, Pin 4	Output
33	P33	Port 3, Pin 3	Input
34-38	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
39	NC	Not Connected	
40-42	P25-P27	Port 2, Pins 5,6,7	In/Output
43	P31	Port 3, Pin 1	Input
44	P36	Port 3, Pin 6	Output

Notes:
*Pins 8 and 9 are used for testing purposes. The customer must use these pins as "floaters."
†To avoid System ESD failure in Standard Mode, Pin 10 must be grounded.

PIN DESCRIPTION

EPROM Mode

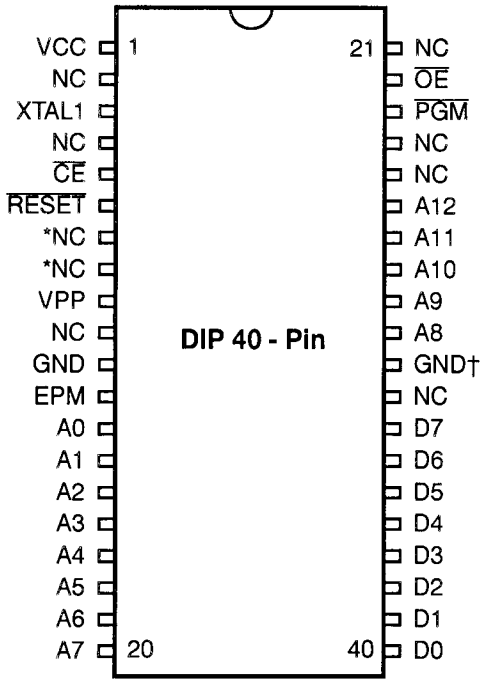


Figure 4. 40-Pin DIP Pin Configuration (EPROM Mode)

Table 3. 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	NC	Not Connected	
3	XTAL1	Crystal, Oscillator Clock	Input
4	NC	Not Connected	Input
5	$\overline{CE}$	Chip Enable	Input
6	$\overline{RESET}$	Reset	Input
7	*NC	Not Connected	
8	*NC	Not Connected	
9	VPP	Prog Voltage	Input
10	NC	Not Connected	
11	GND	Ground	Input
12	EPM	EPROM Prog Mode	Input
13-20	A0-A7	Address 0,1,2,3,4,5,6,7	Input
21-28	D0-D7	Data 0,1,2,3,4,5,6,7	In/Output
29	NC	Not Connected	
30	GND†	Ground	Input
31-35	A8-A12	Address 8,9,10,11,12	Input
36-37	NC	Not Connected	
38	/PGM	Prog Mode	Input
39	/OE	Output Enable	Input
40	NC	Not Connected	

Notes:
*Pins 7 and 8 are used for testing purposes. The customer must use these pins as "floaters."
†To avoid System ESD failure in Standard Mode, Pin 30 must be grounded.

PIN DESCRIPTION (Continued)

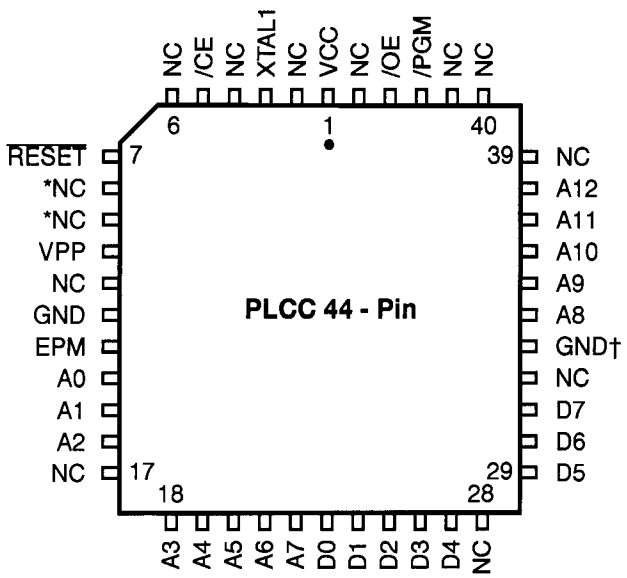


Figure 5. 44-Pin PLCC Pin Configuration (EPROM Mode)

Table 4. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	NC	Not Connected	
3	XTAL1	Crystal, Oscillator Clock	Input
4	NC	Not Connected	
5	/CE	Chip Enable	Input
6	NC	Not Connected	
7	$\overline{\text{RESET}}$	Reset	Input
8	*NC	Not Connected	
9	*NC	Not Connected	
10	V_{PP}	Prog Voltage	Input
11	NC	Not Connected	
12	GND	Ground	Input
13	EPM	EPROM Prog. Mode	Input
14-16	A0-A2	Address 0,1,2	Input
17	NC	Not Connected	
18-22	A3-A7	Address 3,4,5,6,7	Input

Table 4. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
23-27	D0-D4	Data 0,1,2,3,4	In/Output
28	NC	Not Connected	
29-31	D5-D7	Data 5,6,7	In/Output
32	NC	Not Connected	
33	GND†	Ground	Input
34-38	A8-A12	Address 8,9,10,11,12	Input
39-41	NC	Not Connected	
42	/PGM	Prog. Mode	Input
43	/OE	Output Enable	Input
44	NC	Not Connected	

Notes:
*Pins 8 and 9 are used for testing purposes. The customer must use these pins as "floaters."
†To avoid System ESD failure in Standard Mode, Pin 33 must be grounded.

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	C
T_A	Oper Ambient Temp		†	C

Notes:
* Voltages on all pins with respect to GND.
13.0 V Maximum on P33-P30.
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 6).

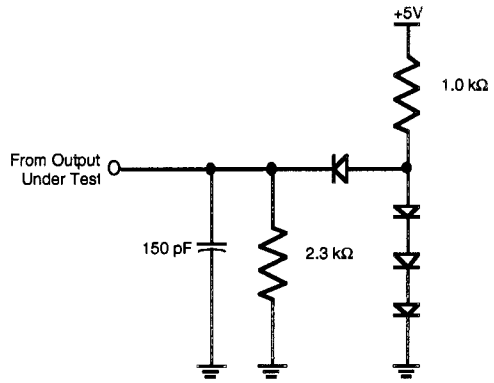


Figure 6. Test Load Diagram

PIN FUNCTIONS

XTAL1, XTAL2 Crystal 1, Crystal 2 (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

/RESET (input, active Low). To avoid asynchronous and noisy reset problems, the Z86E23 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. When /RESET is deactivated, program execution begins at location 000CH. During power up, Reset time must be held low for 50 ms, or until V_{CC} is stable, whichever is longer.

Note: Reset pin has internal pull-up resistor to V_{CC}.

XTAL1, XTAL2 Crystal 1, Crystal 2 (time-based input and output, respectively). These pins connect a parallel-resonant crystal or an external single-phase clock to the on-chip clock oscillator and buffer.

Port 0 (P07-P00). Port 0 is an 8-bit, nibble-programmable, bidirectional, NMOS-compatible I/O port. These eight I/O lines can be configured under software control as a nibble input port, or as a nibble open-drain output port. When used as an I/O port, inputs are standard NMOS and outputs are open-drain (Figure 8).

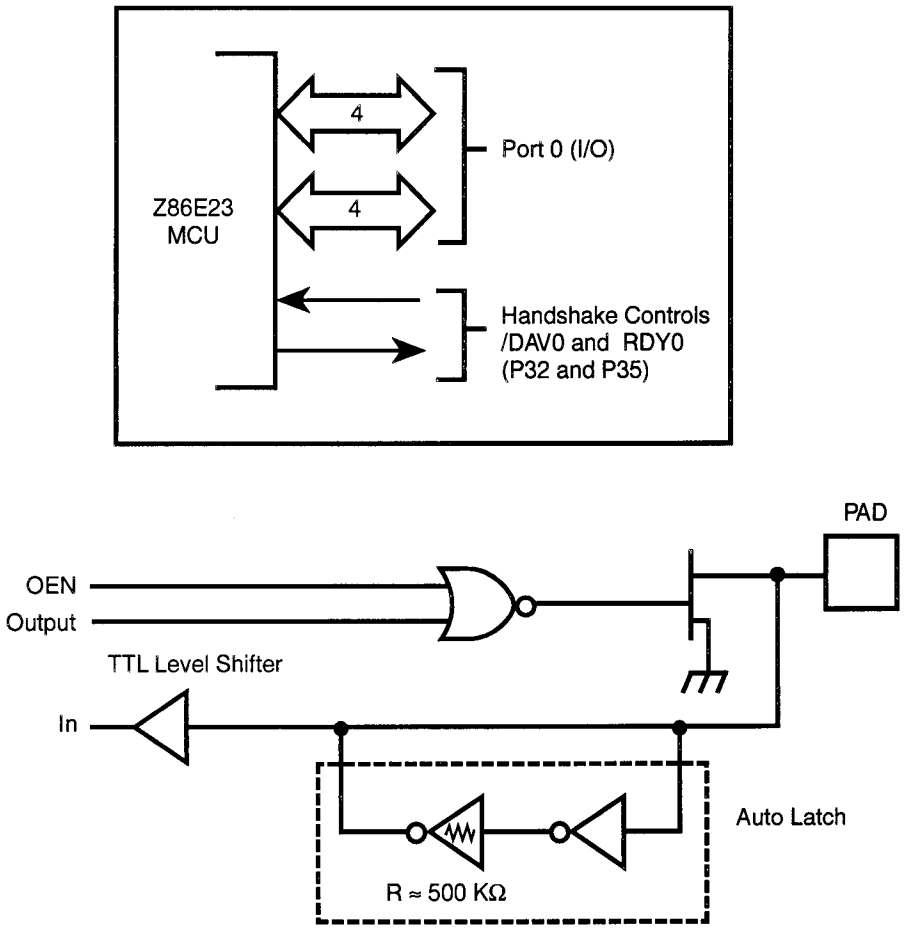


Figure 8. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P17-P10). Port 1 is an 8-bit, byte-programmable, bidirectional, TTL-compatible I/O port. These eight I/O lines are configured under a software control program as a byte input port or as an open-drain output port. When used as an I/O port, inputs are standard TTL and outputs are open-drain (Figure 9).

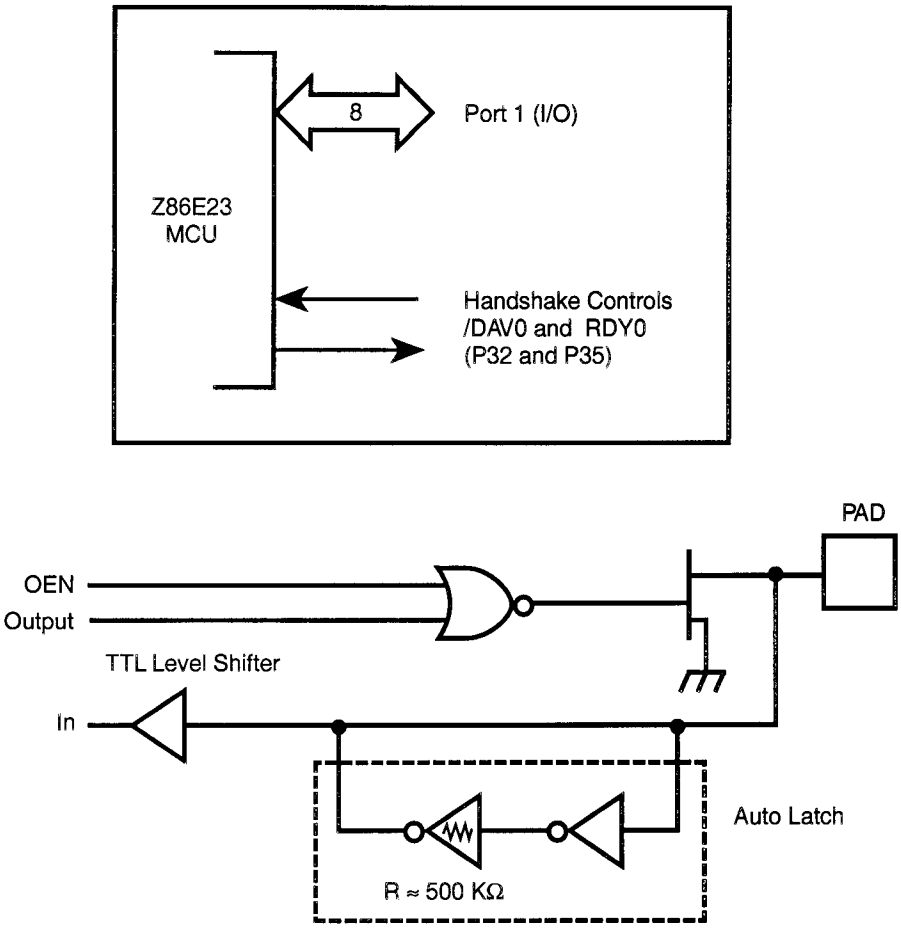


Figure 9. Port 1 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bit-programmable, bi-directional, CMOS-compatible port. Each of these eight I/O lines can be independently programmed as an input or output, or globally as an open-drain output. Port 2 is always available for I/O operation (Figure 10).

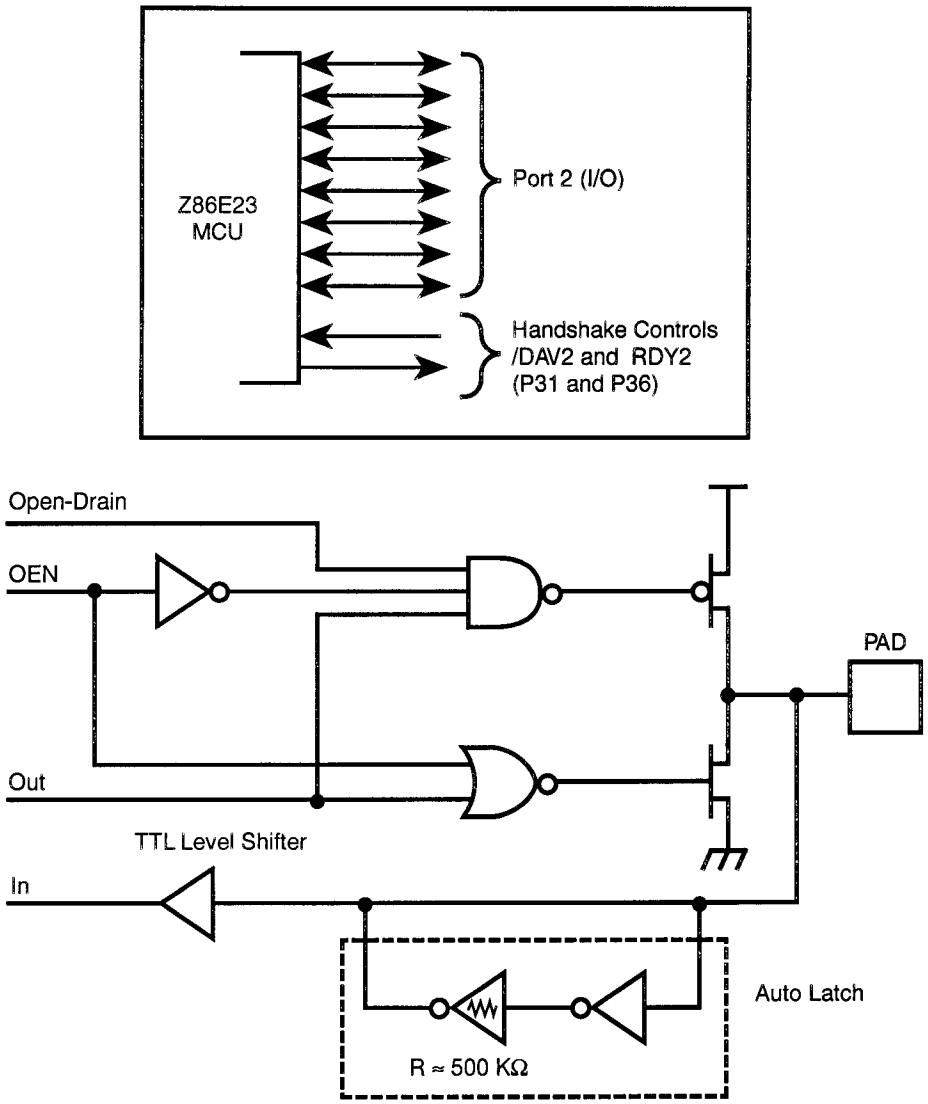


Figure 10. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS-compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33-P30) input and four-fixed (P37-P34) output ports. Port 3 outputs have the capability of driving LEDs directly with a pull-up resistor (output voltage of Port 3 is 0.8V @ 10 mA).

Port 3 is configured under software control to provide the following control functions: four external interrupt request signals (IRQ3-IRQ0); timer input and output signals (T_{IN} and T_{OUT}), and EPROM control signals (P30=/CE, P31=/OE, P32=EPM and P33=GND) in Table 5.

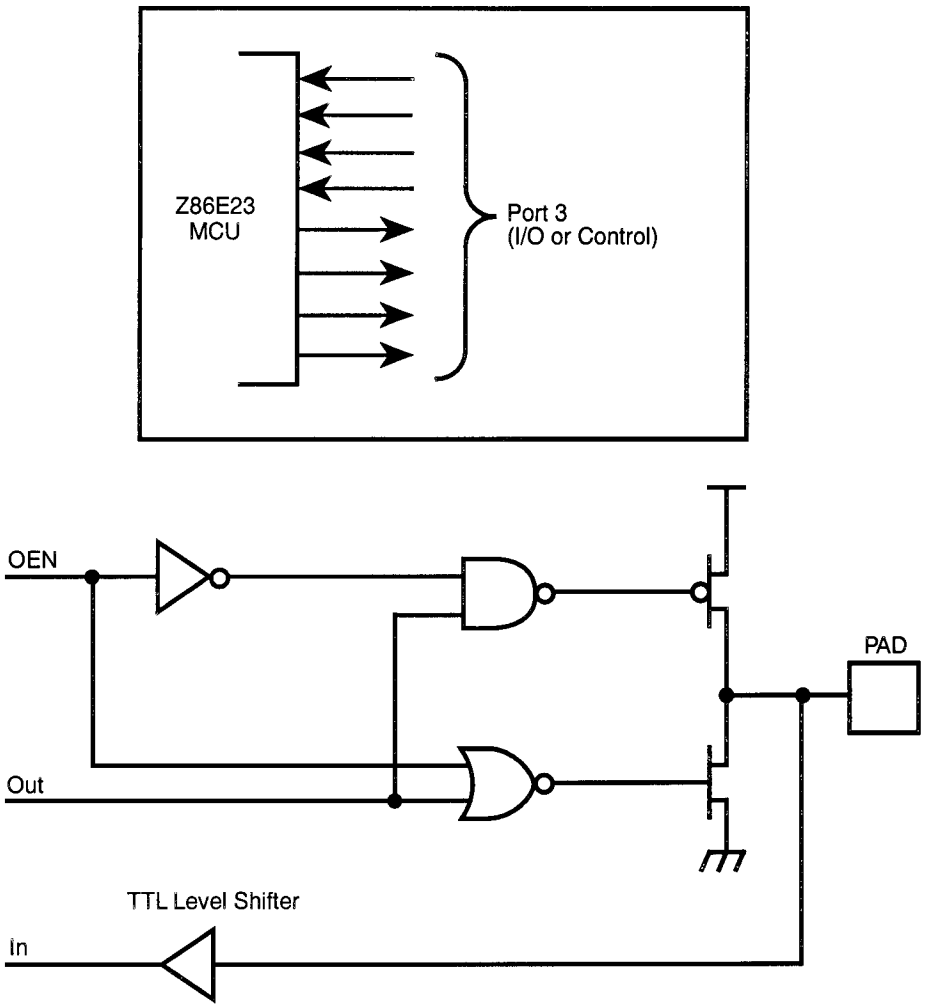


Figure 11. Port 3 Configuration

FUNCTIONAL DESCRIPTION

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 15).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counters and prescalers reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter is programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single-pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36 also serves as a timer output (TOUT) through which T0, T1, or the internal clock can be output. The counter/timers are cascaded by connecting the T0 output to the input of T1.

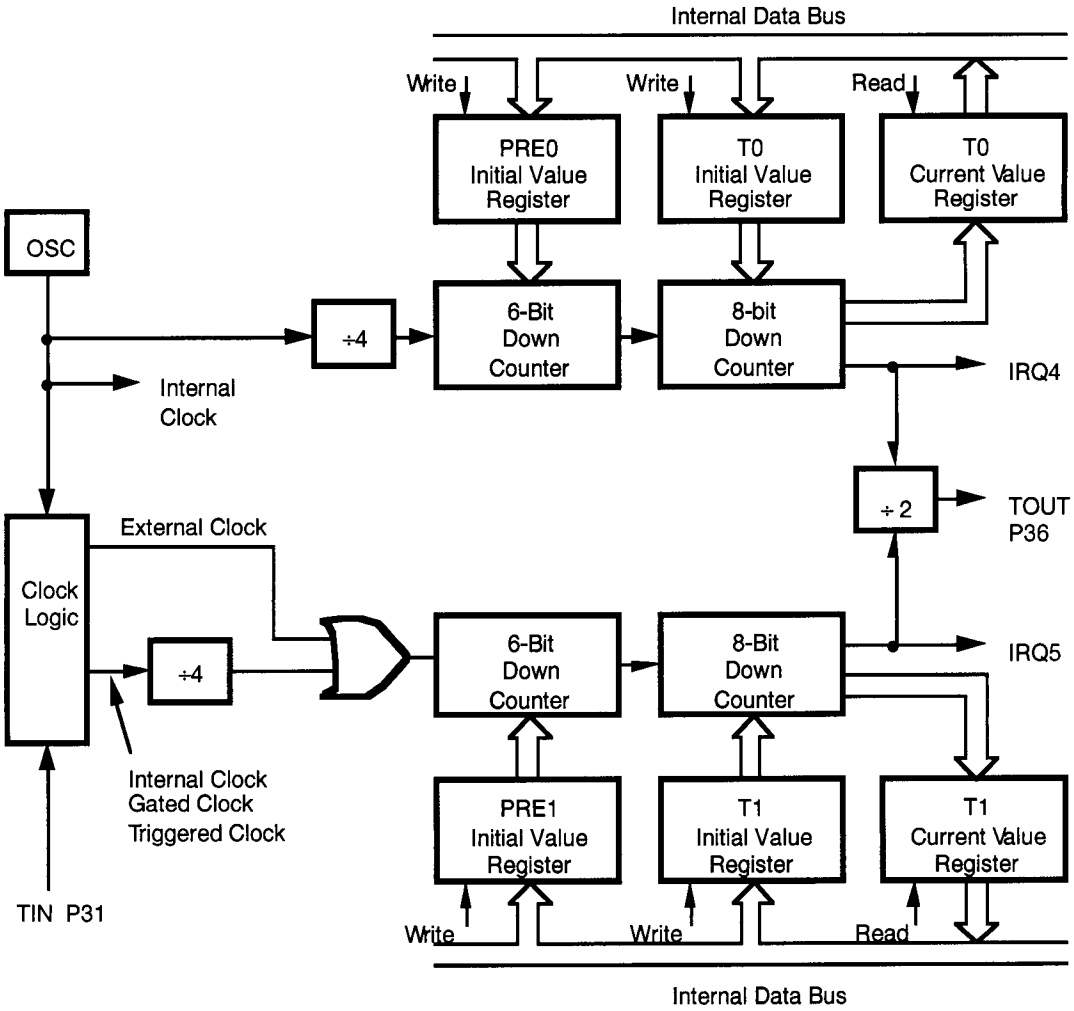


Figure 15. Counter/Timers Block Diagram

Interrupts. The Z86E23 has six different interrupts from six different sources. The interrupts are maskable and prioritized. The six sources are divided as follows; four sources are claimed by Port 3 lines P33-P30, and two by the counter/timers (Figure 16). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register.

All Z86E23 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. This disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initialed interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 2.5 TpC before the falling edge of the last clock cycle of the currently executing instruction.

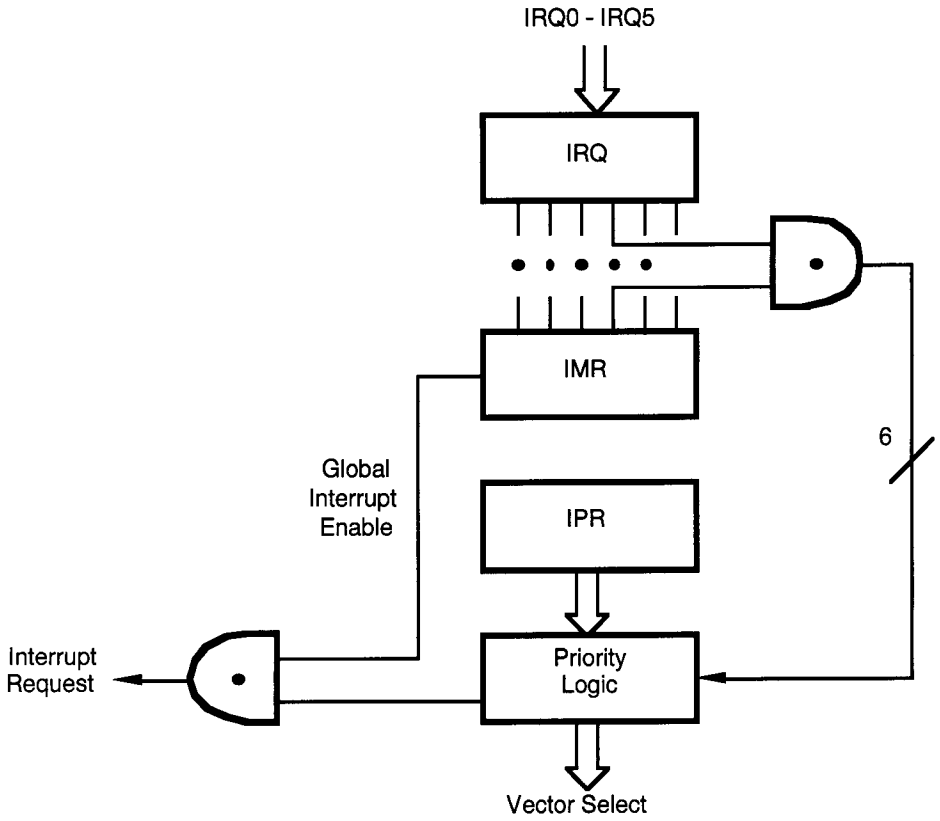


Figure 16. Interrupt Block Diagram

PROGRAMMING

Z86E23 User Modes

The Z86E23 uses separate AC timing cycles for the different User Modes available. Table 7 shows the Z86E23 User Modes. Table 8 shows the timing of the programming waveforms. Port 1 Data Bus requires pull-up resistors for program/verify.

User MODE 1 EPROM Read

The Z86E23 EPROM read cycle is provided so that the user may read the Z86E23 as a standard 2764A EPROM. This is accomplished by driving the /EPM pin (P32) to VH and activating /CE and /OE. /PGM remains inactive. This mode is not valid after execution of an EPROM protect cycle. Timing for the EPROM read cycle is shown in Figure 18.

User MODE 2 EPROM Program

The Z86E23 Program function conforms to the Intelligent programming algorithm. The device is programmed with VCC at 6.0V and VPP = 12.5V. Programming pulses are applied in 1 ms increments to a maximum of 25 pulses before proper verification. After verification, a programming pulse of three times the duration of the cycles necessary to program the device is issued to ensure proper programming. After all addresses are programmed, a final data comparison is executed and the programming cycle is complete. Timing for the Z86E23 programming cycle is shown in Figure 19.

User MODE 3 EPROM Verify

The Program Verify cycle is used as part of the Intelligent programming algorithm to ensure data integrity under worst-case conditions. It differs from the EPROM read cycle in that VPP is active and VCC must be driven to 6.0V. Timing is shown in Figure 19.

User MODES 4 and 5 EPROM and RAM Protect

To extend program security, EPROM and RAM protect cycles are provided for the Z86E23. Execution of the EPROM protect cycle prohibits proper execution of the EPROM Read, EPROM Verify, and EPROM programming cycles. Execution of the RAM protect cycle disables accesses to the upper 128 bytes of register memory (excluding mode and configuration registers), but first the user's program must set bit-6 of the IMR (R251). Timing is shown in Figure 20.

Table 7. EEPROM Rogram Modes

Mode	VPP	EPM	/CE	/OE	/PGM	VCC*	ADDR	Data
EPROM Read1	X	V_H	VIL	V_{IL}	V_{IH}	4.5	ADDR	OUT
EPROM Read2	X	V_H	VIL	V_{IL}	V_{IH}	5.5	ADDR	OUT
Program	V_H	X	VIL	V_{IH}	V_{IL}	6.0	ADDR	IN
Program Verify	V_H	X	VIL	V_{IL}	V_{IH}	6.0	ADDR	OUT
EPROM Protect Select	V_H	V_H	VH	V_{IH}	V_{IL}	6.0	NU	NU
RAM Protect	V_H	V_{IH}	VH	V_H	V_{IL}	6.0	NU	NU

Notes:

* Tolerance is ±0.25V

V_H = 12.5 ±0.5V

V_{IH} = As per DC specification.

V_{IL} = As per DC specification.

X = Not used, but must be set to either VH, VIH or VIL level.

NU = Not used, but must be set to either VIH or VIL.

I_{PP} during programming = 40 mA maximum.

I_{CC} during either programming, verify, or read = 40 mA maximum.

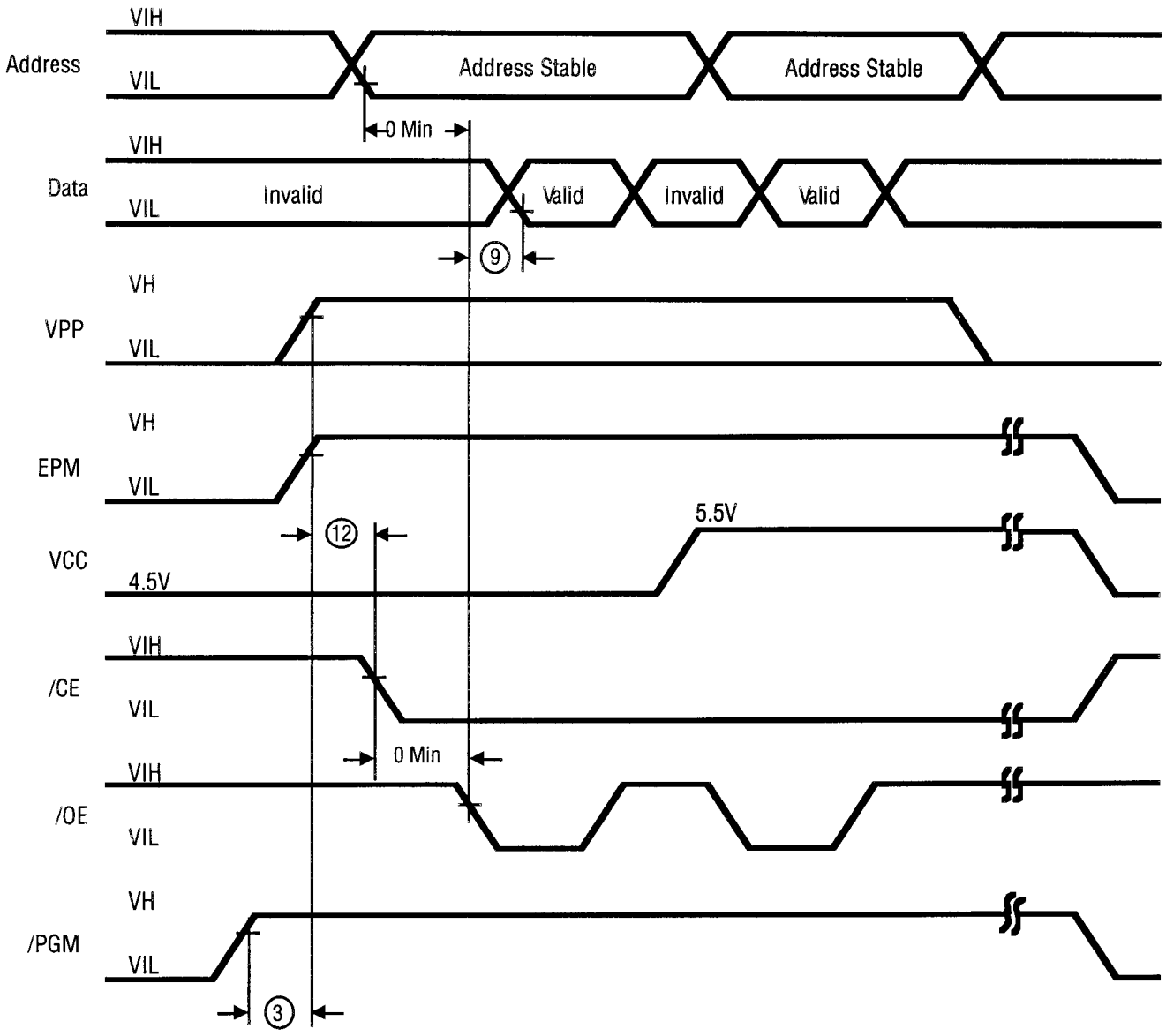


Figure 18. EPROM Read

PROGRAMMING (Continued)

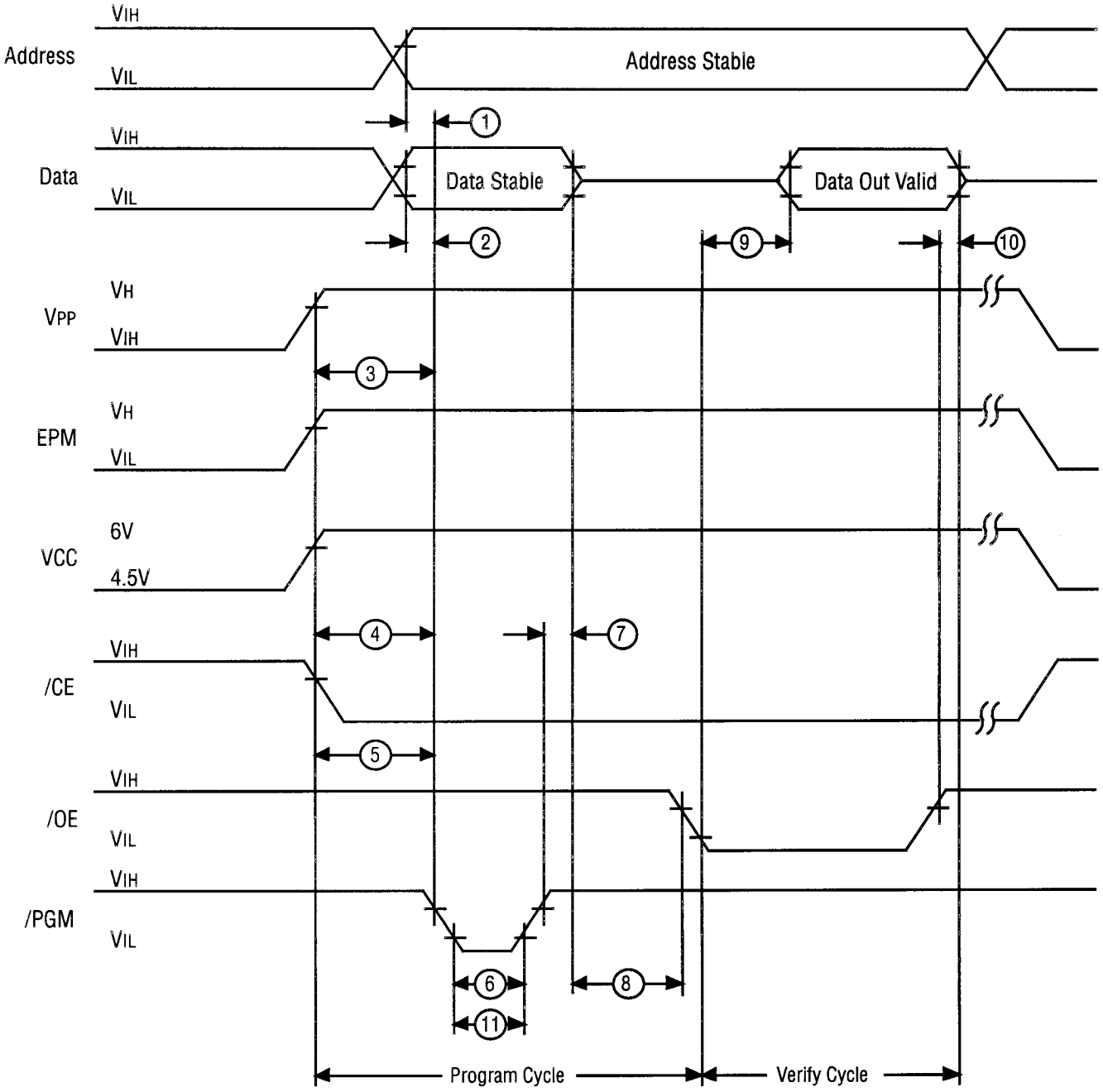


Figure 19. EPROM Program and Verify

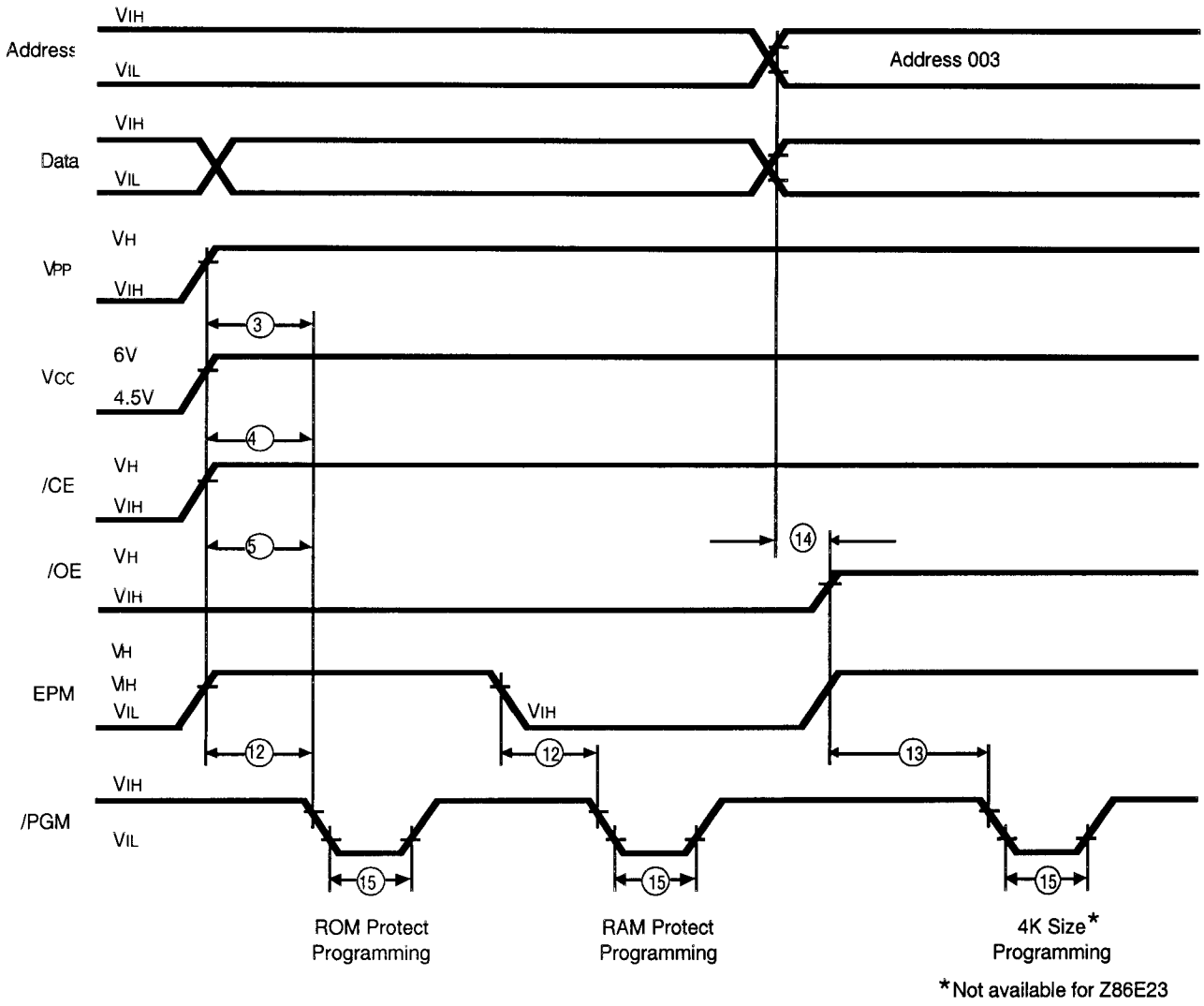


Figure 20. EPROM and RAM Protect and 4K Size Selection

PROGRAMMING (Continued)

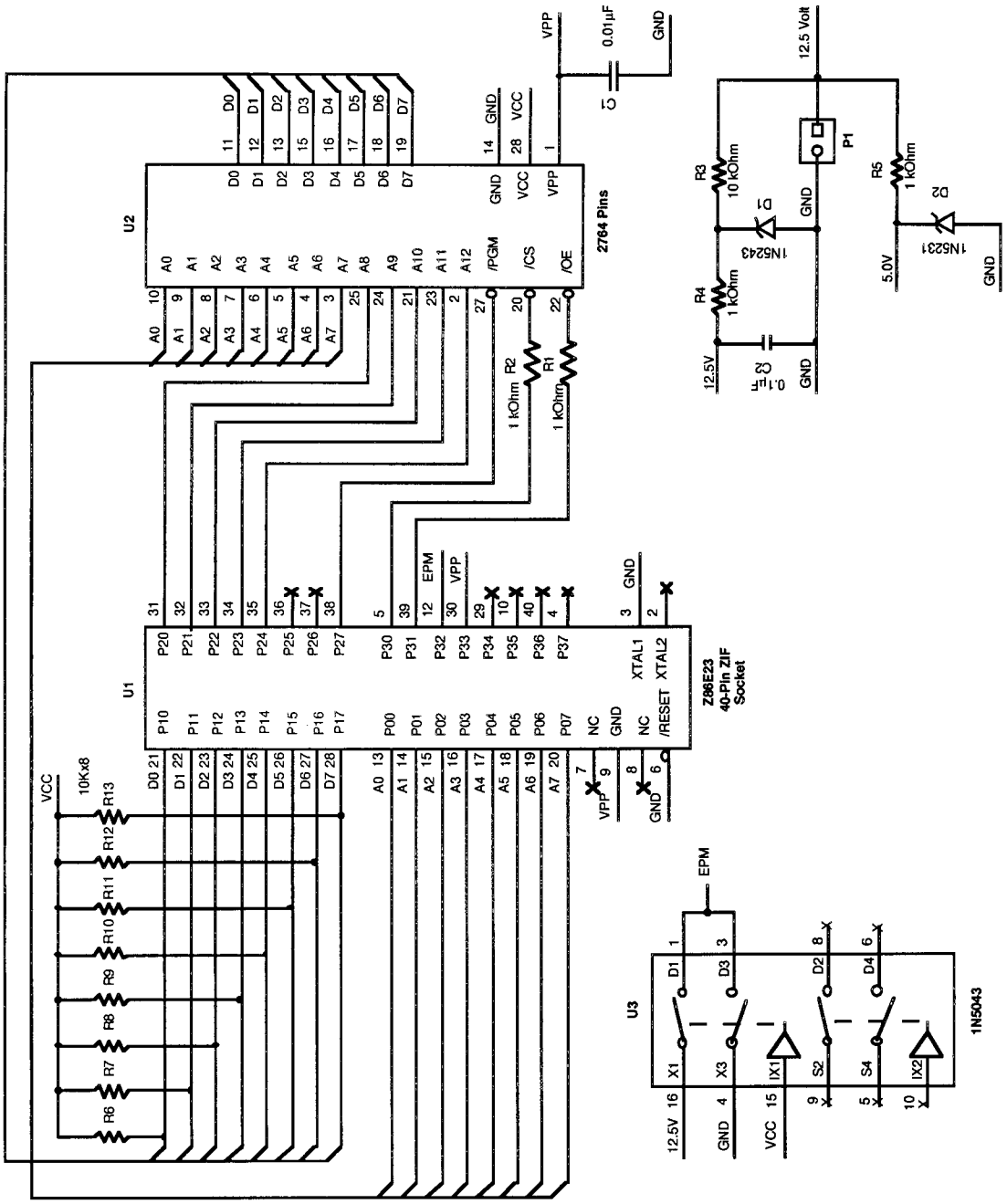


Figure 21. Z86E23 Z8 OTP Programming Adapter

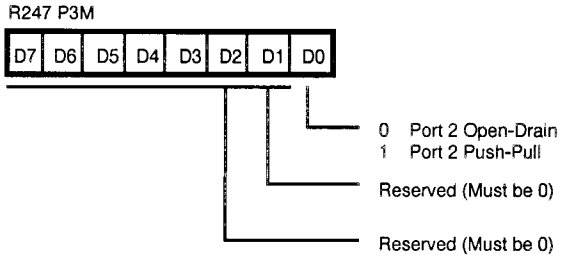


Figure 30. Port 0 and 1 Mode Register (F8H: Write Only)

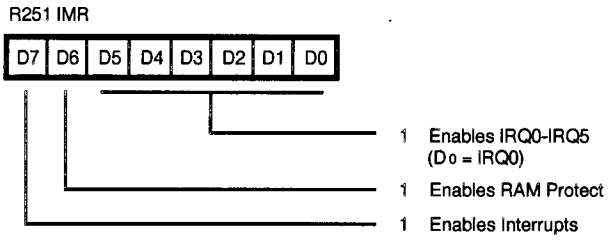


Figure 33. Interrupt Mask Register (FBH: Read/Write)

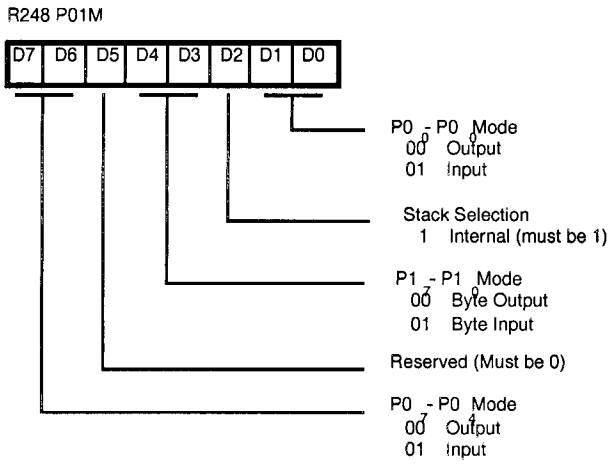


Figure 31. Interrupt Priority Register (F9H: Write Only)

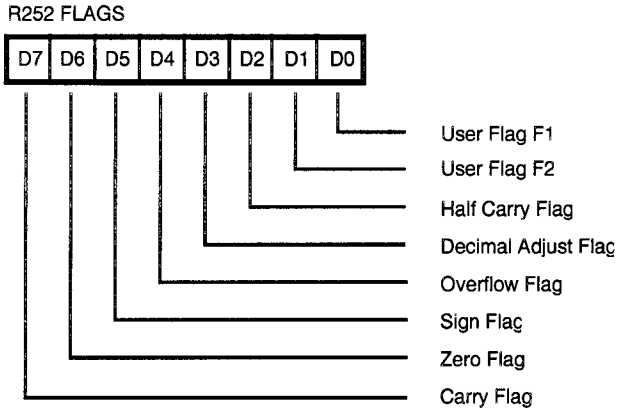


Figure 34. Flag Register (FCH: Read/Write)

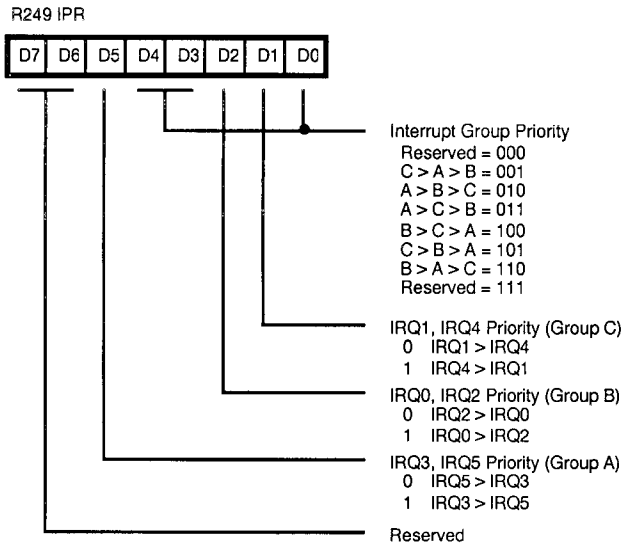


Figure 32. Interrupt Request Register (FAH: Read/Write)

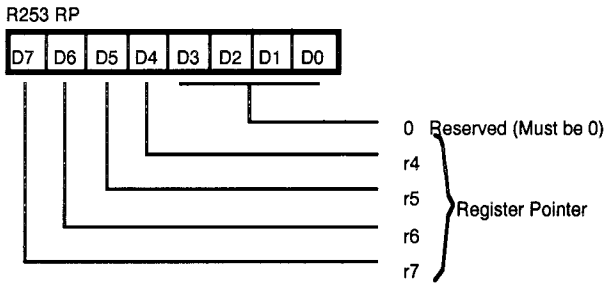


Figure 35. Register Pointer Register (FDH: Read/Write)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

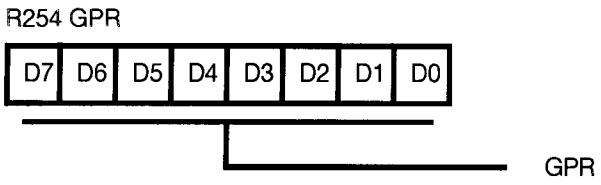


Figure 36. General Purpose Register (FEH: Read/Write)

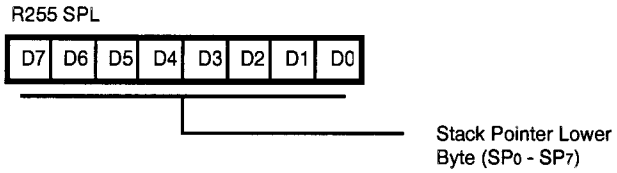
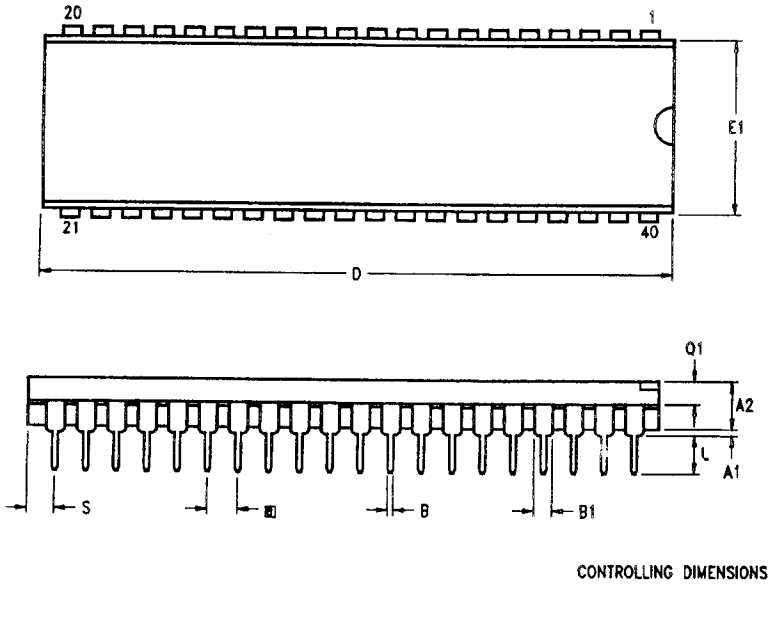


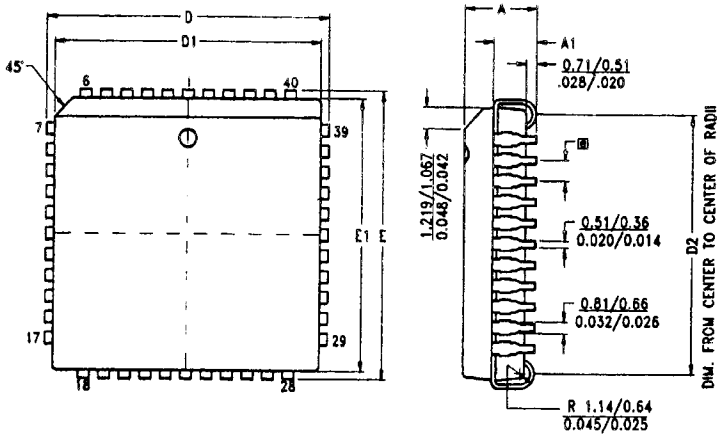
Figure 37. Stack Pointer Register (FFH: Read/Write)

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

Figure 38. 40-Lead DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 TYP		0.050 TYP	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM / INCH

Figure 39. 44-Lead PLCC Package Diagram

ORDERING INFORMATION

Z86E23

4 MHz

40-Pin DIP	44-Pin PLCC
Z86E2304PSC	Z86E2304VSC

For fast results, contact your Zilog sales office for assistance in ordering the part desired.

Package
P = Plastic DIP
V = Plastic Chip Carrier

Temperature
S = 0°C to +70°C

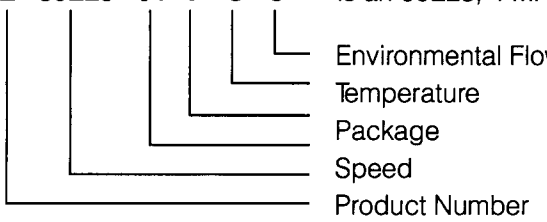
Speed
4 = 4 MHz

Environmental
C = Plastic Standard

Example:

Example:

Z 86E23 04 P S C is an 86E23, 4 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



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