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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFl

Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	96КВ (96К × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-54
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe161fl12f80vaafxuma1

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Functional Description

		, , ,	,	
Address Area	Start Loc.	End Loc.	Area Size ²⁾	Notes
ESFR area	00'F000 _H	00'F1FF _H	0.5 Kbytes	
XSFR area	00'E000 _H	00'EFFF _H	4 Kbytes	
Data SRAM (DSRAM)	00'C800 _H	00'DFFF _H	6 Kbytes	
Reserved for DSRAM	00'8000 _H	00'C7FF _H	18 Kbytes	
External memory area	00'000 _H	00'7FFF _H	32 Kbytes	

Table 8XE161xL Memory Map (cont'd)¹⁾ (cont'd)

 Accesses to the shaded areas are reserved. In devices with external bus interface these accesses generate external bus accesses.

2) The areas marked with "<" are slightly smaller than indicated, see column "Notes".

3) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

4) Several pipeline optimizations are not active within the external IO area.

This common memory space consists of 16 Mbytes organized as 256 segments of 64 Kbytes; each segment contains four data pages of 16 Kbytes. The entire memory space can be accessed bytewise or wordwise. Portions of the on-chip DPRAM and the register spaces (ESFR/SFR) additionally are directly bit addressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls access to the program memories such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls access to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected to the high-speed system bus so that they can exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources. These include peripherals on the LXBus such as USIC or MultiCAN. The system bus allows concurrent two-way communication for maximum transfer performance.

4 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is optimized for code fetches. A section of the PSRAM with programmable size can be write-protected.



Functional Description

3.2 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instructionfetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.



Figure 4 CPU Block Diagram



Functional Description

3.3 Memory Protection Unit (MPU)

The XE161xL's Memory Protection Unit (MPU) protects user-specified memory areas from unauthorized read, write, or instruction fetch accesses. The MPU can protect the whole address space including the peripheral area. This completes established mechanisms such as the register security mechanism or stack overrun/underrun detection.

Four Protection Levels support flexible system programming where operating system, low level drivers, and applications run on separate levels. Each protection level permits different access restrictions for instructions and/or data.

Every access is checked (if the MPU is enabled) and an access violating the permission rules will be marked as invalid and leads to a protection trap.

A set of protection registers for each protection level specifies the address ranges and the access permissions. Applications requiring more than 4 protection levels can dynamically re-program the protection registers.

3.4 Memory Checker Module (MCHK)

The XE161xL's Memory Checker Module calculates a checksum (fractional polynomial division) on a block of data, often called Cyclic Redundancy Code (CRC). It is based on a 32-bit linear feedback shift register and may, therefore, also be used to generate pseudo-random numbers.

The Memory Checker Module is a 16-bit parallel input signature compression circuitry which enables error detection within a block of data stored in memory, registers, or communicated e.g. via serial communication lines. It reduces the probability of error masking due to repeated error patterns by calculating the signature of blocks of data.

The polynomial used for operation is configurable, so most of the commonly used polynomials may be used. Also, the block size for generating a CRC result is configurable via a local counter. An interrupt may be generated if testing the current data block reveals an error.

An autonomous CRC compare circuitry is included to enable redundant error detection, e.g. to enable higher safety integrity levels.

The Memory Checker Module provides enhanced fault detection (beyond parity or ECC) for data and instructions in volatile and non volatile memories. This is especially important for the safety and reliability of embedded systems.



Functional Description



Figure 5 CAPCOM Unit Block Diagram



Functional Description



Figure 6 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.



Functional Description

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

Table 11 Instruction Set Summary (cont'd)

1) The Enter Power Down Mode instruction is not used in the XE161xL, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.



4.1.1 Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XE161xL. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Note: Typical parameter values refer to room temperature and nominal supply voltage, minimum/maximum parameter values also include conditions of minimum/maximum temperature and minimum/maximum supply voltage. Additional details are described where applicable.

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Voltage Regulator Buffer Capacitance for DMP_M	$C_{\rm EVRM}$ SR	1.0	-	4.7	μF	1)2)
External Load Capacitance	$C_{L} \operatorname{SR}$	-	20 ³⁾	-	pF	pin out driver= default 4)
System frequency	$f_{\rm SYS}{ m SR}$	-	-	80	MHz	5)
Overload current for analog inputs ⁶⁾	$I_{\rm OVA}{ m SR}$	-2	-	5	mA	not subject to production test
Overload current for digital inputs ⁶⁾	$I_{\rm OVD}{\rm SR}$	-5	_	5	mA	not subject to production test
Overload current coupling factor for analog inputs ⁷)	K _{OVA} CC	-	2.5 x 10 ⁻⁴	1.5 x 10 ⁻³	-	<i>I</i> _{OV} < 0 mA; not subject to production test
		_	1.0 x 10 ⁻⁶	1.0 x 10 ⁻⁴	-	<i>I</i> _{OV} > 0 mA; not subject to production test

Table 13 Operating Conditions

Electrical Parameters

Parameter	Symbol		Values	5	Unit	Note /
		Min.	Тур.	Max.		Test Condition
Input high voltage (all except XTAL1)	$V_{IH}SR$	$0.7 ext{ x}$ $V_{ ext{DDP}}$	-	V _{DDP} + 0.3	V	
Input low voltage (all except XTAL1)	$V_{IL} \operatorname{SR}$	-0.3	-	0.3 x V_{DDP}	V	
Output High voltage ⁶⁾	V _{OH} CC	V _{DDP} - 1.0	-	-	V	$I_{\text{OH}} \ge I_{\text{OHmax}}$
		V _{DDP} - 0.4	-	-	V	$I_{\text{OH}} \ge I_{\text{OHnom}}^{7}$
Output Low Voltage ⁶⁾	V _{OL} CC	-	-	0.4	V	$I_{\rm OL} \le I_{\rm OLnom}^{8)}$
		-	-	1.0	V	$I_{OL} \leq I_{OLmax}$

Table 17 DC Characteristics for Lower Voltage Range (cont'd)

 Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

- 2) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{\rm IN} < V_{\rm SS}$) or supply ripple ($V_{\rm IN} > V_{\rm DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current ($I_{\rm INJ}$) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor $K_{\rm OV}$.
- 3) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature (*T*_J = junction temperature [°C]): *I*_{OZ} = 0.05 x e^(1.5 + 0.028 x TJ-) [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = *V*_{DDP} *V*_{PIN} [V]): *I*_{OZ} = *I*_{OZtempmax} (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.
- Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device.
- 5) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level.
- 6) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.
- As a rule, with decreasing output current the output levels approach the respective supply level (VOL->VSS, VOH->VDDP). However, only the levels for nominal output currents are verified.
- 8) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL} -> V_{SS} , V_{OH} -> V_{DDP}). However, only the levels for nominal output currents are verified.



4.6 Flash Memory Parameters

The XE161xL is delivered with all Flash sectors erased and with no protection installed. The data retention time of the XE161xL's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Parameter	Symbol		Values	5	Unit	Note /
		Min.	Тур.	Max.		Test Condition
Parallel Flash module	$N_{\rm PP}{\rm SR}$	-	-	2 ¹⁾		$N_{\rm FL_RD} \leq 1$
program/erase limit depending on Flash read activity		_	-	1 ²⁾		N _{FL_RD} > 1
Flash erase endurance for security pages	$N_{\rm SEC}{ m SR}$	10	-	-	cycle s	$t_{RET} \ge 20$ years
Flash wait states ³⁾	N _{WSFLASH} SR	1	-	-		f _{SYS} ≤ 8 MHz
		2	-	-		$f_{\rm SYS} \le 13 \ \rm MHz$
		3	-	-		$f_{\rm SYS}$ \leq 17 MHz
		4	-	-		$f_{\rm SYS}$ > 17 MHz
Erase time per sector/page	t _{ER} CC	_	7 ⁴⁾	8.0	ms	
Programming time per page	t _{PR} CC	-	34)	3.5	ms	
Data retention time	t _{RET} CC	20	-	-	year s	$N_{\rm ER} \le$ 1,000 cycl es
Drain disturb limit	$N_{\rm DD}{ m SR}$	32	-	-	cycle s	

Table 27 Flash Parameters



4.7 AC Parameters

These parameters describe the dynamic behavior of the XE161xL.

4.7.1 Testing Waveforms

These values are used for characterization and production testing (except pin XTAL1).



Figure 16 Input Output Waveforms







Parameter	Symbol		Values	S	Unit	Note /
		Min.	Тур.	Max.		Test Condition
VCO output frequency	f _{vco} CC	50	-	110	MHz	VCOSEL= 00 _B ; VCOmode= controlled
		10	-	40	MHz	VCOSEL= 00 _B ; VCOmode= free running
		100	-	160	MHz	VCOSEL= 01 _B ; VCOmode= controlled
		20	-	80	MHz	VCOSEL= 01 _B ; VCOmode= free running

Table 28 System PLL Parameters

4.7.2.2 Wakeup Clock

When wakeup operation is selected (SYSCON0.CLKSEL = 00_B), the system clock is derived from the low-frequency wakeup clock source:

 $f_{SYS} = f_{WU}$.

In this mode, a basic functionality can be maintained without requiring an external clock source and while minimizing the power consumption.

4.7.2.3 Selecting and Changing the Operating Frequency

When selecting a clock source and the clock generation method, the required parameters must be carefully written to the respective bit fields, to avoid unintended intermediate states.

Many applications change the frequency of the system clock (f_{SYS}) during operation in order to optimize system performance and power consumption. Changing the operating frequency also changes the switching currents, which influences the power supply.

To ensure proper operation of the on-chip EVRs while they generate the core voltage, the operating frequency shall only be changed in certain steps. This prevents overshoots and undershoots of the supply voltage.

To avoid the indicated problems, recommended sequences are provided which ensure the intended operation of the clock system interacting with the power system. Please refer to the Programmer's Guide.



- 2) Overload conditions must not occur on pin XTAL1.
- Note: For crystal/resonator operation, it is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for oscillator operation. The manufacturers of crystals and ceramic resonators offer an oscillator evaluation service. This evaluation checks the crystal/resonator specification limits to ensure a reliable oscillatior operation.



Figure 20 External Clock Drive XTAL1



Electrical Parameters

Table 31	Standard Pad P	Parameters for Lower	Voltage Range	(cont'd)
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Parameter	Symbol	Values			Unit	Note /												
		Min.	Тур.	Max.		Test Condition												
Nominal output driver current (absolute value)	I _{Onom} CC	-	-	0.8	mA	Driver_Strength = Medium												
		-	-	1.0	mA	Driver_Strength = Strong												
		-	-	0.15	mA	Driver_Strength = Weak												
Rise and Fall times (10% - 90%)	t _{RF} CC	-	_	73 + 0.85 x C _L	ns	$C_{L} \ge 20 \text{ pF};$ $C_{L} \le 100 \text{ pF};$ Driver_Strength = Medium												
		-	-	6+0.6 x C _L	ns	$C_{L} \ge 20 \text{ pF};$ $C_{L} \le 100 \text{ pF};$ Driver_Strength = Strong; Driver_Edge= Soft												
																-	-	33 + 0.6 x C _L
		-	-	385 + 3.25 x C _L	ns	$C_{L} \ge 20 \text{ pF};$ $C_{L} \le 100 \text{ pF};$ Driver_Strength = Weak												

 The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and Σ-I_{OH}) must remain below 25 mA.



Electrical Parameters



Figure 23 DAP Timing Host to Device



Figure 24 DAP Timing Device to Host

Note: The transmission timing is determined by the receiving debugger by evaluating the sync-request synchronization pattern telegram.



Debug via JTAG

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 38 is valid under the following conditions: $C_1 = 20 \text{ pF}$; voltage_range= upper

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
TCK clock period	t ₁ SR	100 ¹⁾	_	_	ns	2)
TCK high time	t_2 SR	16	-	-	ns	
TCK low time	t ₃ SR	16	-	-	ns	
TCK clock rise time	t ₄ SR	-	-	8	ns	
TCK clock fall time	t ₅ SR	-	-	8	ns	
TDI/TMS setup to TCK rising edge	t ₆ SR	6	-	-	ns	
TDI/TMS hold after TCK rising edge	t ₇ SR	6	-	-	ns	
TDO valid from TCK falling edge (propagation delay) ³⁾	t ₈ CC	-	29	32	ns	
TDO high impedance to valid output from TCK falling edge ⁴⁾³⁾	t ₉ CC	-	29	32	ns	
TDO valid output to high impedance from TCK falling edge ³⁾	<i>t</i> ₁₀ CC	-	29	32	ns	
TDO hold after TCK falling edge ³⁾	<i>t</i> ₁₈ CC	5	_	_	ns	

Table 38 JTAG Interface Timing for Upper Voltage Range

1) The debug interface cannot operate faster than the overall system, therefore $t_1 \ge t_{SYS}$.

2) Under typical conditions, the JTAG interface can operate at transfer rates up to 10 MHz.

3) The falling edge on TCK is used to generate the TDO timing.

4) The setup time for TDO is given implicitly by the TCK cycle time.













Debug via SPD

The SPD interface will work with standard SPD tools having a sample/output clock frequency deviation of +/- 5% or less.

Note: For further details please refer to application note AP24004 in section SPD Timing Requirements.

Note: Operating Conditions apply.



Package and Reliability

particular, the size of the Exposed Pad (if present) may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

Package Outlines



Figure 27 PG-VQFN-48-54 (Plastic Green Thin Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page "Packages": http://www.infineon.com/packages



Package and Reliability

5.2 Thermal Considerations

When operating the XE161xL in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The "Thermal resistance $R_{\Theta JA}$ " quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta,IA}$

The internal power consumption is defined as

 $P_{\text{INT}} = V_{\text{DDP}} \times I_{\text{DDP}}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as $P_{\text{IOSTAT}} = \Sigma((V_{\text{DDP}} - V_{\text{OH}}) \times I_{\text{OH}}) + \Sigma(V_{\text{OL}} \times I_{\text{OL}})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP} , if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- · Reduce the load on active output drivers

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