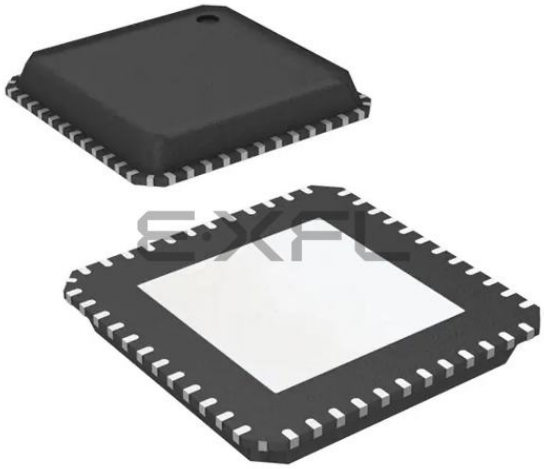
Infineon Technologies - XE161FL20F80VAAFXUMA1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-54
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe161fl20f80vaafxuma1

Table of Contents

- On-Chip Peripheral Modules
  - Synchronizable 12-bit A/D Converter with up to 10 channels, conversion time below 1 µs, optional data preprocessing (data reduction, range check), broken wire detection
  - 16-channel general purpose capture/compare unit (CC2)
  - Two capture/compare units for flexible PWM signal generation (CCU6x)
  - Multi-functional general purpose timer unit with 5 timers
  - Up to 4 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI/QSPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
  - On-chip MultiCAN interface (Rev. 2.0B active) with up to 32 message objects (Full CAN/Basic CAN) on 2 CAN nodes and gateway functionality
  - On-chip system timer and on-chip real time clock
- Single power supply from 3.0 V to 5.5 V
- Power reduction and wake-up modes with flexible power management
- Programmable window watchdog timer and oscillator watchdog
- Up to 33 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via Device Access Port (DAP), Single-Pin DAP (SPD) or JTAG interface
- 48-pin Green VQFN package, 0.5 mm (10.7 mil) pitch

Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the function set of the corresponding product type
- the temperature range[1)]:
  - SAF-…: -40°C to 85°C
  - SAK-…: -40°C to 125°C
- the package and the type of delivery.

For ordering codes for the XE161xL please contact your sales representative or local distributor.

1) Not all derivatives are offered in all temperature ranges.

1.2 Definition of Feature Variants

The XE161xL types are offered with several Flash memory sizes. **Table 3** and **Table 4** describe the location of the available Flash memory.

Table 3 Continuous Flash Memory Ranges

Total Flash Size	1st Range[1)]	2nd Range	3rd Range
160 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C2'0FFF_H$	$C4'0000_H$ … $C4'7FFF_H$
96 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C1'0FFF_H$	$C4'0000_H$ … $C4'7FFF_H$

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

Table 4 Flash Memory Module Allocation (in Kbytes)

Total Flash Size	Flash 0[1)]	Flash 1
160	128	32
96	64	32

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

The XE161xL types are offered with different interface options. **Table 5** lists the available channels for each option.

Table 5 Interface Channel Association

Total Number	Available Channels / Message Objects
10 ADC0 channels	CH0, CH2, CH3, CH4, CH8, CH9, CH16, CH17, CH19, CH20
2 CAN nodes	CAN0, CAN1 32 message objects
4 serial channels	U0C0, U0C1, U1C0, U1C1

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
13	P5.4	I	In/B	**Bit 4 of Port 5, General Purpose Input**
	ADC0_CH4	I	In/B	**Analog Input Channel 4 for ADC0**
	CCU63_T12HRB	I	In/B	**External Run Control Input for T12 of CCU63**
	T3EUDA	I	In/B	**GPT12E Timer T3 External Up/Down Control Input**
	TMS_A	I	In/B	**JTAG Test Mode Selection Input**
14	P5.8	I	In/B	**Bit 8 of Port 5, General Purpose Input**
	ADC0_CH8	I	In/B	**Analog Input Channel 8 for ADC0**
	CCU6x_T12HRC	I	In/B	**External Run Control Input for T12 of CCU60/3**
	CCU6x_T13HRC	I	In/B	**External Run Control Input for T13 of CCU60/3**
15	P5.9	I	In/B	**Bit 9 of Port 5, General Purpose Input**
	ADC0_CH9	I	In/B	**Analog Input Channel 9 for ADC0**
	CC2_T7IN	I	In/B	**CAPCOM2 Timer T7 Count Input**
16	P2.0	O0 / I	DA/B	**Bit 0 of Port 2, General Purpose Input/Output**
	CCU63_CC60	O2	DA/B	**CCU63 Channel 0 Output**
	RxDC0C	I	DA/B	**CAN Node 0 Receive Data Input**
	CCU63_CC60INB	I	DA/B	**CCU63 Channel 0 Input**
	ADC0_CH19	I	DA/B	**Analog Input Channel 19 for ADC0**
	T5INB	I	DA/B	**GPT12E Timer T5 Count/Gate Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
40	P10.9	O0 / I	St/B	**Bit 9 of Port 10, General Purpose Input/Output**
	U0C0_SELO 4	O1	St/B	**USIC0 Channel 0 Select/Control 4 Output**
	U0C1_MCLK OUT	O2	St/B	**USIC0 Channel 1 Master Clock Output**
	TxDC1	O3	St/B	**CAN Node 1 Transmit Data Output**
	CCU60_CCP OS2A	I	St/B	**CCU60 Position Input 2**
	TCK_B	I	St/B	**DAP0/JTAG Clock Input**
	T3INB	I	St/B	**GPT12E Timer T3 Count/Gate Input**
44	P10.10	O0 / I	St/B	**Bit 10 of Port 10, General Purpose Input/Output**
	U0C0_SELO 0	O1	St/B	**USIC0 Channel 0 Select/Control 0 Output**
	CCU60_COU T63	O2	St/B	**CCU60 Channel 3 Output**
	U1C0_DOUT	O3	St/B	**USIC1 Channel 0 Shift Data Output**
	U0C0_DX2C	I	St/B	**USIC0 Channel 0 Shift Control Input**
	TDI_B	I	St/B	**JTAG Test Data Input**
	U0C1_DX1A	I	St/B	**USIC0 Channel 1 Shift Clock Input**
45	P10.12	O0 / I	St/B	**Bit 12 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	U0C0_DOUT	O2	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU63_COU T62	O3	St/B	**CCU63 Channel 2 Output**
	TDO_A	OH	St/B	**DAP1/JTAG Test Data Output**
	SPD_0	I/OH	St/B	**SPD Input/Output**
	C0	I	St/B	**Configuration Pin 0**
	U0C0_DX0D	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U1C0_DX0C	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX1E	I	St/B	**USIC1 Channel 0 Shift Clock Input**
46	XTAL2	O	Sp/M	**Crystal Oscillator Amplifier Output**

3.7 Capture/Compare Unit (CC2)

The CAPCOM unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of one system clock cycle (eight cycles in staggered mode). The CAPCOM unit is typically used to handle high-speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), digital to analog (D/A) conversion, software timing, or time recording with respect to external events.

Two 16-bit timers with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, external count inputs allow event scheduling for the capture/compare registers relative to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer and programmed for capture or compare function.
All registers have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

Table 9 Compare Modes

Compare Modes	Function
Mode 0	Interrupt-only compare mode; Several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; Several compare events per timer period are possible

When clocked by f_{SYS} = 80 MHz, time intervals between 12.5 ns and 13.4 s can be monitored.

When clocked by f_{WU} = 500 kHz, time intervals between 2.0 µs and 2147.5 s can be monitored.

The default Watchdog Timer interval after power-up is 0.13 s (@ f_{WU} = 500 kHz).

3.16 Clock Generation

The Clock Generation Unit can generate the system clock signal f_{SYS} for the XE161xL from a number of external or internal clock sources:

- External clock signals with pad voltage or core voltage levels
- External crystal or resonator using the on-chip oscillator
- On-chip clock source for operation without crystal/resonator
- Wake-up clock (ultra-low-power) to further reduce power consumption

The programmable on-chip PLL with multiple prescalers generates a clock signal for maximum system performance from standard crystals, a clock input signal, or from the on-chip clock source. See also **Section 4.7.2**.

The Oscillator Watchdog (OWD) generates an interrupt if the crystal oscillator frequency falls below a certain limit or stops completely. In this case, the system can be supplied with an emergency clock to enable operation even after an external clock failure.

All available clock signals can be output on the EXTCLK pin.

3.19 Instruction Set Summary

Table 11 lists the instructions of the XE161xL.
The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **"Instruction Set Manual"**.

This document also provides a detailed description of each instruction.

Table 11 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

4.1.1 Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XE161xL. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Note: Typical parameter values refer to room temperature and nominal supply voltage, minimum/maximum parameter values also include conditions of minimum/maximum temperature and minimum/maximum supply voltage. Additional details are described where applicable.

Table 13 Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage Regulator Buffer Capacitance for DMP_M	C_{EVRM} SR	1.0	–	4.7	µF	[1)2)]
External Load Capacitance	C_L SR	–	20[3)]	–	pF	pin out driver= default [4)]
System frequency	f_{SYS} SR	–	–	80	MHz	[5)]
Overload current for analog inputs[6)]	I_{OVA} SR	-2	–	5	mA	not subject to production test
Overload current for digital inputs[6)]	I_{OVD} SR	-5	–	5	mA	not subject to production test
Overload current coupling factor for analog inputs[7)]	K_{OVA} CC	–	2.5×10^{-4}	1.5×10^{-3}	-	I_{OV}< 0 mA; not subject to production test
		–	1.0×10^{-6}	1.0×10^{-4}	-	I_{OV}> 0 mA; not subject to production test

Table 22 ADC Parameters for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Wakeup time from analog powerdown, fast mode	t_{WAF} CC	–	–	8.5	µs	
Wakeup time from analog powerdown, slow mode	t_{WAS} CC	–	–	15.0	µs	

1) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation.
2) The sum of DNL/INL/GAIN/OFF errors does not exceed the related TUE total unadjusted error.
3) If a reduced analog reference voltage between 1V and V_{DDPB} / 2 is used, then there are additional decrease in the ADC speed and accuracy.
4) If the analog reference voltage range is below V_{DDPB} but still in the defined range of V_{DDPB} / 2 and V_{DDPB} is used, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE, DNL, INL, Gain and Offset errors increase also by the factor 1/k.
5) If the analog reference voltage is > V_{DDPB}, then the ADC converter errors increase.
6) TUE is based on 12-bit conversion.
7) TUE is tested at V_{AREF} = V_{DDPB} = 3.3 V, V_{AGND} = 0 V. It is verified by design for all other voltages within the defined voltage range. The specified TUE is valid only if the absolute sum of input overload currents on analog port pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the measurement time.

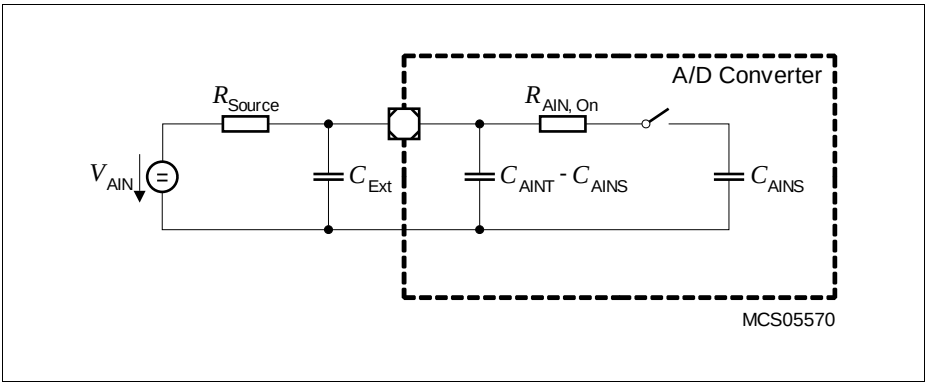

Figure 15 Equivalent Circuitry for Analog Inputs

Sample time and conversion time of the XE161xL's A/D converters are programmable. The timing above can be calculated using **Table 23**.
The limit values for f_{ADCI} must not be exceeded when selecting the prescaler value.

Table 23 A/D Converter Computation Table

GLOBCTR.5-0 (DIVA)	A/D Converter Analog Clock f_{ADCI}	INPCRx.7-0 (STC)	Sample Time[1] t_S
000000_B	f_{SYS}	00_H	$t_{ADCI} \times 2$
000001_B	f_{SYS} / 2	01_H	$t_{ADCI} \times 3$
000010_B	f_{SYS} / 3	02_H	$t_{ADCI} \times 4$
:	f_{SYS} / (DIVA+1)	:	$t_{ADCI} \times$ (STC+2)
111110_B	f_{SYS} / 63	FE_H	$t_{ADCI} \times 256$
111111_B	f_{SYS} / 64	FF_H	$t_{ADCI} \times 257$

1) The selected sample time is doubled if broken wire detection is active (due to the presampling phase).

Converter Timing Example A:

Assumptions: f_{SYS} = 80 MHz (i.e. t_{SYS} = 12.5 ns), DIVA = 03_H, STC = 00_H
Analog clock f_{ADCI} = f_{SYS} / 4 = 20 MHz, i.e. t_{ADCI} = 50 ns
Sample time t_S = $t_{ADCI} \times 2$ = 100 ns

Conversion 12-bit:

$t_{C12} = 16 \times t_{ADCI} + 2 \times t_{SYS} = 16 \times 50\text{ ns} + 2 \times 12.5\text{ ns} = 0.825\ \mu s$

Conversion 10-bit:

$t_{C10} = 12 \times t_{ADCI} + 2 \times t_{SYS} = 12 \times 50\text{ ns} + 2 \times 12.5\text{ ns} = 0.625\ \mu s$

Conversion 8-bit:

$t_{C8} = 10 \times t_{ADCI} + 2 \times t_{SYS} = 10 \times 50\text{ ns} + 2 \times 12.5\text{ ns} = 0.525\ \mu s$

Converter Timing Example B:

Assumptions: f_{SYS} = 66 MHz (i.e. t_{SYS} = 15.2 ns), DIVA = 03_H, STC = 00_H
Analog clock f_{ADCI} = f_{SYS} / 4 = 16.5 MHz, i.e. t_{ADCI} = 60.6 ns
Sample time t_S = $t_{ADCI} \times 2$ = 121.2 ns

Conversion 12-bit:

$t_{C12} = 16 \times t_{ADCI} + 2 \times t_{SYS} = 16 \times 60.6\text{ ns} + 2 \times 15.2\text{ ns} = 1.0\ \mu s$

Conversion 10-bit:

$t_{C10} = 12 \times t_{ADCI} + 2 \times t_{SYS} = 12 \times 60.6\text{ ns} + 2 \times 15.2\text{ ns} = 0.758\ \mu s$

4.5 System Parameters

The following parameters specify several aspects which are important when integrating the XE161xL into an application system.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 24 Various System Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Short-term deviation of internal clock source frequency[1]	Δf_{INT} CC	-1	–	1	%	ΔT_J = ≤ 10°C
Internal clock source frequency	f_{INT} CC	4.8	5.0	5.2	MHz	
Wakeup clock source frequency[2]	f_{WU} CC	400	–	700	kHz	FREQSEL= 00
		210	–	390	kHz	FREQSEL= 01
		140	–	260	kHz	FREQSEL= 10
		110	–	200	kHz	FREQSEL= 11
Startup time from power-on with code execution from Flash	t_{SPO} CC	1.4	1.9	2.4	ms	f_{WU} = 500 kHz
Startup time from stopover mode with code execution from PSRAM	t_{SSO} CC	11 / f_{WU}[3]	–	12 / f_{WU}[3]	µs	
Core voltage (PVC) supervision level	V_{PVC} CC	V_{LV} - 0.03	V_{LV}	V_{LV} + 0.07[4]	V	[5]
Supply watchdog (SWD) supervision level	V_{SWD} CC	V_{LV} - 0.10[6]	V_{LV}	V_{LV} + 0.15	V	voltage_range= lower [5]
		V_{LV} - 0.15	V_{LV}	V_{LV} + 0.15	V	voltage_range= upper [5]

1) The short-term frequency deviation refers to a timeframe of a few hours and is measured relative to the current frequency at the beginning of the respective timeframe. This parameter is useful to determine a time span for re-triggering a LIN synchronization.

2) This parameter is tested for the fastest and the slowest selection. The medium selections are not subject to production test - verified by design/characterization.

3) f_{WU} in MHz.

4.7.2 Definition of Internal Timing

The internal operation of the XE161xL is controlled by the internal system clock f_{SYS}.

Because the system clock signal f_{SYS} can be generated from a number of internal and external sources using different mechanisms, the duration of the system clock periods (TCSs) and their variation (as well as the derived external timing) depend on the mechanism used to generate f_{SYS}. This must be considered when calculating the timing for the XE161xL.

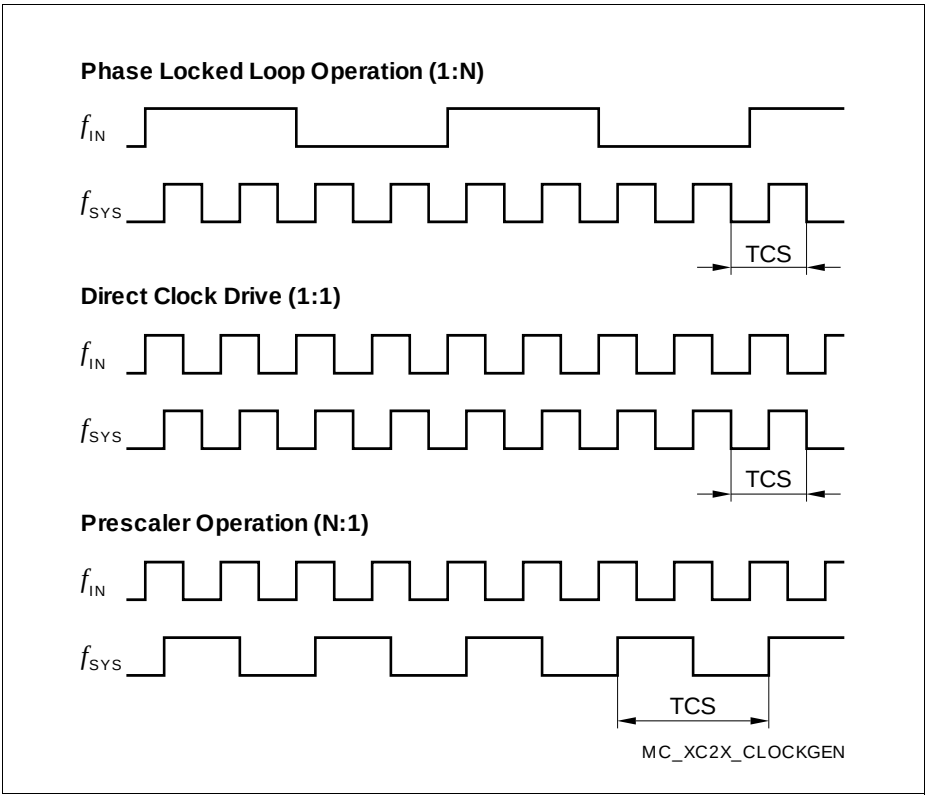

Figure 18 Generation Mechanisms for the System Clock

*Note: The example of PLL operation shown in **Figure 18** uses a PLL factor of 1:4; the example of prescaler operation uses a divider factor of 2:1.*

The specification of the external timing (AC Characteristics) depends on the period of the system clock (TCS).

Table 30 Standard Pad Parameters for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise and Fall times (10% - 90%)	t_{RF} CC	–	–	38 + 0.6 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Medium
		–	–	1 + 0.45 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Soft
		–	–	16 + 0.45 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Slow
		–	–	200 + 2.5 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Weak

1) The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and Σ-I_{OH}) must remain below 25 mA.

Table 31 Standard Pad Parameters for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output driver current (absolute value)[1)]	I_{Omax} CC	–	–	1.8	mA	Driver_Strength = Medium
		–	–	3.0	mA	Driver_Strength = Strong
		–	–	0.3	mA	Driver_Strength = Weak

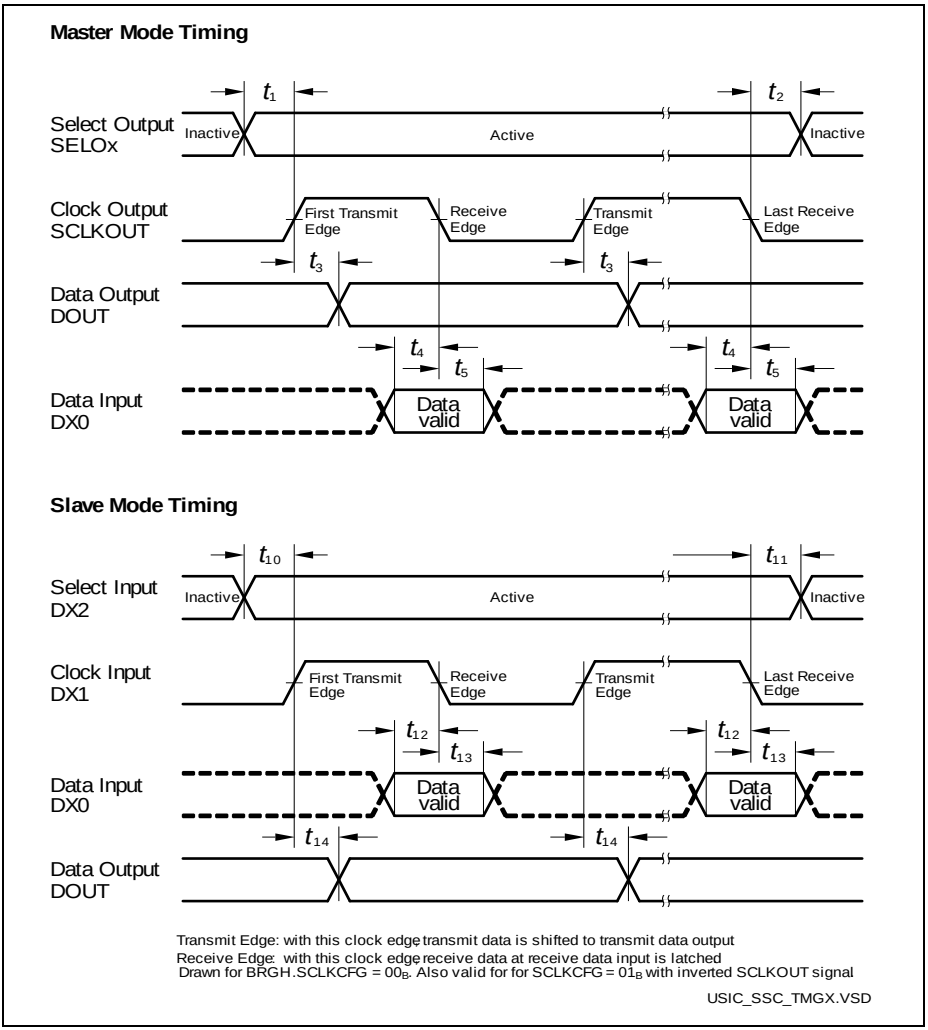

Figure 21 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.

Table 37 is valid under the following conditions: C_L= 20 pF; voltage_range= lower

Table 37 DAP Interface Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} SR	100[1)]	–	–	ns	
DAP0 high time	t_{12} SR	8	–	–	ns	
DAP0 low time	t_{13} SR	8	–	–	ns	
DAP0 clock rise time	t_{14} SR	–	–	4	ns	
DAP0 clock fall time	t_{15} SR	–	–	4	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	6	–	–	ns	pad_type= standard
DAP1 hold after DAP0 rising edge	t_{17} SR	6	–	–	ns	pad_type= standard
DAP1 valid per DAP0 clock period[2)]	t_{19} CC	87	92	–	ns	pad_type= standard

1) The debug interface cannot operate faster than the overall system, therefore $t_{11} \geq t_{SYS}$.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

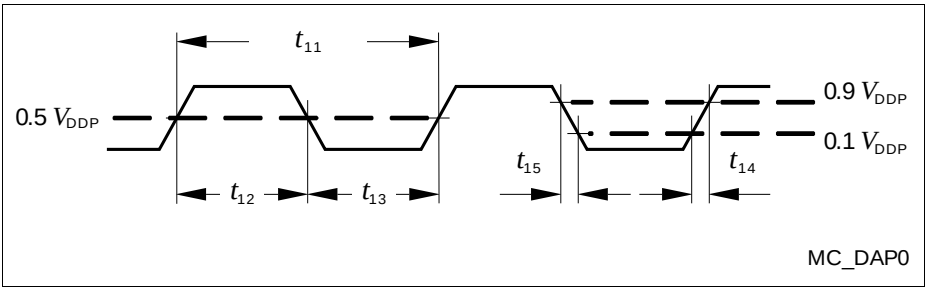

Figure 22 Test Clock Timing (DAP0)

Debug via JTAG

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 38 is valid under the following conditions: C_L= 20 pF; voltage_range= upper

Table 38 JTAG Interface Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	100[1]	–	–	ns	[2]
TCK high time	t_2 SR	16	–	–	ns	
TCK low time	t_3 SR	16	–	–	ns	
TCK clock rise time	t_4 SR	–	–	8	ns	
TCK clock fall time	t_5 SR	–	–	8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	
TDO valid from TCK falling edge (propagation delay)[3]	t_8 CC	–	29	32	ns	
TDO high impedance to valid output from TCK falling edge[4][3]	t_9 CC	–	29	32	ns	
TDO valid output to high impedance from TCK falling edge[3]	t_{10} CC	–	29	32	ns	
TDO hold after TCK falling edge[3]	t_{18} CC	5	–	–	ns	

1) The debug interface cannot operate faster than the overall system, therefore $t_1 \geq t_{SYS}$.

2) Under typical conditions, the JTAG interface can operate at transfer rates up to 10 MHz.

3) The falling edge on TCK is used to generate the TDO timing.

4) The setup time for TDO is given implicitly by the TCK cycle time.

Debug via SPD

The SPD interface will work with standard SPD tools having a sample/output clock frequency deviation of +/- 5% or less.

Note: For further details please refer to application note AP24004 in section SPD Timing Requirements.

Note: Operating Conditions apply.

5 Package and Reliability

The XE166 Family devices use the package type:

- PG-VQFN (Plastic Green - Very Thin Profile Quad Flat Non-Leaded Package)

The following specifications must be regarded to ensure proper integration of the XE161xL in its target environment.

5.1 Packaging

These parameters specify the packaging rather than the silicon.

Table 40 Package Parameters (PG-VQFN-48-54)

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Exposed Pad Dimension	Ex × Ey	–	5.2 x 5.2	mm	–
Power Dissipation	P_{DISS}	–	0.7	W	–
Thermal resistance Junction-Ambient	$R_{\Theta JA}$	–	73	K/W	No thermal via, 2-layer[1)]
			49	K/W	No thermal via, 4-layer[2)]
			43	K/W	4-layer, no pad[3)]
			34	K/W	4-layer, pad[4)]

1) Device mounted on a 2-layer JEDEC board (according to JESD 51-3) without thermal vias; exposed pad not soldered.

2) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) without thermal vias; exposed pad not soldered.

3) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad not soldered.

4) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad soldered to the board.

Note: To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground, independent of the thermal requirements.
Board layout examples are given in an application note.

Package Compatibility Considerations

The XE161xL is a member of the XE166 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In

particular, the size of the Exposed Pad (if present) may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

Package Outlines

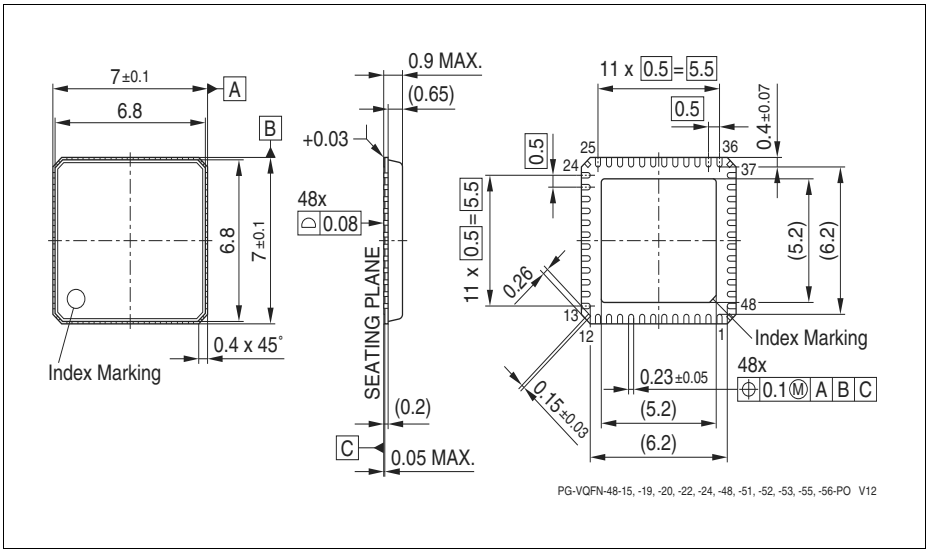

Figure 27 PG-VQFN-48-54 (Plastic Green Thin Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: **http://www.infineon.com/packages**