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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

EXF

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	LINbus, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-UQFN Exposed Pad
Supplier Device Package	16-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1574t-i-jq

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN+/DAC1OUT/	RA0	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
ICSPDAT	AN0	AN	_	ADC Channel input.
	C1IN+	AN		Comparator positive input.
	DAC1OUT	—	AN	Digital-to-Analog Converter output.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RA1/AN1/VREF+/C1IN0-/C2IN0-/	RA1	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
ICSPCLK	AN1	AN		ADC Channel input.
	VREF+	AN	_	Voltage Reference input.
	C1IN0-	AN		Comparator negative input.
	C2IN0-	AN		Comparator negative input.
	ICSPCLK	ST	_	ICSP Programming Clock.
RA2/AN2/T0CKI ⁽¹⁾ /CWG1IN ⁽¹⁾ /	RA2	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
INT ⁽¹⁾	AN2	AN	_	ADC Channel input.
	TOCKI	TTL/ST	_	Timer0 clock input.
	CWG1IN	TTL/ST	_	CWG complementary input.
	INT	TTL/ST	_	External interrupt.
RA3/VPP/MCLR	RA3	TTL/ST	_	General purpose input with IOC and WPU.
	Vpp	HV	_	Programming voltage.
	MCLR	ST	_	Master Clear with internal pull-up.
RA4/AN3/T1G ⁽¹⁾ /CLKOUT	RA4	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN3	AN	_	ADC Channel input.
	T1G	TTL/ST		Timer1 Gate input.
	CLKOUT	_	CMOS	Fosc/4 output.
RA5/CLKIN/T1CKI ⁽¹⁾	RA5	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	CLKIN	CMOS		External clock input (EC mode).
	T1CKI	TTL/ST		Timer1 clock input.
RB4/AN10	RB4	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN10	AN	_	ADC Channel input.
RB5/AN11/RX ⁽¹⁾	RB5	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN11	AN	_	ADC Channel input.
	RX	ST	_	USART asynchronous input.
RB6	RB6	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
RB7/CK	RB7	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	СК	ST	CMOS	USART synchronous clock.
RC0/AN4/C2IN+	RC0	TTL/ST	CMOS/OD	General purpose input with IOC and WPU.
	AN4	AN	_	ADC Channel input.
	C2IN+	AN		Comparator positive input.
Legendu AN - Apolog ipput or or			I mootible innu	

TABLE 1-3: PIC16(L)F1578/9 PINOUT DESCRIPTION

 Legend:
 AN = Analog input or output
 CMOS = CMOS compatible input or output
 OD = Open-Drain

 TTL = TTL compatible input
 ST = Schmitt Trigger input with CMOS levels
 I²C = Schmitt Trigger input with I²C levels

 HV = High Voltage
 XTAL = Crystal
 Levels

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
 All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 12-1.

3: These USART functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 3-5: PIC16(L)F1578 MEMORY MAP, BANKS 0-7

	BANK0		BANK1		BANK2		BANK3		BANK4		BANK5		BANK6		BANK7
000h		080h		100h		180h		200h		280h		300h		380h	
	Core Registers		Core Registers		Core Registers		Core Registers		Core Registers		Core Registers		Core Registers		Core Registers
	(Table 3-2)		(Table 3-2)		(Table 3-2)		(Table 3-2)		(Table 3-2)		(Table 3-2)		(Table 3-2)		(Table 3-2)
00Bh		08Bh		10Bh		18Bh		20Bh		28Bh		30Bh		38Bh	
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	WPUA	28Ch	ODCONA	30Ch	SLRCONA	38Ch	INLVLA
00Dh	PORTB	08Dh	TRISB	10Dh	LATB	18Dh	ANSELB	20Dh	WPUB	28Dh	ODCONB	30Dh	SLRCONB	38Dh	INLVLB
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	ANSELC	20Eh	WPUC	28Eh	ODCONC	30Eh	SLRCONC	38Eh	INLVLC
00Fh	<u> </u>	08Fh	_	10Fh		18Fh	_	20Fh		28Fh	—	30Fh	—	38Fh	—
010h	_	090h	_	110h		190h		210h	—	290h	_	310h	_	390h	—
011h	PIR1	091h	PIE1	111h	CM1CON0	191h	PMADRL	211h		291h	—	311h	—	391h	IOCAP
012h	PIR2	092h	PIE2	112h	CM1CON1	192h	PMADRH	212h		292h	—	312h	—	392h	IOCAN
013h	PIR3	093h	PIE3	113h	CM2CON0	193h	PMDATL	213h	—	293h	—	313h	—	393h	IOCAF
014h		094h		114h	CM2CON1	194h	PMDATH	214h	_	294h	_	314h	_	394h	IOCBP
015h	TMR0	095h	OPTION_REG	115h	CMOUT	195h	PMCON1	215h	—	295h	—	315h	—	395h	IOCBN
016h	TMR1L	096h	PCON	116h	BORCON	196h	PMCON2	216h	—	296h	—	316h	—	396h	IOCBF
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h	VREGCON ⁽¹⁾	217h	—	297h	—	317h	—	397h	IOCCP
018h	T1CON	098h	OSCTUNE	118h	DACCON0	198h	—	218h	—	298h	—	318h	—	398h	IOCCN
019h	T1GCON	099h	OSCCON	119h	DACCON1	199h	RCREG	219h	—	299h	—	319h	—	399h	IOCCF
01Ah	TMR2	09Ah	OSCSTAT	11Ah	—	19Ah	TXREG	21Ah	—	29Ah	—	31Ah	—	39Ah	—
01Bh	PR2	09Bh	ADRESL	11Bh	—	19Bh	SPBRGL	21Bh	—	29Bh	—	31Bh	—	39Bh	—
01Ch	T2CON	09Ch	ADRESH	11Ch	_	19Ch	SPBRGH	21Ch	_	29Ch	—	31Ch	—	39Ch	—
01Dh	—	09Dh	ADCON0	11Dh	—	19Dh	RCSTA	21Dh	—	29Dh	—	31Dh	—	39Dh	—
01Eh	—	09Eh	ADCON1	11Eh	_	19Eh	TXSTA	21Eh	—	29Eh	—	31Eh	—	39Eh	—
01Fh	_	09Fh	ADCON2	11Fh	_	19Fh	BAUDCON	21Fh	—	29Fh	—	31Fh	—	39Fh	_
020h		0A0h		120h		1A0h		220h		2A0h		320h	General	3A0h	
													Purpose		
	General		General		General		General		General		General	20Eb	16 Bytes		
	Purpose		Purpose		Purpose		Purpose		Purpose		Purpose	32F11	10 D J 100		Unimplemented
	Register 80 Bytes		Register 80 Bytes		Register 80 Bytes		Register 80 Bytes		Register 80 Bytes		Register 80 Bytes	33011	Unimplemented		Read as 0
	00 Dytes		oo bytes		oo bytes		oo bytes		oo bytes		oo bytes		Read as '0'		
005		0.55		1051				0.05		0.5.5				000	
06Fh		0EFh		16Fh		1EFh		26Fh		2EFh		36FN		3EFN	
070h		u⊢uh	A0000000	170n	A	TEON	A	270h	A	2F0h	A 0000000	370N	A	3⊢0n	A
	Common RAM		70h – 7Fh		70h – 7Fh		70h – 7Fh		70h – 7Fh		70h – 7Fh		70h – 7Fh		70h – 7Fh
07Eb		0EEb		17Eb		1EEb		27Eb		2EEb		37Eh		3EEb	/ 0.1. / 1.1.
07FN		UFFN		17-0		IFFN		_ ∠/⊢n		∠⊢⊢n		31-11		3FFN	

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: Unimplemented on PIC16LF1578.

TABLE 3-10: PIC16(L)F1574/5/8/9 MEMORY MAP, BANKS 24-31

	BANK 24		BANK 25		BANK 26		BANK 27		BANK 28		BANK 29		BANK 30		BANK 31
C00h	Core Registers	C80h	Core Registers	D00h	Core Registers	D80h	Core Registers	E00h	Core Registers	E80h	Core Registers	F00h	Core Registers	F80h	Core Registers
C0Bh	(Table 3-2)	C8Bh	(Table 3-2)	D0Bh	(Table 3-2)	D8Bh	(Table 3-2)	E0Bh	(Table 3-2)	E8Bh	(Table 3-2)	F0Bh	(Table 3-2)	F8Bh	(Table 3-2)
C0Ch	_	C8Ch	_	D0Ch	_	D8Ch		E0Ch		E8Ch		F0Ch	—	F8Ch	
C0Dh	—	C8Dh	—	D0Dh	—							F0Dh	_		
C0Eh	—	C8Eh	—	D0Eh	_							F0Eh			
C0Fh	_	C8Fh	_	D0Fh	—							F0Fh	—		
C10h	_	C90h	_	D10h	—							F10h	—		
C11h	—	C91h	—	D11h	—							F11h	—		
C12h	—	C92h	—	D12h	—							F12h	—		
C13h	—	C93h	—	D13h	—							F13h	—		
C14h	—	C94h	—	D14h	—							F14h	—		
C15h	—	C95h	—	D15h	—							F15h			
C16h	—	C96h	—	D16h	—							F16h	_		
C17h		C97h	_	D17h	_							F17h			
C18h	—	C98h	—	D18h	—		See Table 3-11		See Table 3-12		See Table 3-12	F18h			See Table 3-13
C19h	_	C99h	_	D19h	_							F19h			
C1Ah	—	C9Ah	—	D1Ah	—							F1Ah	_		
C1Bh	—	C9Bh	—	D1Bh	—							F1Bh	_		
C1Ch	—	C9Ch	—	D1Ch	—							F1Ch	—		
C1Dh	_	C9Dh		D1Dh								F1Dh			
		C9En	_		_							FIEN			
C20h	_	C9Fn	_	D1Fn D20h	_							F1FN F20h			
02011		0/1011		DZOII								1 2011			
	Unimplemented Read as '0'		Unimplemented Read as '0'		Unimplemented Read as '0'								Unimplemented Read as '0'		
C6Fh		CEEh		D6Fh		DEEh		F6F h		FFFh		F6Fh		FFFh	
C70h		CF0h		D70h		DF0h		E70h		EF0h		F70h		FF0h	
	Accesses		Accesses		Accesses		Accesses		Accesses		Accesses		Accesses		Accesses
	70h – 7Fh		70h – 7Fh		70h – 7Fh		70h – 7Fh		70h – 7Fh		70h – 7Fh		70h – 7Fh		70h – 7Fh
CFFh		CFFh		D7Fh		DFFh		E7Fh		EFFh		F7Fh		FFFh	

Legend: = Unimplemented data memory locations, read as '0'

TABLE 3-15: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 2											
10Ch	LATA	_	—	LATA5	LATA4	_	LATA2	LATA1	LATA0	xx -xxx	uu -uuu
10Dh	LATB ⁽¹⁾	LATB7	LATB6	LATB5	LATB4	—	—	—	—	xxxx	xxxx
10Eh	LATC	LATC7 ⁽¹⁾	LATC6 ⁽¹⁾	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx xxxx	XXXX XXXX
10Fh	—	Unimpleme	nted					•	_	_	
110h	—	Unimpleme	nted							_	_
111h	CM1CON0	C10N	C10UT	_	C1POL	—	C1SP	C1HYS	C1SYNC	00-0 -100	00-0 -100
112h	CM1CON1	C1INTP	C1INTN	C1PC	CH<1:0>	—		C1NCH<2:0>		0000 -000	0000 -000
113h	CM2CON0	C2ON	C2OUT	_	C2POL	—	C2SP	C2HYS	C2SYNC	00-0 -100	00-0 -100
114h	CM2CON1	C2INTP	C2INTN	C2PC	CH<1:0>	—		C2NCH<2:0>		0000 -000	0000 -000
115h	CMOUT	_	_	_	_	—	—	MC2OUT	MC1OUT	00	00
116h	BORCON	SBOREN	BORFS	_	_	—	—	—	BORRDY	10q	uuu
117h	FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAF	/R<1:0>	ADFV	R<1:0>	0000 00p0	0q00 0000
118h	DACCON0	DACEN	_	DACOE	_	DACPS	SS<1:0>	—	—	0-0- 00	0-0- 00
119h	DACCON1	_	_	_			DACR<4:0>			0 0000	0 0000
11Ah to 11Fh	_	Unimpleme	_	_							

PIC16(L)F1574/5/8/9

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'.

 Note
 1:
 PIC16(L)F1578/9 only.

 2:
 PIC16F1574/5/8/9 only.

3: Unimplemented, read as '1'.

5.3 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bits of the OSCCON register. The following clock sources can be selected using the SCS bits:

- Default system oscillator determined by FOSC bits in Configuration Words
- Internal Oscillator Block (INTOSC)

5.3.1 SYSTEM CLOCK SELECT (SCS) BITS

The System Clock Select (SCS) bits of the OSCCON register selects the system clock source that is used for the CPU and peripherals.

- When the SCS bits of the OSCCON register = 00, the system clock source is determined by value of the FOSC<1:0> bits in the Configuration Words.
- When the SCS bits of the OSCCON register = 01, the system clock source is the Timer1 oscillator.
- When the SCS bits of the OSCCON register = 1x, the system clock source is chosen by the internal oscillator frequency selected by the IRCF<3:0> bits of the OSCCON register. After a Reset, the SCS bits of the OSCCON register are always cleared.

Note:	Any automatic clock switch does not
	update the SCS bits of the OSCCON
	register. The user can monitor the OSTS
	bit of the OSCSTAT register to determine
	the current system clock source.

When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 5-1.

5.4 Clock Switching Before Sleep

When clock switching from an old clock to a new clock is requested just prior to entering Sleep mode, it is necessary to confirm that the switch is complete before the SLEEP instruction is executed. Failure to do so may result in an incomplete switch and consequential loss of the system clock altogether. Clock switching is confirmed by monitoring the clock Status bits in the OSCSTAT register. Switch confirmation can be accomplished by sensing that the ready bit for the new clock is set or the ready bit for the old clock is cleared. For example, when switching between the internal oscillator with the PLL and the internal oscillator without the PLL, monitor the PLLR bit. When PLLR is set, the switch to 32 MHz operation is complete. Conversely, when PLLR is cleared, the switch from 32 MHz operation to the selected internal clock is complete.

IABLE 5-1:	OSCILLATOR SWITCHING DELAYS

Switch From	Switch To	Frequency	Oscillator Delay
Sleep/POR	LFINTOSC ⁽¹⁾ MFINTOSC ⁽¹⁾ HFINTOSC ⁽¹⁾	31 kHz 31.25 kHz-500 kHz 31.25 kHz-16 MHz	Oscillator Warm-up Delay (Twarm) ⁽²⁾
Sleep/POR	EC ⁽¹⁾	DC – 32 MHz	2 cycles
LFINTOSC	EC ⁽¹⁾	DC – 32 MHz	1 cycle of each
Any clock source	MFINTOSC ⁽¹⁾ HFINTOSC ⁽¹⁾	31.25 kHz-500 kHz 31.25 kHz-16 MHz	2 μs (approx.)
Any clock source	LFINTOSC ⁽¹⁾	31 kHz	1 cycle of each
PLL inactive	PLL active	16-32 MHz	2 ms (approx.)

Note 1: PLL inactive.

2: See Section 27.0 "Electrical Specifications".

R/W-0/0	R/W-0/0	R-0/0	R-0/0	U-0	U-0	R/W-0/0	R/W-0/0				
TMR1GIF	ADIF	RCIF	TXIF	—	—	TMR2IF	TMR1IF				
bit 7							bit 0				
Legend:											
R = Readab	ole bit	W = Writable	bit	U = Unimplemented bit, read as '0'							
u = Bit is unchanged		x = Bit is unkr	nown	-n/n = Value at POR and BOR/Value at all other Resets							
'1' = Bit is se	et	'0' = Bit is cle	ared								
bit 7	TMR1GIF: Ti	mer1 Gate Inte	rrupt Flag bit								
	1 = Interrupt i 0 = Interrupt i	is pending is not pending									
bit 6	bit 6 ADIF: ADC Interrupt Flag bit										
	1 = Interrupt is pending 0 = Interrupt is not pending										
bit 5	BCIE: USART Receive Interrunt Elag bit										
Sit 0	1 = Interrupt i	is pendina	aptriag bit								
	0 = Interrupt	is not pending									
bit 4	TXIF: USART	Transmit Inter	rupt Flag bit								
	1 = Interrupt i 0 = Interrupt i	is pending is not pending									
bit 3-2	Unimplemen	ted: Read as '	0'								
bit 1	TMR2IF: Tim	er2 to PR2 Inte	errupt Flag bit								
	1 = Interrupt i 0 = Interrupt i	is pending is not pending									
bit 0	TMR1IF: Tim	er1 Overflow Ir	nterrupt Flag b	it							
	1 = Interrupt	is pending									
	0 = Interrupt	is not pending									
Note: In co if	nterrupt flag bits a condition occurs, r ts corresponding	re set when an egardless of the enable bit or th	interrupt e state of le Global								
l l	nterrupt Enable b	it, GIE of the	INTCON								

REGISTER 7-5: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Interrupt Enable bit, GIE of the INTCON
	register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. The USART RCIF and TXIE bits are read only.
	and this are redu-unly.

9.0 WATCHDOG TIMER (WDT)

The Watchdog Timer is a system timer that generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events.

The WDT has the following features:

- Independent clock source
- Multiple operating modes
 - WDT is always on
 - WDT is off when in Sleep
 - WDT is controlled by software
 - WDT is always off
- Configurable time-out period is from 1 ms to 256 seconds (nominal)
- Multiple Reset conditions
- Operation during Sleep





U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1		
—	—	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0		
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'					
u = Bit is uncha	anged	x = Bit is unkn	nown	-n/n = Value at POR and BOR/Value at all other Resets					
'1' = Bit is set		'0' = Bit is clea	ared						

REGISTER 11-5: WPUA: WEAK PULL-UP PORTA REGISTER

bit 7-6 Unimplemented: Read as '0'

bit 5-0 WPUA<5:0>: Weak Pull-up Register bits⁽³⁾ 1 = Pull-up enabled 0 = Pull-up disabled

Note 1: Global WPUEN bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.

- 2: The weak pull-up device is automatically disabled if the pin is configured as an output.
- **3:** For the WPUA3 bit, when MCLRE = 1, weak pull-up is internally enabled, but not reported here.

REGISTER 11-6: ODCONA: PORTA OPEN-DRAIN CONTROL REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	ODA5	ODA4	—	ODA2	ODA1	ODA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6	Unimplemented: Read as '0'
bit 5-4	ODA<5:4>: PORTA Open-Drain Enable bits For RA<5:4> pins, respectively 1 = Port pin operates as open-drain drive (sink current only) 0 = Port pin operates as standard push-pull drive (source and sink current)
bit 3	Unimplemented: Read as '0'
bit 2-0	ODA<2:0>: PORTA Open-Drain Enable bits For RA<2:0> pins, respectively 1 = Port pin operates as open-drain drive (sink current only) 0 = Port pin operates as standard push-pull drive (source and sink current)

12.3 Bidirectional Pins

PPS selections for peripherals with bidirectional signals on a single pin must be made so that the PPS input and PPS output select the same pin. Peripherals that have bidirectional signals include:

- EUSART (synchronous operation)
- MSSP (I²C)

Note: The I²C default input pins are I²C and SMBus compatible and are the only pins on the device with this compatibility.

12.4 PPS Lock

The PPS includes a mode in which all input and output selections can be locked to prevent inadvertent changes. PPS selections are locked by setting the PPSLOCKED bit of the PPSLOCK register. Setting and clearing this bit requires a special sequence as an extra precaution against inadvertent changes. Examples of setting and clearing the PPSLOCKED bit are shown in Example 12-1.

EXAMPLE 12-1: PPS LOCK/UNLOCK SEQUENCE

;	suspend interrupts
	bcf INTCON,GIE
;	BANKSEL PPSLOCK ; set bank
;	required sequence, next 5 instructions
	movlw 0x55
	movwf PPSLOCK
	movlw 0xAA
	movwf PPSLOCK
;	Set PPSLOCKED bit to disable writes or
;	Clear PPSLOCKED bit to enable writes
	bsf PPSLOCK, PPSLOCKED
;	restore interrupts
	bsf INTCON,GIE

12.5 PPS Permanent Lock

The PPS can be permanently locked by setting the PPS1WAY Configuration bit. When this bit is set, the PPSLOCKED bit can only be cleared and set one time after a device Reset. This allows for clearing the PPSLOCKED bit so that the input and output selections can be made during initialization. When the PPSLOCKED bit is set after all selections have been made, it will remain set and cannot be cleared until after the next device Reset event.

12.6 Operation During Sleep

PPS input and output selections are unaffected by Sleep.

12.7 Effects of a Reset

A device Power-On-Reset (POR) clears all PPS input and output selections to their default values. All other Resets leave the selections unchanged. Default input selections are shown in Table 12-1.

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	_	—		ADRE	S<9:8>
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit, read	l as '0'	
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at a				R/Value at all o	other Resets		
'1' = Bit is set		'0' = Bit is clea	ared				

REGISTER 16-6: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1

bit 7-2 **Reserved**: Do not use.

bit 1-0	ADRES<9:8>: ADC Result Register bits
	Upper two bits of 10-bit conversion result

REGISTER 16-7: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ADRES<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ADRES<7:0>**: ADC Result Register bits Lower eight bits of 10-bit conversion result

P/M/-0/u	P/M/_0/u	P/M/_0/u	P/\/_0/		P_v/v	P/M/_0/u	P/M_0/u	
	T10D0'			T4000/		T109	S<1.0>	
IMR1GE	TIGPOL	IIGIM	TIGSPM	DONE	11GVAL	1103	5<1.02	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimplem	nented bit, read	1 as '0'		
u = Bit is unch	anged	x = Bit is unkr	nown	-n/n = Value a	t POR and BO	R/Value at all	other Resets	
'1' = Bit is set		'0' = Bit is clea	ared	HC = Bit is cle	eared by hardw	are		
bit 7 TMR1GE: Timer1 Gate Enable bit <u>If TMR1ON = 0</u> : This bit is ignored <u>If TMR1ON = 1</u> : 1 = Timer1 counting is controlled by the Timer1 gate function 0 = Timer1 counts according of Timer1 gate function								
bit 6	T1GPOL: Tin	ner1 Gate Pola	rity bit					
	1 = Timer1 g 0 = Timer1 g	ate is active-hi ate is active-lo	gh (Timer1 cou w (Timer1 cou	unts when gate nts when gate i	is high) s low)			
bit 5	T1GTM: Time	er1 Gate Toggle	e Mode bit					
	1 = Timer1 G 0 = Timer1 G Timer1 gate f	Bate Toggle mo Bate Toggle mo Iip-flop toggles	de is enabled de is disabled on every rising	and toggle flip- g edge.	flop is cleared			
bit 4	T1GSPM: Tin	ner1 Gate Sing	le-Pulse Mode	e bit				
	1 = Timer1 g 0 = Timer1 g	ate Single-Puls ate Single-Puls	se mode is ena se mode is disa	abled and is cor abled	ntrolling Timer1	gate		
bit 3	T1GGO/DON	E: Timer1 Gate	e Single-Pulse	Acquisition Sta	itus bit			
	 1 = Timer1 gate single-pulse acquisition is ready, waiting for an edge 0 = Timer1 gate single-pulse acquisition has completed or has not been started 							
bit 2	T1GVAL: Timer1 Gate Value Status bit Indicates the current state of the Timer1 gate that could be provided to TMR1H:TMR1L. Unaffected by Timer1 Gate Enable (TMR1GE).							
bit 1-0	T1GSS<1:0>	: Timer1 Gate	Source Select	bits				
	11GSS<1:U>: Timer1 Gate Source Select bits 11 = Comparator 2 optionally synchronized output (C2OUT_sync) 10 = Comparator 1 optionally synchronized output (C1OUT_sync) 01 = Timer0 overflow output (T0_overflow) 00 = Timer1 gate pin (T1G)							

REGISTER 20-2: T1GCON: TIMER1 GATE CONTROL REGISTER

21.1 Timer2 Operation

The clock input to the Timer2 module is the system instruction clock (Fosc/4).

TMR2 increments from 00h on each clock edge.

A 4-bit counter/prescaler on the clock input allows direct input, divide-by-4 and divide-by-16 prescale options. These options are selected by the prescaler control bits, T2CKPS<1:0> of the T2CON register. The value of TMR2 is compared to that of the Period register, PR2, on each clock cycle. When the two values match, the comparator generates a match signal as the timer output. This signal also resets the value of TMR2 to 00h on the next cycle and drives the output counter/ postscaler (see Section 21.2 "Timer2 Interrupt").

The TMR2 and PR2 registers are both directly readable and writable. The TMR2 register is cleared on any device Reset, whereas the PR2 register initializes to FFh. Both the prescaler and postscaler counters are cleared on the following events:

- · a write to the TMR2 register
- · a write to the T2CON register
- Power-On Reset (POR)
- Brown-Out Reset (BOR)
- MCLR Reset
- Watchdog Timer (WDT) Reset
- · Stack Overflow Reset
- Stack Underflow Reset
- RESET Instruction

Note:	TMR2	is	not	cleared	when	T2CON	is
	written.						

21.2 Timer2 Interrupt

Timer2 can also generate an optional device interrupt. The Timer2 output signal (T2_match) provides the input for the 4-bit counter/postscaler. This counter generates the TMR2 match interrupt flag which is latched in TMR2IF of the PIR1 register. The interrupt is enabled by setting the TMR2 Match Interrupt Enable bit, TMR2IE of the PIE1 register.

A range of 16 postscale options (from 1:1 through 1:16 inclusive) can be selected with the postscaler control bits, T2OUTPS<3:0>, of the T2CON register.

21.3 Timer2 Output

The output of TMR2 is T2_match.

The T2_match signal is synchronous with the system clock. Figure 21-3 shows two examples of the timing of the T2_match signal relative to Fosc and prescale value, T2CKPS<1:0>. The upper diagram illustrates 1:1 prescale timing and the lower diagram, 1:X prescale timing.

FIGURE 21-3: T2_MATCH TIMING DIAGRAM



21.4 Timer2 Operation During Sleep

Timer2 cannot be operated while the processor is in Sleep mode. The contents of the TMR2 and PR2 registers will remain unchanged while the processor is in Sleep mode.

Mnemonic, Operands		Description	Cyclos	14-Bit Opcode				Status	Notoo
		Description	Cycles	MSb			LSb	Affected	Notes
		CONTROL OPERA	TIONS						
BRA	k	Relative Branch	2	11	001k	kkkk	kkkk		
BRW	_	Relative Branch with W	2	00	0000	0000	1011		
CALL	k	Call Subroutine	2	10	0kkk	kkkk	kkkk		
CALLW	-	Call Subroutine with W	2	00	0000	0000	1010		
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
RETFIE	k	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	0100	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
		INHERENT OPERA	TIONS						
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO, PD	
NOP	-	No Operation	1	00	0000	0000	0000		
OPTION	-	Load OPTION_REG register with W	1	00	0000	0110	0010		
RESET	-	Software device Reset	1	00	0000	0000	0001		
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	TO, PD	
TRIS	f	Load TRIS register with W	1	00	0000	0110	Offf		
		C-COMPILER OPT	IMIZED						
ADDFSR	n, k	Add Literal k to FSRn	1	11	0001	0nkk	kkkk		
MOVIW	n mm	Move Indirect FSRn to W with pre/post inc/dec	1	00	0000	0001	0nmm	Z	2, 3
		modifier, mm					kkkk		
	k[n]	Move INDFn to W, Indexed Indirect.	1	11	1111	0nkk	1nmm	Z	2
MOVWI	n mm	Move W to Indirect FSRn with pre/post inc/dec	1	00	0000	0001	kkkk		2, 3
		modifier, mm							
	k[n]	Move W to INDFn, Indexed Indirect.	1	11	1111	1nkk			2

TABLE 26-3: ENHANCED MID-RANGE INSTRUCTION SET (CONTINUED)

Note 1: If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

2: If this instruction addresses an INDF register and the MSb of the corresponding FSR is set, this instruction will require one additional instruction cycle.

3: See Table in the MOVIW and MOVWI instruction descriptions.

27.2 Standard Operating Conditions

The standard operating conditions for any device are defined as: $V \text{DDMIN} \leq V \text{DD} \leq V \text{DDMAX}$ Operating Voltage: Operating Temperature: TA MIN \leq TA \leq TA MAX VDD — Operating Supply Voltage⁽¹⁾ PIC16LF1574/5/8/9 PIC16F1574/5/8/9 TA — Operating Ambient Temperature Range Industrial Temperature TA MIN.....--40°C **Extended Temperature** Ta MIN.....--40°C

Note 1: See Parameter D001, DS Characteristics: Supply Voltage.

*

TABLE 27-8: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated)									
Param. No.	Sym.	Characteristic	Freq. Tolerance	Min.	Тур†	Max.	Units	Conditions	
OS08	HFosc	Internal Calibrated HFINTOSC Frequency ⁽¹⁾	±2%		16.0		MHz	VDD = 3.0V, TA = 25°C, (Note 2)	
OS09	LFosc	Internal LFINTOSC Frequency	_	_	31	_	kHz		
OS10*	TWARM	HFINTOSC Wake-up from Sleep Start-up Time	_		5	15	μS		
		LFINTOSC Wake-up from Sleep Start-up Time	—		0.5		ms		

These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 μ F and 0.01 μ F values in parallel are recommended.

2: See Figure 27-6: "HFINTOSC Frequency Accuracy over Device VDD and Temperature.

FIGURE 27-6: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE



Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions
F10	Fosc	Oscillator Frequency Range	4		8	MHz	
F11	Fsys	On-Chip VCO System Frequency	16		32	MHz	
F12	TRC	PLL Start-up Time (Lock Time)	—	-	2	ms	
F13*	ΔCLK	CLKOUT Stability (Jitter)	-0.25%	-	+0.25%	%	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 27-13: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING



TABLE 27-17: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions	
US120	ТскН2ртV	SYNC XMIT (Master and Slave)	_	80	ns	$3.0V \le V\text{DD} \le 5.5V$	
		Clock high to data-out valid	—	100	ns	$1.8V \leq V\text{DD} \leq 5.5V$	
US121	TCKRF	Clock out rise time and fall time (Master mode)	_	45	ns	$3.0V \le V\text{DD} \le 5.5V$	
			_	50	ns	$1.8V \leq V\text{DD} \leq 5.5V$	
US122	TDTRF	Data-out rise time and fall time	—	45	ns	$3.0V \leq V\text{DD} \leq 5.5V$	
			_	50	ns	$1.8V \le V\text{DD} \le 5.5V$	

FIGURE 27-14: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



TABLE 27-18: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions	
US125	TDTV2CKL	SYNC RCV (Master and Slave) Data-hold before CK \downarrow (DT hold time)	10		ns		
US126	TCKL2DTL	Data-hold after CK \downarrow (DT hold time)	15	_	ns		

PIC16(L)F1574/5/8/9



(BOR), BORV = 1, PIC16LF1574/5/8/9 Only.



FIGURE 28-26: Ipd, Brown-Out Reset (BOR), BORV = 1, PIC16F1574/5/8/9 Only.



Reset (LPBOR = 0), PIC16LF1574/5/8/9 Only.



FIGURE 28-28: Ipd, Low-Power Brown-Out Reset (LPBOR = 0), PIC16F1574/5/8/9 Only.



FIGURE 28-29: Ipd, ADC Non Converting, PIC16LF1574/5/8/9 Only.



FIGURE 28-30: Ipd, ADC Non Converting, PIC16F1574/5/8/9 Only.

29.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- · Support for the entire device instruction set
- Support for fixed-point and floating-point data
- · Command-line interface
- · Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

29.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- · Integration into MPLAB X IDE projects
- User-defined macros to streamline
 assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

29.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

29.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- · Support for the entire device instruction set
- · Support for fixed-point and floating-point data
- · Command-line interface
- Rich directive set
- · Flexible macro language
- · MPLAB X IDE compatibility

20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





VI	EW	С	

l	Jnits	N	S			
Dimension Limits		MIN	NOM	MAX		
Number of Pins	Ν	20				
Pitch	е		1.27 BSC			
Overall Height	А	-	-	2.65		
Molded Package Thickness	A2	2.05	I	-		
Standoff §	A1	0.10	-	0.30		
Overall Width	E	10.30 BSC				
Molded Package Width	E1	7.50 BSC				
Overall Length	D	12.80 BSC				
Chamfer (Optional)	h	0.25	I	0.75		
Foot Length	L	0.40	-	1.27		
Footprint	L1	1.40 REF				
Lead Angle	Θ	0°	-	-		
Foot Angle	φ	0°	-	8°		
Lead Thickness	С	0.20	-	0.33		
Lead Width	b	0.31	-	0.51		
Mold Draft Angle Top	α	5°	-	15°		
Mold Draft Angle Bottom	β	5°	-	15°		

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-094C Sheet 2 of 2

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