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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	LINbus, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1575-i-sl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 2: PACKAGES

Packages	PDIP	SOIC	TSSOP	SSOP	UQFN
PIC16(L)F1574	•	•	•		•
PIC16(L)F1575	•	•	•		•
PIC16(L)F1578	•	•		•	•
PIC16(L)F1579	•	•		•	•

Note: Pin details are subject to change.

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
	_			TUN	<5:0>		
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'	
u = Bit is uncha	anged	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all	other Resets
'1' = Bit is set		'0' = Bit is clea	ared				
bit 7-6	Unimplemen	nted: Read as '	0'				
bit 5-0	TUN<5:0>: F	requency Tunir	ng bits				
	100000 = M	linimum frequer	псу				
	•						
	•						
	111111 =						
	000000 = O	scillator module	e is running at	the factory-calil	brated frequen	cy.	
	000001 =						
	•						
	•						
	011110 =						
	011111 = M	laximum freque	ncy				

REGISTER 5-3: OSCTUNE: OSCILLATOR TUNING REGISTER

PIC16(L)F1574/5/8/9



2: Asynchronous interrupt latency = 3-5 TCY. Synchronous latency = 3-4 TCY, where TCY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: For minimum width of INT pulse, refer to AC specifications in Section 27.0 "Electrical Specifications".

4: INTF is enabled to be set any time during the Q4-Q1 cycles.

9.6 Register Definitions: Watchdog Control

U-0	U-0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1	R/W-1/1	R/W-0/0
_				WDTPS<4:0	>		SWDTEN
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	l as '0'	
u = Bit is uncha	anged	x = Bit is unkr	iown	-n/n = Value a	at POR and BO	R/Value at all o	other Resets
'1' = Bit is set		'0' = Bit is clea	ared				
bit 7-6	Unimplemen	ted: Read as ')'				
bit 5-1	WDTPS<4:0	: Watchdog Tir	mer Period Se	elect bits ⁽¹⁾			
	Bit Value = F	Prescale Rate					
	11111 = Re	served. Results	s in minimum	interval (1:32)			
	•						
	•						
	10011 = Re	served. Results	s in minimum	interval (1:32)			
		22					
	10010 = 1:8	3388608 (2 ²³) (I	nterval 256s	nominal)			
	10001 = 1:4	194304 (2 ²²) (1	nterval 128s	nominal)			
	10000 = 1.2	2097 152 (2) (1 1048576 (2 ²⁰) (1	nterval 32s n	ominal)			
	01111 = 1.1 01110 = 1.5	524288 (2 ¹⁹) (In	terval 16s no	minal)			
	01101 = 1:2	262144 (2 ¹⁸) (In	terval 8s non	ninal)			
	01100 = 1:1	131072 (2 ¹⁷) (In	terval 4s non	ninal)			
	01011 = 1:6	5536 (Interval	2s nominal) (, Reset value)			
	01010 = 1:3	32768 (Interval	1s nominal)	· · · · · ·			
	01001 = 1:1	6384 (Interval	512 ms nomir	nal)			
	01000 = 1:8	3192 (Interval 2	56 ms nomina	al)			
	00111 = 1:4	1096 (Interval 12	28 ms nomina	al)			
	00110 = 1:2	2048 (Interval 64	4 ms nominal)			
	00101 = 1:1	024 (Interval 3	2 ms nominal)			
	00100 = 1:5	512 (Interval 16	ms nominal)				
	00011 = 1:2	256 (Interval 8 n	ns nominal)				
	00010 = 1:1	28 (Interval 4 n	ns nominal)				
	00001 = 1:6	64 (Interval 2 m	s nominal)				
	00000 = 1.3						
DIT U	SWDIEN: SO	offware Enable/	Disable for W	atchdog Timer	DI		
	This bit is ign	$2 = 1 \times 1$					
		> = 01					
	1 = WDT is t	urned on					
	0 = WDT is t	urned off					
	If WDTE<1:0	> = 00:					
	This bit is ign	ored.					

REGISTER 9-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER



W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0				
Program Memory Control Register 2											
bit 7 bit 0											
Legend:											
R = Readable I	bit	W = Writable	bit	U = Unimple	mented bit, read	l as '0'					
S = Bit can only	y be set	x = Bit is unkr	iown	-n/n = Value	at POR and BO	R/Value at all c	other Resets				
'1' = Bit is set		'0' = Bit is clea	ared								

REGISTER 10-6: PMCON2: PROGRAM MEMORY CONTROL 2 REGISTER

bit 7-0 Flash Memory Unlock Pattern bits

To unlock writes, a 55h must be written first, followed by an AAh, before setting the WR bit of the PMCON1 register. The value written to this register is used to unlock the writes. There are specific timing requirements on these writes.

TABLE 10-3: SUMMARY OF REGISTERS ASSOCIATED WITH FLASH PROGRAM MEMORY

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page	
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	86	
PMCON1	(1)	CFGS	LWLO	FREE	WRERR	WREN	WR	RD	115	
PMCON2	Program Memory Control Register 2									
PMADRL				PMAD	RL<7:0>				114	
PMADRH	(1)			F	MADRH<6:0	>			114	
PMDATL	PMDATL<7:0>									
PMDATH	_	_			PMDAT	H<5:0>			114	

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Flash program memory.

Note 1: Unimplemented, read as '1'.

TABLE 10-4: SUMMARY OF CONFIGURATION WORD WITH FLASH PROGRAM MEMORY

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
0015104	13:8	_	—	—	—	CLKOUTEN	BORE	N<1:0>	—	50
CONFIGT	7:0	CP	MCLRE	PWRTE	WDTE	=<1:0>	—	FOSC	<1:0>	00
0015100	13:8	_	—	LVP	DEBUG	LPBOR	BORV	STVREN	PLLEN	F7
CONFIG2	7:0	-	_	_	_	_	PPS1WAY	WRT	<1:0>	57

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Flash program memory.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELB	—	_	ANSB5	ANSB4	_	_		—	127
INLVLB	INLVLB7	INLVLB6	INLVLB5	INLVLB4	—	—	—	—	128
LATB	LATB7	LATB6	LATB5	LATB4	—	—	—	—	126
ODCONB	ODB7	ODB6	ODB5	ODB4	—	—	—	—	128
PORTB	RB7	RB6	RB5	RB4	—	—	—	—	126
SLRCONB	SLRB7	SLRB6	SLRB5	SLRB4	—	—	—	—	128
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	128
WPUB	WPUB7	WPUB6	WPUB5	WPUB4	_	_	_	_	127

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTB.

11.5 PORTC Registers

11.5.1 DATA REGISTER

PORTC is a 6-bit wide bidirectional port in the PIC16(L)F1574/5 device and 8-bit wide bidirectional port in the PIC16(L)F1578/9 device. The corresponding data direction register is TRISC (Register 11-18). Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 11-1 shows how to initialize an I/O port.

Reading the PORTC register (Register 11-17) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATC).

11.5.2 DIRECTION CONTROL

The TRISC register (Register 11-18) controls the PORTC pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISC register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

11.5.3 INPUT THRESHOLD CONTROL

The INLVLC register (Register 11-24) controls the input voltage threshold for each of the available PORTC input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTC register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Table 27-4 for more information on threshold levels.

Note: Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

11.5.4 OPEN DRAIN CONTROL

The ODCONC register (Register 11-22) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONC bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCONC bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

11.5.5 SLEW RATE CONTROL

The SLRCONC register (Register 11-23) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONC bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONC bit is cleared, The corresponding port pin drive slews at the maximum rate possible.

11.5.6 ANALOG CONTROL

The ANSELC register (Register 11-20) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELC bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELC bits has no effect on digital output functions. A pin with TRIS clear and ANSELC set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELC bits default to the Analog
	mode after Reset. To use any pins as
	digital general purpose or peripheral
	inputs, the corresponding ANSEL bits
	must be initialized to '0' by user software.

11.5.7 PORTC FUNCTIONS AND OUTPUT PRIORITIES

Each pin defaults to the PORT latch data after Reset. Other functions are selected with the peripheral pin select logic. See **Section 12.0** "**Peripheral Pin Select** (**PPS**) **Module**" for more information.

Analog input functions, such as ADC inputs, are not shown in the peripheral pin select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELC register. Digital output functions may continue to control the pin when it is in Analog mode.

REGISTER 11-20:	ANSELC: PORTC ANALOG SELECT REGISTER
-----------------	--------------------------------------

R/W-1/1	R/W-1/1	U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1			
ANSC7 ⁽²⁾	ANSC6 ⁽²⁾	—	—	ANSC3	ANSC2	ANSC1	ANSC0			
bit 7				•		•	bit 0			
Legend:										
R = Readab	le bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'				
u = Bit is une	changed	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all o	other Resets			
'1' = Bit is se	et	'0' = Bit is clea	ared							
bit 7-6	ANSC<7:6 >: 0 = Digital I/ 1 = Analog ir	Analog Select O. Pin is assigr ıput. Pin is ass	between Anale ned to port or c igned as analo	og or Digital Fu digital special fu og input ⁽¹⁾ . Digit	nction on pins Inction. tal input buffer	RC<7:6>, resp disabled.	ectively ^(1, 2)			
bit 5-4	Unimplemen	ted: Read as '	0'							
bit 3-0	bit 3-0 ANSC<3:0> : Analog Select between Analog or Digital Function on pins RC<3:0>, respectively ⁽¹⁾ 0 = Digital I/O. Pin is assigned to port or digital special function. 1 = Analog input. Pin is assigned as analog input ⁽¹⁾ . Digital input buffer disabled.									
Note 1: V	Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to									

allow external control of the voltage on the pin. 2: ANSC<7:6> are available on PIC16(L)F1578/9 only.

REGISTER 11-21: WPUC: WEAK PULL-UP PORTC REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
WPUC7 ⁽³⁾	WPUC6 ⁽³⁾	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 WPUC<7:0>: Weak Pull-up Register bits⁽³⁾

1 = Pull-up enabled

0 = Pull-up disabled

Note 1: Global WPUEN bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is configured as an output.

3: WPUC<7:6> are available on PIC16(L)F1578/9 only.

16.4 ADC Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 16-5. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD), refer to Figure 16-5. The maximum recommended impedance for analog sources is 10 k Ω . As the

source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an ADC acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 16-1 may be used. This equation assumes that 1/2 LSb error is used (1,024 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 16-1: ACQUISITION TIME EXAMPLE

Assumptions: Temperature = 50°C and external impedance of $10k\Omega 5.0V VDD$ TACQ = Amplifier Settling Time + Hold Capacitor Charging Time + Temperature Coefficient<math>= TAMP + TC + TCOFF $= 2\mu s + TC + [(Temperature - 25°C)(0.05\mu s/°C)]$ The value for TC can be approximated with the following equations: $VAPPLIED\left(1 - \frac{1}{(2^{n+1}) - 1}\right) = VCHOLD$;[1] VCHOLD charged to within 1/2 lsb $VAPPLIED\left(1 - e^{\frac{-TC}{RC}}\right) = VCHOLD$;[2] VCHOLD charge response to VAPPLIED $VAPPLIED\left(1 - e^{\frac{-TC}{RC}}\right) = VCHOLD$;[2] VCHOLD charge response to VAPPLIED $VAPPLIED\left(1 - e^{\frac{-TC}{RC}}\right) = VAPPLIED\left(1 - \frac{1}{(2^{n+1}) - 1}\right)$; combining [1] and [2] Note: Where n = number of bits of the ADC. Solving for TC: $TC = -CHOLD(RIC + RSS + RS) \ln(1/2047)$

$$= -12.5pF(1k\Omega + 7k\Omega + 10k\Omega) \ln(0.0004885)$$

= 1.715µs

Therefore:

$$TACQ = 2\mu s + 1.715\mu s + [(50^{\circ}C - 25^{\circ}C)(0.05\mu s/^{\circ}C)]$$

= 4.96\mu s

Note 1: The reference voltage (VRPOS) has no effect on the equation, since it cancels itself out.

- 2: The charge holding capacitor (CHOLD) is not discharged after each conversion.
- **3:** The maximum recommended impedance for analog sources is 10 k Ω . This is required to meet the pin leakage specification.

19.1.3 SOFTWARE PROGRAMMABLE PRESCALER

A software programmable prescaler is available for exclusive use with Timer0. The prescaler is enabled by clearing the PSA bit of the OPTION_REG register.

Note:	The Watchdog Timer (WDT) uses its own
	independent prescaler.

There are eight prescaler options for the Timer0 module ranging from 1:2 to 1:256. The prescale values are selectable via the PS<2:0> bits of the OPTION_REG register. In order to have a 1:1 prescaler value for the Timer0 module, the prescaler must be disabled by setting the PSA bit of the OPTION_REG register.

The prescaler is not readable or writable. All instructions writing to the TMR0 register will clear the prescaler.

19.1.4 TIMER0 INTERRUPT

Timer0 will generate an interrupt when the TMR0 register overflows from FFh to 00h. The TMR0IF interrupt flag bit of the INTCON register is set every time the TMR0 register overflows, regardless of whether or not the Timer0 interrupt is enabled. The TMR0IF bit can only be cleared in software. The Timer0 interrupt enable is the TMR0IE bit of the INTCON register.

Note:	The Timer0 interrupt cannot wake the						
	processor from Sleep since the timer is						
	frozen during Sleep.						

19.1.5 8-BIT COUNTER MODE SYNCHRONIZATION

When in 8-Bit Counter mode, the incrementing edge on the T0CKI pin must be synchronized to the instruction clock. Synchronization can be accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the instruction clock. The high and low periods of the external clocking source must meet the timing requirements as shown in **Section 27.0 "Electrical Specifications"**.

19.1.6 OPERATION DURING SLEEP

Timer0 cannot operate while the processor is in Sleep mode. The contents of the TMR0 register will remain unchanged while the processor is in Sleep mode.

22.5.2 SYNCHRONOUS SLAVE MODE

The following bits are used to configure the EUSART for synchronous slave operation:

- SYNC = 1
- CSRC = 0
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXSTA register configures the device for synchronous operation. Clearing the CSRC bit of the TXSTA register configures the device as a slave. Clearing the SREN and CREN bits of the RCSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCSTA register enables the EUSART.

22.5.2.1 EUSART Synchronous Slave Transmit

The operation of the Synchronous Master and Slave modes are identical (see Section 22.5.1.3 "Synchronous Master Transmission"), except in the case of the Sleep mode. If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

- 1. The first character will immediately transfer to the TSR register and transmit.
- 2. The second word will remain in the TXREG register.
- 3. The TXIF bit will not be set.
- After the first character has been shifted out of TSR, the TXREG register will transfer the second character to the TSR and the TXIF bit will now be set.
- If the PEIE and TXIE bits are set, the interrupt will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will call the Interrupt Service Routine.
- 22.5.2.2 Synchronous Slave Transmission Set-up:
- 1. Set the SYNC and SPEN bits and clear the CSRC bit.
- 2. Clear the ANSEL bit for the CK pin (if applicable).
- 3. Clear the CREN and SREN bits.
- If interrupts are desired, set the TXIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 5. If 9-bit transmission is desired, set the TX9 bit.
- 6. Enable transmission by setting the TXEN bit.
- 7. If 9-bit transmission is selected, insert the Most Significant bit into the TX9D bit.
- 8. Start transmission by writing the Least Significant eight bits to the TXREG register.

TABLE 22-9:SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE
TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	204
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	86
PIE1	TMR1GIE	ADIE	RCIE	TXIE	—	—	TMR2IE	TMR1IE	87
PIR1	TMR1GIF	ADIF	RCIF	TXIF	—	—	TMR2IF	TMR1IF	90
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	203
TXREG	EUSART Transmit Data Register								194*
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	202

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for synchronous slave transmission.

* Page provides register information.

23.3 Offset Modes

The Offset modes provide the means to adjust the waveform of a slave PWM module relative to the waveform of a master PWM module in the same device.

23.3.1 INDEPENDENT RUN MODE

In Independent Run mode (OFM = 00), the PWM module is unaffected by the other PWM modules in the device. The PWMxTMR associated with the PWM module in this mode starts counting as soon as the EN bit associated with this PWM module is set and continues counting until the EN bit is cleared. Period events reset the PWMxTMR to zero after which the timer continues to count.

A detailed timing diagram of this mode used with Standard PWM mode is shown in Figure 23-8.

23.3.2 SLAVE RUN MODE WITH SYNC START

In Slave Run mode with Sync Start (OFM = 01), the slave PWMxTMR waits for the master's OF_match event. When this event occurs, if the EN bit is set, the PWMxTMR begins counting and continues to count until software clears the EN bit. Slave period events reset the PWMxTMR to zero after which the timer continues to count.

A detailed timing diagram of this mode used with Standard PWM mode is shown in Figure 23-9.

23.3.3 ONE-SHOT SLAVE MODE WITH SYNC START

In One-Shot Slave mode with Synchronous Start (OFM = 10), the slave PWMxTMR waits until the master's OF_match event. The timer then begins counting, starting from the value that is already in the timer and continues to count until the period match event. When the period event occurs, the timer resets to zero and stops counting. The timer then waits until the next master OF_match event, after which it begins counting again to repeat the cycle. An OF_match event that occurs before the slave PWM has completed the previously triggered period will be ignored. A slave period that is greater than the master period, but less than twice the master period, will result in a slave output every other master period.

Note: During the time the slave timers are resetting to zero, if another Offset Match event is received, it is possible that the slave PWM would not recognize this match event and the slave timers would fail to begin counting again. This would result in missing duty cycles from the output of the slave PWM. To prevent this from happening, avoid using the same period for both the master and slave PWM's.

A detailed timing diagram of this mode used with Standard PWM mode is shown in Figure 23-10.

23.3.4 CONTINUOUS RUN SLAVE MODE WITH SYNC START AND TIMER RESET

In Continuous Run Slave mode with Synchronous Start and Timer Reset (OFM = 11) the slave PWMxTMR is inhibited from counting after the slave PWM enable is set. The first master OF match event starts the slave PWMxTMR. Subsequent master OF_match events reset the slave PWMxTMR timer value back to 1 after which the slave PWMxTMR continues to count. The next master OF match event resets the slave PWMxTMR back to 1 to repeat the cycle. Slave period events that occur before the master's OF match event will reset the slave PWMxTMR to zero after which the timer will continue to count. Slaves operating in this mode must have a PWMxPH register pair value equal to or greater than 1, otherwise, the phase match event will not occur precluding the start of the PWM output duty cycle.

The offset timing will persist If both the master and slave PWMxPR values are the same and the Slave Offset mode is changed to Independent Run mode while the PWM module is operating.

A detailed timing diagram of this mode used in Standard PWM mode is shown in Figure 23-11.

Note:	Unexpected results will occur if the slave
	PWM_clock is a higher frequency than the
	master PWM_clock.

23.3.5 OFFSET MATCH IN CENTER-ALIGNED MODE

When a master is operating in Center-Aligned mode the offset match event depends on which direction the PWMxTMR is counting. Clearing the OFO bit of the PWMxOFCON register will cause the OF_match event to occur when the timer is counting up. Setting the OFO bit of the PWMxOFCON register will cause the OF_match event to occur when the timer is counting down. The OFO bit is ignored in non-center-aligned modes.

The OFO bit is double buffered and requires setting the LDA bit to take effect when the PWM module is operating.

Detailed timing diagrams of Center-Aligned mode using offset match control in Independent Slave with Sync Start mode can be seen in Figure 23-12 and Figure 23-13.

REGISTER 23-15: PWMxTMRH: PWMx TIMER HIGH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u			
	TMR<15:8>									
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable I	bit	U = Unimplemented bit, read as '0'						
u = Bit is unchanged x = Bit is unknown		iown	-n/n = Value a	at POR and BC	R/Value at all	other Resets				
'1' = Bit is set		'0' = Bit is clea	ared							

bit 7-0 TMR<15:8>: PWM Timer High bits Upper eight bits of PWM timer counter

REGISTER 23-16: PWMxTMRL: PWMx TIMER LOW REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u		
TMR<7:0>									
bit 7 bit 0									

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 TMR<7:0>: PWM Timer Low bits Lower eight bits of PWM timer counter ٦

R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	
GxASE	GxARSEN	_	_	GxASDSC2	GxASDSC1	GxASDSPPS	—	
bit 7			•				bit 0	
Legend:								
R = Readable	bit	W = Writable	e bit	U = Unimpler	mented bit, read	l as '0'		
u = Bit is unch	anged	x = Bit is unk	nown	-n/n = Value a	at POR and BO	R/Value at all oth	er Resets	
'1' = Bit is set		'0' = Bit is cle	eared	q = Value dep	pends on condit	ion		
bit 7	GxASE: Auto	-Shutdown Ev	ent Status bi	t				
	1 = An auto-s	shutdown eve	nt has occurre	ed				
	0 = No auto-s	shutdown eve	nt has occurr	ed				
bit 6	GxARSEN: A	uto-Restart E	nable bit					
	1 = Auto-rest	tart is enabled						
	0 = Auto-rest	tart is disabled	1					
bit 5-4	Unimplemen	ted: Read as	'0'					
bit 3	GxASDSC2:	CWG Auto-sh	utdown on C	omparator C2 I	Enable bit			
	1 = Shutdow	n when Comp	arator C2 out	put (C2OUT_s	ync) is high			
	0 = Compara	ator C2 output	has no effect	on shutdown				
bit 2	GxASDSC1:	CWG Auto-sh	utdown on C	omparator C1 I	Enable bit			
	1 = Shutdown when Comparator C1 output (C1OUT_sync) is high							
	0 = Comparator C1 output has no effect on shutdown							
bit 1 GxASDSPPS: CWG Input Pin Enable bit								
	1 = Shutdow	n when CWG	input pin (CV	/GxIN) is high				
	0 = CWG inp	out pin (CWGx	IN) signal has	s no effect on s	hutdown			
bit 0	Unimplemented: Read as '0'							

REGISTER 24-3: CWGxCON2: CWG CONTROL REGISTER 2

Standard Operating Conditions (unless otherwise stated)								
Param. No.	Sym.	Characteristic	Тур.	Units	Conditions			
TH01	θJA	Thermal Resistance Junction to Ambient	70	°C/W	14-pin PDIP package			
			95.3	°C/W	14-pin SOIC package			
			100	°C/W	14-pin TSSOP package			
			31.8	°C/W	16-pin UQFN 4x4mm package			
			62.2	°C/W	20-pin PDIP package			
			77.7	°C/W	20-pin SOIC package			
			87.3	°C/W	20-pin SSOP package			
			32.8	°C/W	20-pin UQFN 4x4mm package			
TH02	θJC	Thermal Resistance Junction to Case	32.75	°C/W	14-pin PDIP package			
			31	°C/W	14-pin SOIC package			
			24.4	°C/W	14-pin TSSOP package			
			24.4	°C/W	16-pin UQFN 4x4mm package			
			27.5	°C/W	20-pin PDIP package			
			23.1	°C/W	20-pin SOIC package			
			31.1	°C/W	20-pin SSOP package			
			27.4	°C/W	20-pin UQFN 4x4mm package			
TH03	Тјмах	Maximum Junction Temperature	150	°C				
TH04	PD	Power Dissipation	-	W	PD = PINTERNAL + PI/O			
TH05	PINTERNAL	Internal Power Dissipation	—	W	PINTERNAL = IDD x VDD ⁽¹⁾			
TH06	Pi/o	I/O Power Dissipation	—	W	$PI/O = \Sigma (IOL * VOL) + \Sigma (IOH * (VDD - VOH))$			
TH07	Pder	Derated Power		W	Pder = PDmax (Tj - Ta)/θja ⁽²⁾			

TABLE 27-6: THERMAL CHARACTERISTICS

Note 1: IDD is current to run the chip alone without driving any load on the output pins.

2: TA = Ambient Temperature; TJ = Junction Temperature









Note 1: If the ADC clock source is selected as FRC, a time of TCY is added before the ADC clock starts. This allows the SLEEP instruction to be executed.



FIGURE 28-43: HFINTOSC Accuracy Over Temperature, VDD = 1.8V, LF Devices Only.



FIGURE 28-44: HFINTOSC Accuracy Over Temperature, $2.3V \le VDD \le 5.5V$.



FIGURE 28-45: Brown-Out Reset Voltage, BORV = 1, PIC16LF1574/5/8/9 Only.



FIGURE 28-46: Brown-Out Reset Hysteresis, BORV = 1, PIC16LF1574/5/8/9 Only.



FIGURE 28-47: Brown-Out Reset Voltage, BORV = 1, PIC16F1574/5/8/9 Only.



FIGURE 28-48: Brown-Out Reset Hysteresis, BORV = 1, PIC16F1574/5/8/9 Only.

16-Lead Ultra Thin Plastic Quad Flat, No Lead Package (JQ) - 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimensio	MIN	NOM	MAX	
Contact Pitch E		0.65 BSC		
Optional Center Pad Width	X2			2.70
Optional Center Pad Length	Y2			2.70
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X16)	X1			0.35
Contact Pad Length (X16)	Y1			0.80

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2257A

20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	С		9.40	
Contact Pad Width (X20)	Х			0.60
Contact Pad Length (X20)	Y			1.95
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.45		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2094A

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