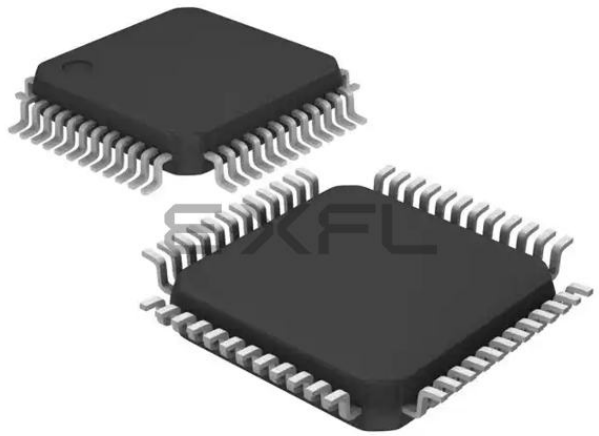
Renesas Electronics America Inc - UPD70F3814GA(R)-GAM-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, CSI, EBI/EMI, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 6x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3814ga-r-gam-ax

(5) TAAn I/O control register 2 (TAAnIOC2)

The TAAnIOC2 register is an 8-bit register that controls the valid edge of the external event count input signal (TIAAn0 pin) and external trigger input signal (TIAAn0 pin).

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: TAA0IOC2 FFFFF634H, TAA1IOC2 FFFFF644H, TAA2IOC2 FFFFF654H

TAAnIOC2 (n = 0 to 2)

7	6	5	4	3	2	1	0
0	0	0	0	TAAnEES1	TAAnEES0	TAAnETS1	TAAnETS0

TAAnEES1	TAAnEES0	External event count input signal (TIAAn0 pin) valid edge setting
0	0	No edge detection (external event count invalid)
0	1	Detection of rising edge
1	0	Detection of falling edge
1	1	Detection of both edges

TAAnETS1	TAAnETS0	External trigger input signal (TIAAn0 pin) valid edge setting
0	0	No edge detection (external trigger invalid)
0	1	Detection of rising edge
1	0	Detection of falling edge
1	1	Detection of both edges

Cautions

1. **Rewrite the TAAnEES1, TAAnEES0, TAAnETS1, and TAAnETS0 bits when the TAAnCTL0.TAAnCE bit = 0. (The same value can be written when the TAAnCE bit = 1.) If rewriting was mistakenly performed, clear the TAAnCE bit to 0 and then set the bits again.**
2. **The TAAnEES1 and TAAnEES0 bits are valid only when the TAAnCTL1.TAAnEEE bit = 1 or when the external event count mode (TAAnCTL1.TAAnMD2 to TAAnCTL1.TAAnMD0 bits = 001) has been set.**
3. **The TAAnETS1 and TAAnETS0 bits are valid only when the external trigger pulse output mode (TAAnCTL1.TAAnMD2 to TAAnCTL1.TAAnMD0 bits = 010) or the one-shot pulse output mode (TAAnCTL1.TAAnMD2 to TAAnCTL1.TAAnMD0 = 011) is set.**

(11) TAAn counter read buffer register (TAAnCNT)

The TAAnCNT register is a read buffer register that can read the count value of the 16-bit counter.

If this register is read when the TAAnCTL0.TAAnCE bit = 1, the count value of the 16-bit timer can be read.

This register is read-only, in 16-bit units.

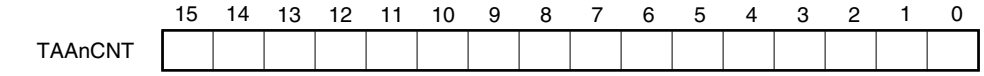
The value of the TAAnCNT register is cleared to 0000H when the TAAnCE bit = 0. If the TAAnCNT register is read at this time, the value of the 16-bit counter (FFFFH) is not read, but 0000H is read.

Reset clears the TAAnCE bit to 0. Therefore, the value of the TAAnCNT register is cleared to 0000H.

Caution Accessing the TAAnCNT register is prohibited in the following statuses. For details, see 3.4.9 (2) Accessing specific on-chip peripheral I/O registers.

- **When the CPU operates with the subclock and the main clock oscillation is stopped**
- **When the CPU operates with the internal oscillation clock**

After reset: 0000H R Address: TAA0CNT FFFFF63AH, TAA1CNT FFFFF64AH, TAA2CNT FFFFF65AH, TAA4CNT FFFFF67AH



TAAnCNT

(n = 0 to 2, 4)

(8) TMT0 option register 0 (TT0OPT0)

The TT0OPT0 register is an 8-bit register that sets the capture/compare operation and detects overflows.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF607H

	7	6	5	4	3	2	1	<0>
TT0OPT0	0	0	TT0CCS1	TT0CCS0	0	0	0	TT0OVF

TT0CCS1	TT0CCR1 register capture/compare selection
0	Selected as compare register
1	Selected as capture register (cleared by the TT0CTL0.TT0CE bit = 0)
The TT0CCS1 bit setting is valid only in the free-running timer mode.	

TT0CCS0	TT0CCR0 register capture/compare selection
0	Selected as compare register
1	Selected as capture register (cleared by the TT0CTL0.TT0CE bit = 0)
The TT0CCS0 bit setting is valid only in the free-running timer mode.	

TT0OVF	TMT0 overflow detection flag
Set (1)	Overflow occurred
Reset (0)	0 written to TT0OVF bit or TT0CTL0.TT0CE bit = 0

- The TT0OVF bit is set to 1 when the 16-bit counter value overflows from FFFFH to 0000H in the free-running timer mode or the pulse width measurement mode.
- An overflow interrupt request signal (INTTT0OV) is generated when the TT0OVF bit is set to 1. The INTTT0OV signal is not generated in modes other than the free-running timer mode and the pulse width measurement mode.
- The TT0OVF bit is not cleared to 0 even when the TT0OVF bit or the TT0OPT0 register are read when the TT0OVF bit = 1.
- Before clearing the TT0OVF bit to 0 after generation of the INTTT0OV signal, be sure to confirm (by reading) that the TT0OVF bit is set to 1.
- The TT0OVF bit can be both read and written, but the TT0OVF bit cannot be set to 1 by software. Writing 1 has no effect on the operation of TMT0.

Cautions 1. Rewrite the TT0CCS1 and TT0CCS0 bits when the TT0CE bit = 0. (The same value can be written when the TT0CE bit = 1.) If rewriting was mistakenly performed, clear the TT0CE bit to 0 and then set these bits again.

2. Be sure to set bits 1 to 3, 6, and 7 to "0".

(1) Basic counter operation

This section explains the basic operation of the 16-bit counter. For details, refer to the description of the operation in each mode.

(a) Count start operation

- **Encoder compare mode**

  A count operation is controlled by TENC00 and TENC01 phases.

  The 16-bit counter initial setting is performed by transferring the set value of the TT0TCW register to the 16-bit counter and the count operation is started. (When the TT0CTL2.TT0ECC bit = 0, the TT0TCW register set value is transferred to the 16-bit counter at the timing when the TT0CTL0.TT0CE bit changes from 0 to 1.)

- **Triangular-wave PWM mode**

  The 16-bit counter starts counting from the initial value FFFFH.

  It counts up FFFFH, 0000H, 0001H, 0002H, 0003H, and so on.

  Following the count-up operation, the counter counts down upon a match between the 16-bit count value and the CCR0 buffer register.

- **Mode other than above**

  The 16-bit counter starts counting from the initial value FFFFH.

  It counts up FFFFH, 0000H, 0001H, 0002H, 0003H, and so on.

(b) Clear operation

The 16-bit counter is cleared to 0000H when its value matches the value of the compare register, when its value is captured, when the edge of the encoder clear signal is detected, and when the clear level condition of the TENC00, TENC01, and TECR0 pins is detected. The count operation from FFFFH to 0000H that takes place immediately after the counter has started counting or when the counter overflows is not a clear operation. Therefore, the INTTT0CC0 and INTTT0CC1 interrupt signals are not generated.

(c) Overflow operation

The 16-bit counter overflows when it counts up from FFFFH to 0000H in the free-running mode, pulse width measurement mode, and encoder compare mode. If the counter overflows in the free-running mode and pulse width measurement mode, the TT0OPT0.TT0OVF bit is set to 1 and an interrupt request signal (INTTT0OV) is generated.

If the counter overflows in the encoder compare mode, the TT0OPT1.TT0EOF bit is set to 1 and an interrupt request signal (INTTT0OV) is generated.

Note that the INTTT0OV signal is not generated under the following conditions.

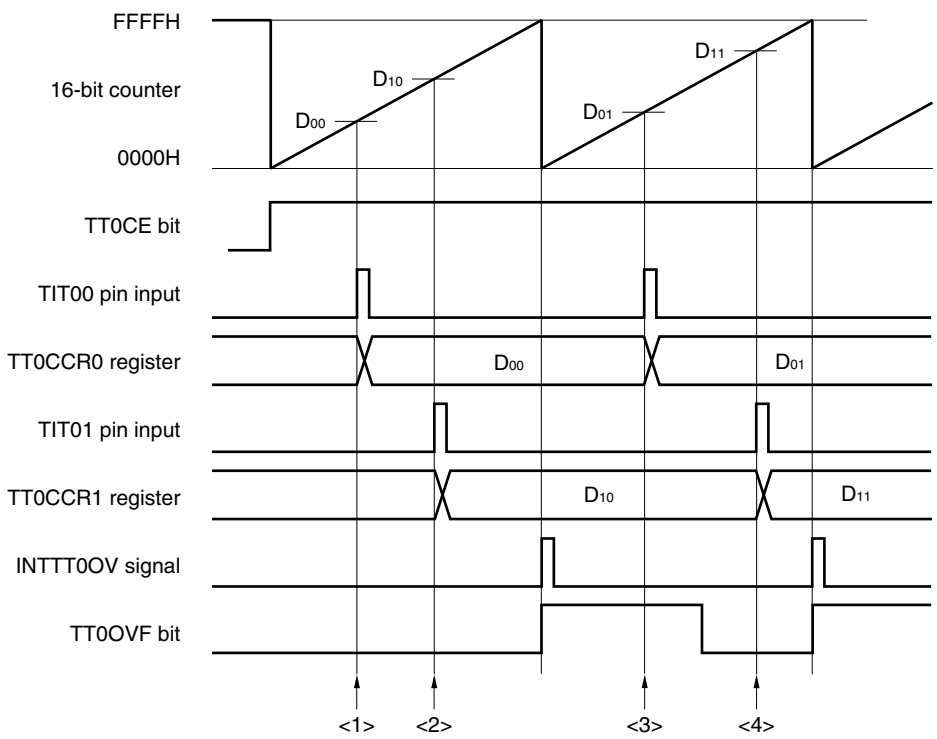
- Immediately after a count operation has been started
- If the counter value matches the compare value FFFFH and is cleared
- When FFFFH is captured and cleared to 0000H in the pulse width measurement mode

Caution After the overflow interrupt request signal (INTTT0OV) has been generated, be sure to check that the overflow flag (TT0OVF, TT0EOF bits) is set to 1.

(c) Processing of overflow when two capture registers are used

Care must be exercised in processing the overflow flag when two capture registers are used. First, an example of incorrect processing is shown below.

Example of incorrect processing when two capture registers are used



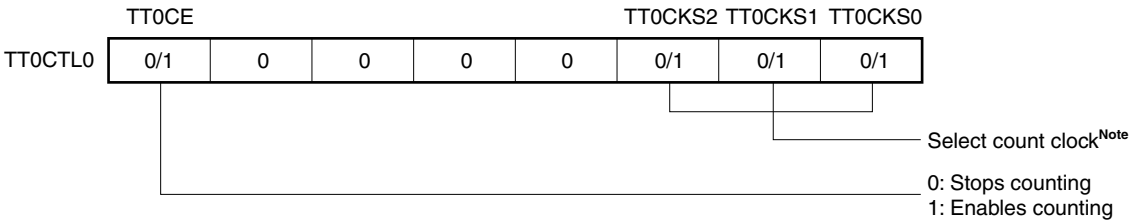
The following problem may occur when two pulse widths are measured in the free-running timer mode.

<1> Read the TT0CCR0 register (setting of the default value of the TIT00 pin input).
<2> Read the TT0CCR1 register (setting of the default value of the TIT01 pin input).
<3> Read the TT0CCR0 register.
Read the overflow flag. If the overflow flag is 1, clear it to 0.
Because the overflow flag is 1, the pulse width can be calculated by (10000H + D_{01} − D_{00}).
<4> Read the TT0CCR1 register.
Read the overflow flag. Because the flag is cleared in <3>, 0 is read.
Because the overflow flag is 0, the pulse width can be calculated by (D_{11} − D_{10}) (incorrect).

When two capture registers are used, and if the overflow flag is cleared to 0 by one capture register, the other capture register may not obtain the correct pulse width.
Use software when using two capture registers. An example of how to use software is shown below.

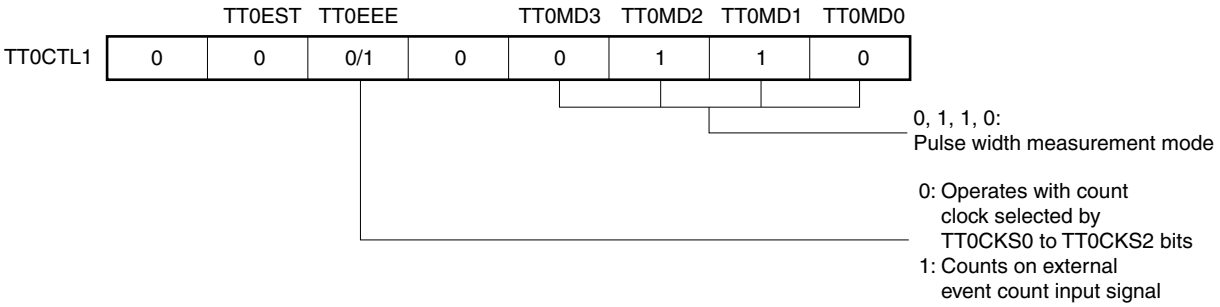
Figure 8-41. Register Setting in Pulse Width Measurement Mode (1/2)

(a) TMT0 control register 0 (TT0CTL0)

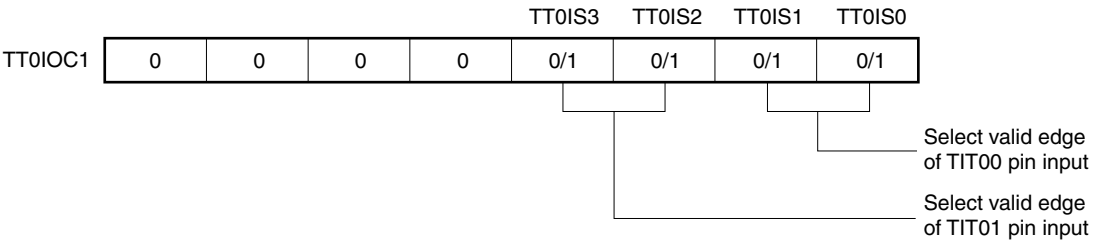


Note Setting is invalid when the TT0CTL1.TT0EEE bit = 1.

(b) TMT0 control register 1 (TT0CTL1)



(c) TMT0 I/O control register 1 (TT0IOC1)



(d) TMT0 I/O control register 2 (TT0IOC2)

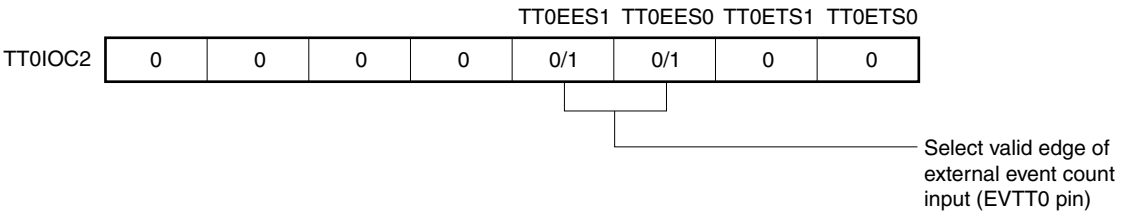


Table 11-7. Range of Frequencies That Can Be Corrected When DEV Bit = 0

F6	F5 to F0	RC1SUBC Correction Value	Frequency of Connected Clock (Including Steady-State Deviation)
0	000000	No correction	–
0	000001	No correction	–
0	000010	Increments RC1SUBC count value by 2 once every 20 seconds	32.76810000 kHz
0	000011	Increments RC1SUBC count value by 4 once every 20 seconds	32.76820000 kHz
0	000100	Increments RC1SUBC count value by 6 once every 20 seconds	32.76830000 kHz
		⋮	
0	111011	Increments RC1SUBC count value by 120 once every 20 seconds	32.77400000 kHz
0	111110	Increments RC1SUBC count value by 122 once every 20 seconds	32.77410000 kHz
0	111111	Increments RC1SUBC count value by 124 once every 20 seconds	32.77420000 kHz (upper limit)
1	000000	No correction	–
1	000001	No correction	–
1	000010	Decrements RC1SUBC count value by 124 once every 20 seconds	32.76180000 kHz (lower limit)
1	000011	Decrements RC1SUBC count value by 122 once every 20 seconds	32.76190000 kHz
1	000100	Decrements RC1SUBC count value by 120 once every 20 seconds	32.76200000 kHz
		⋮	
1	11011	Decrements RC1SUBC count value by 6 once every 20 seconds	32.76770000 kHz
1	11110	Decrements RC1SUBC count value by 4 once every 20 seconds	32.76780000 kHz
1	11111	Decrements RC1SUBC count value by 2 once every 20 seconds	32.76790000 kHz

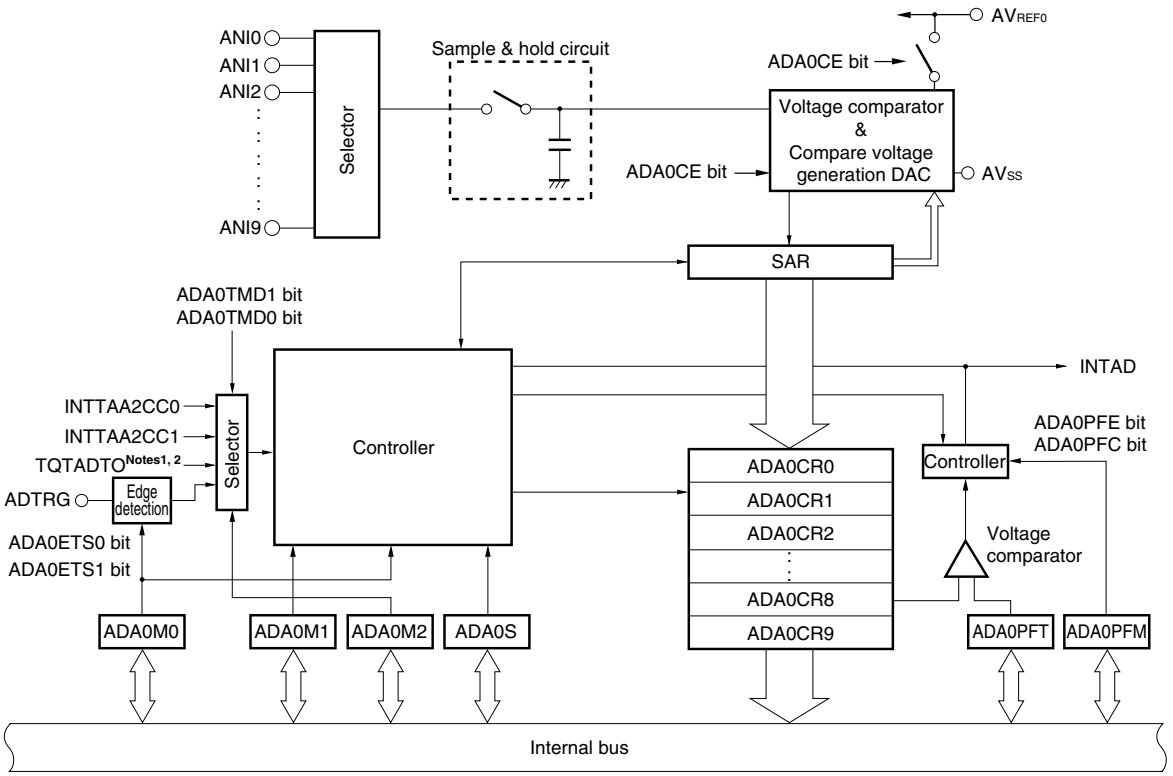
Table 11-8. Range of Frequencies That Can Be Corrected When DEV Bit = 1

F6	F5 to F0	RC1SUBC Correction Value	Frequency of Connected Clock (Including Steady-State Deviation)
0	000000	No correction	–
0	000001	No correction	–
0	000010	Increments RC1SUBC count value by 2 once every 60 seconds	32.76803333 kHz
0	000011	Increments RC1SUBC count value by 4 once every 60 seconds	32.76806667 kHz
0	000100	Increments RC1SUBC count value by 6 once every 60 seconds	32.76810000 kHz
		⋮	
0	111011	Increments RC1SUBC count value by 120 once every 60 seconds	32.77000000 kHz
0	111110	Increments RC1SUBC count value by 122 once every 60 seconds	32.77003333 kHz
0	111111	Increments RC1SUBC count value by 124 once every 60 seconds	32.77006667 kHz (upper limit)
1	000000	No correction	–
1	000001	No correction	–
1	000010	Decrements RC1SUBC count value by 124 once every 60 seconds	32.76593333 kHz (lower limit)
1	000011	Decrements RC1SUBC count value by 122 once every 60 seconds	32.76596667 kHz
1	000100	Decrements RC1SUBC count value by 120 once every 60 seconds	32.76600000 kHz
		⋮	
1	11011	Decrements RC1SUBC count value by 6 once every 60 seconds	32.76790000 kHz
1	11110	Decrements RC1SUBC count value by 4 once every 60 seconds	32.76793333 kHz
1	11111	Decrements RC1SUBC count value by 2 once every 60 seconds	32.76796667 kHz

14.3 Configuration

The block diagram of the A/D converter is shown below.

Figure 14-1. Block Diagram of A/D Converter



Notes1. V850ES/JE3-H only

2. The timer trigger signal from 6-phase PWM output circuit (TMQOP)

The A/D converter includes the following hardware.

Table 14-1. Configuration of A/D Converter

Item	Configuration
Analog inputs	10 channels (ANI0 to ANI9 pins)
Registers	Successive approximation register (SAR) A/D conversion result registers 0 to 9 (ADA0CR0 to ADA0CR9) A/D conversion result registers 0H to 9H (ADCR0H to ADCR9H): Only higher 8 bits can be read
Control registers	A/D converter mode registers 0 to 2 (ADA0M0 to ADA0M9) A/D converter channel specification register 0 (ADA0S) Power fail compare mode register (ADA0PFM) Power fail compare threshold value register (ADA0PFT)

(12) Compare voltage generation DAC

This compare voltage generation DAC is connected between AV_{REF0} and AV_{SS} and generates a voltage for comparison with the analog input signal.

(13) ANI0 to ANI9 pins

These are analog input pins for the 10 A/D converter channels and are used to input analog signals to be converted into digital signals. Pins other than the one selected as the analog input by the ADA0S register can be used as input port pins.

Caution Make sure that the voltages input to the ANI0 to ANI9 pins do not exceed the rated values. In particular if a voltage of AV_{REF0} or higher is input to a channel, the conversion value of that channel becomes undefined, and the conversion values of the other channels may also be affected.

(14) AV_{REF0} pin

This is the pin used to input the reference voltage of the A/D converter. Always make the potential at this pin the same as that at the V_{DD} pin even when the A/D converter is not used.

The signals input to the ANI0 to ANI9 pins are converted to digital signals based on the voltage applied between the AV_{REF0} and AV_{SS} pins.

(15) AV_{SS} pin

This is the ground potential pin of the A/D converter. Always make the potential at this pin the same as that at the V_{SS} pin even when the A/D converter is not used.

16.3.4 Mode switching between UARTC4, CSIF0, and I²C01

In the V850ES/JC3-H and V850ES/JE3-H, UARTC4, CSIF0, and I²C01 share the same pin and therefore cannot be used simultaneously. Set UARTC4 in advance, using the PMC4, PFC4, and PMCE4 registers, before use.

Caution The transmit/receive operation of UARTC4, CSIF0, and I²C01 is not guaranteed if these functions are switched during transmission or reception. Be sure to disable the one that is not used.

Figure 16-5. UARTC4, CSIF0 and I²C01 Mode Switch Settings

After reset: 00H R/W Address: FFFFF446H

	7	6	5	4	3	2	1	0
PMC3	PMC37	PMC36	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30

After reset: 00H R/W Address: FFFFF466H

	7	6	5	4	3	2	1	0
PFC3	PFC37Note1	PFC36Note1	PFC35Note2	PFC34	PFC33Note2	PFC32	PFC31	PFC30

After reset: 00H R/W Address: FFFFF706H

	7	6	5	4	3	2	1	0
PFCE3	PFCE37Note1	PFCE36Note1	PFCE35Note2	PFCE34	PFCE33Note2	PFCE32	PFCE31	PFCE30

PMC37Note1	PFCE37Note1	PFC37Note1	Operation mode
0	×	×	Port I/O mode
1	0	0	RXDC3 (UARTC3)
1	0	1	SDA00 (I²C00)
1	1	0	CRXD0 (CAN0)Note3

PMC36Note1	PFCE36Note1	PFC36Note1	Operation mode
0	×	×	Port I/O mode
1	0	0	TXDC3 (UARTC3)
1	0	1	SCL00 (I²C00)
1	1	0	CTXD0 (CAN0)Note3

Notes1. V850ES/JC3-H (48 pin), V850ES/JE3-H only

2. V850ES/JE3-H only

3. μPD70F3819, 70F3825 only

Remark × = don't care

19.5.2 Register access type

Table 19-16. Register Access Types (1/17)

Address	Register Name	Symbol	R/W	Bit Manipulation Units			After Reset
				1 Bit	8 Bits	16 Bits	
03FEC000H	CAN0 global control register	C0GMCTRL	R/W			√	0000H
03FEC002H	CAN0 global clock selection register	C0GMCS			√		0FH
03FEC006H	CAN0 global automatic block transmission register	C0GMABT				√	0000H
03FEC008H	CAN0 global automatic block transmission delay register	C0GMABTD			√		00H
03FEC040H	CAN0 module mask 1 register	C0MASK1L				√	Undefined
03FEC042H		C0MASK1H				√	Undefined
03FEC044H	CAN0 module mask 2 register	C0MASK2L				√	Undefined
03FEC046H		C0MASK2H				√	Undefined
03FEC048H	CAN0 module mask 3 register	C0MASK3L				√	Undefined
03FEC04AH		C0MASK3H				√	Undefined
03FEC04CH	CAN0 module mask 4 register	C0MASK4L				√	Undefined
03FEC04EH		C0MASK4H				√	Undefined
03FEC050H	CAN0 module control register	C0CTRL				√	0000H
03FEC052H	CAN0 module last error code register	C0LEC			√		00H
03FEC053H	CAN0 module information register	C0INFO	R		√		00H
03FEC054H	CAN0 module error counter register	C0ERC				√	0000H
03FEC056H	CAN0 module interrupt enable register	C0IE	R/W			√	0000H
03FEC058H	CAN0 module interrupt status register	C0INTS				√	0000H
03FEC05AH	CAN0 module bit-rate prescaler register	C0BRP			√		FFH
03FEC05CH	CAN0 module bit-rate register	C0BTR				√	370FH
03FEC05EH	CAN0 module last in-pointer register	C0LIPT	R		√		Undefined
03FEC060H	CAN0 module receive history list register	C0RGPT	R/W			√	xx02H
03FEC062H	CAN0 module last out-pointer register	C0LOPT	R		√		Undefined
03FEC064H	CAN0 module transmit history list register	C0TGPT	R/W			√	xx02H
03FEC066H	CAN0 module time stamp register	C0TS				√	0000H

(2/2)

(b) Write

Clear TOVF	Setting of TOVF bit
0	TOVF bit is not changed.
1	TOVF bit is cleared to 0.

(18) CAN0 module time stamp register (C0TS)

The C0TS register is used to control the time stamp function.

(1/2)

After reset: 0000H R/W Address: 03FEC066H

(a) Read

	15	14	13	12	11	10	9	8
C0TS	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
	0	0	0	0	0	TSLOCK	TSSEL	TSEN

(b) Write

	15	14	13	12	11	10	9	8
C0TS	0	0	0	0	0	Set TSLOCK	Set TSSEL	Set TSEN
	7	6	5	4	3	2	1	0
	0	0	0	0	0	Clear TSLOCK	Clear TSSEL	Clear TSEN

Remark The lock function of the time stamp functions must not be used when the CAN module is in the normal operation mode with ABT.

(9/13)

Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
00200302H	UF0 configuration/interface/endpoint descriptor register 158	UF0CIE158	R/W		√		Undefined
00200304H	UF0 configuration/interface/endpoint descriptor register 159	UF0CIE159	R/W		√		Undefined
00200306H	UF0 configuration/interface/endpoint descriptor register 160	UF0CIE160	R/W		√		Undefined
00200308H	UF0 configuration/interface/endpoint descriptor register 161	UF0CIE161	R/W		√		Undefined
0020030AH	UF0 configuration/interface/endpoint descriptor register 162	UF0CIE162	R/W		√		Undefined
0020030CH	UF0 configuration/interface/endpoint descriptor register 163	UF0CIE163	R/W		√		Undefined
0020030EH	UF0 configuration/interface/endpoint descriptor register 164	UF0CIE164	R/W		√		Undefined
00200310H	UF0 configuration/interface/endpoint descriptor register 165	UF0CIE165	R/W		√		Undefined
00200312H	UF0 configuration/interface/endpoint descriptor register 166	UF0CIE166	R/W		√		Undefined
00200314H	UF0 configuration/interface/endpoint descriptor register 167	UF0CIE167	R/W		√		Undefined
00200316H	UF0 configuration/interface/endpoint descriptor register 168	UF0CIE168	R/W		√		Undefined
00200318H	UF0 configuration/interface/endpoint descriptor register 169	UF0CIE169	R/W		√		Undefined
0020031AH	UF0 configuration/interface/endpoint descriptor register 170	UF0CIE170	R/W		√		Undefined
0020031CH	UF0 configuration/interface/endpoint descriptor register 171	UF0CIE171	R/W		√		Undefined
0020031EH	UF0 configuration/interface/endpoint descriptor register 172	UF0CIE172	R/W		√		Undefined
00200320H	UF0 configuration/interface/endpoint descriptor register 173	UF0CIE173	R/W		√		Undefined
00200322H	UF0 configuration/interface/endpoint descriptor register 174	UF0CIE174	R/W		√		Undefined
00200324H	UF0 configuration/interface/endpoint descriptor register 175	UF0CIE175	R/W		√		Undefined
00200326H	UF0 configuration/interface/endpoint descriptor register 176	UF0CIE176	R/W		√		Undefined
00200328H	UF0 configuration/interface/endpoint descriptor register 177	UF0CIE177	R/W		√		Undefined
0020032AH	UF0 configuration/interface/endpoint descriptor register 178	UF0CIE178	R/W		√		Undefined
0020032CH	UF0 configuration/interface/endpoint descriptor register 179	UF0CIE179	R/W		√		Undefined

(3/4)

Bit position	Bit name	Function
1	BKI2NK	This bit controls NAK to Endpoint3 (bulk 2 transfer (IN)). 1: Do not transmit NAK. 0: Transmit NAK (default value). This bit is cleared to 0 only when the FIFO connected to the SIE side of the UF0BI2 register (64-byte FIFO of bank configuration) cannot receive data. It is set to 1 when a toggle operation is performed (the data of the UF0BI2 register is retained until transmission has been correctly completed). The bank is changed (toggle operation) when the following conditions are satisfied. • Data is correctly written to the FIFO connected to the CPU bus side (writing has been completed and the FIFO is full or the UF0DEND register is set). • The value of the FIFO counter connected to the SIE side is 0. This bit is automatically set to 1 and data transmission is started when the FIFO on the CPU side becomes full and a FIFO toggle operation is performed as a result of writing data to the FIFO. However, if the FIFO on the CPU side becomes full as a result of writing data to it by DMA while the BKI2T bit of the UF0DEND register is cleared to 0, the toggle operation is not performed because the condition of the toggle operation is not satisfied until the BKI2DED bit of the UF0DEND register is set to 1. To send a short packet that does not make the FIFO on the CPU side full, set the BKI2DED bit to 1 after completing writing data. When the BKI2DED bit is set to 1, a toggle operation is performed and at the same time, this bit is automatically set to 1. This bit is also cleared to 0 as soon as the UF0BI2 register has been cleared.

Cautions 1. If DMA is enabled while data is being written to the UF0BI2 register in the PIO mode, a DMA request is immediately issued.

2. If 64-byte data is written in the DMA transfer mode, the DMA request signal becomes inactive. If the BKI2NK bit is then set to 1, data is transmitted in synchronization with an IN token. The DMA request signal becomes active again as long as the DMA request is not masked as soon as the FIFO is toggled. If the BKI2NK bit is not set, data is not transmitted even if an IN token has been received. In this case, set the BKI2DED bit of the UF0DEND register to 1.

3. If the TC signal is received in the DMA transfer mode, the DMA request signal becomes inactive. At the same time, the DMA request is masked. If the BKI2NK bit is not set to 1, data is not transmitted even if an IN token is received. When the BKI2DED bit of the UF0DEND register is set to 1 by FW, data is transmitted in synchronization with the IN token. To execute DMA transfer again, unmask the DMA request.

(6) UF0 EP4 status register L (UF0E4SL)

This register stores the value that is to be returned in response to the GET_STATUS Endpoint4 request.

This register can be read or written in 8-bit units. Note, however, that data can be written to this register only when the EP0NKA bit is set to 1.

If an error occurs in Endpoint4, the E4HALT bit is set to 1. A write access to this register is ignored while a USB-side access to Endpoint4 is being received.

The hardware automatically transmits the contents of this register to the host when it has received the GET_STATUS Endpoint4 request. If Endpoint4 has stalled, the UF0BO2 register is cleared and the BKO2NK bit is cleared to 0.

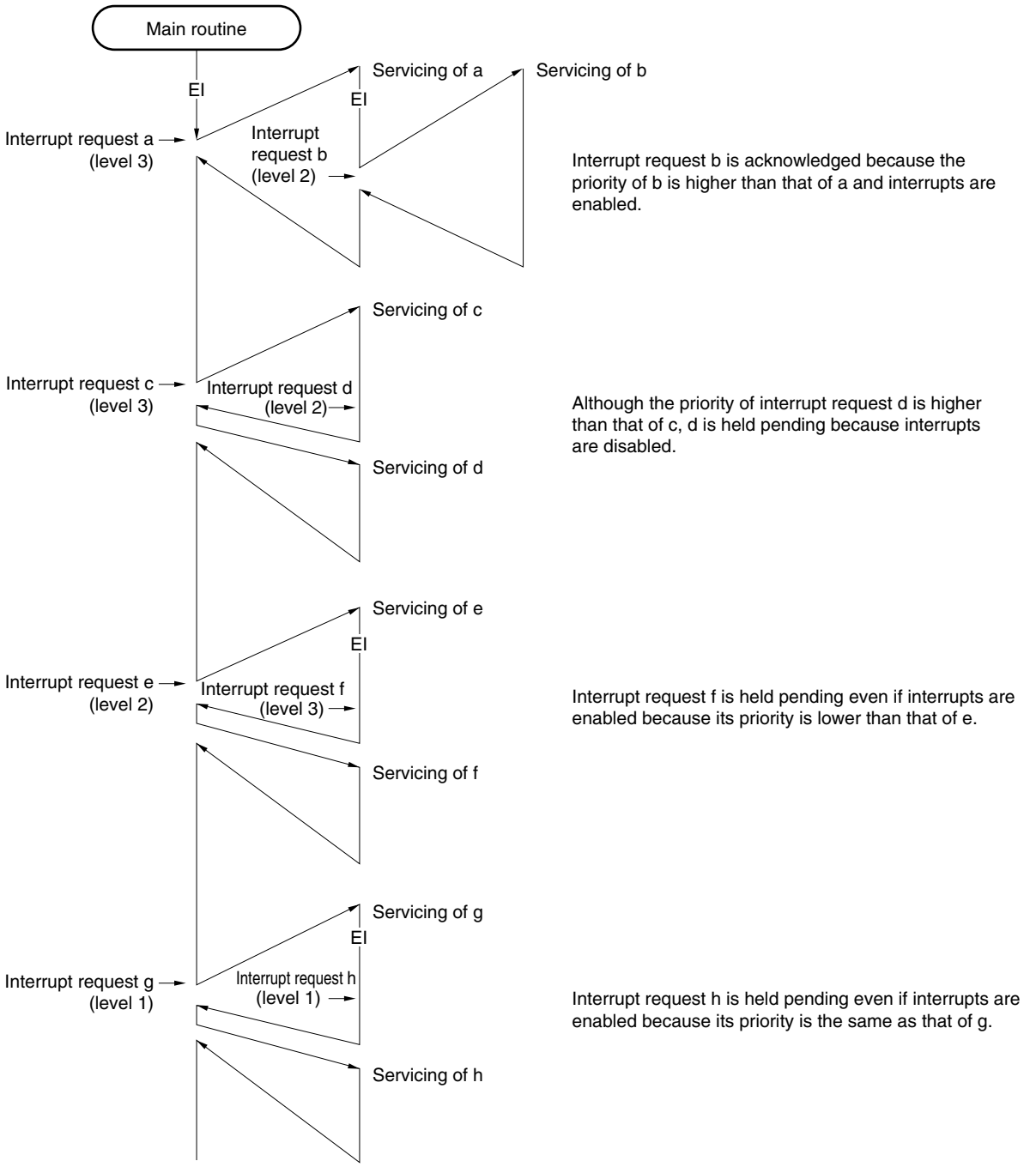
Because writing this register is always masked when transfer to Endpoint4, rather than control transfer, is executed, be sure to check this register to see if data has been correctly written to it.

Caution To rewrite this register, set the EP0NKA bit to 1 before reading the register contents, and rewrite the register contents after confirming that the bit has been set, in order to prevent conflict between a read access and a write access.

	7	6	5	4	3	2	1	0	Address	After reset
UF0E4SL	0	0	0	0	0	0	0	E4HALT	0020015CH	00H

Bit position	Bit name	Function
0	E4HALT	This bit indicates the status of Endpoint4. 1: Stalled 0: Not stalled This bit is set to 1 by hardware when the SET_FEATURE Endpoint4 request has been received. It is cleared to 0 by hardware when the CLEAR_FEATURE Endpoint4 request, SET_CONFIGURATION request, or the SET_INTERFACE request for the Interface to which Endpoint4 is linked has correctly been received. DATA PID is initialized to DATA0.

Figure 22-7. Example of Processing in Which Another Interrupt Request Signal Is Issued While an Interrupt Is Being Serviced (1/2)



Caution To perform multiple interrupt servicing, the values of the EIPC and EIPSW registers must be saved before executing the EI instruction. When returning from multiple interrupt servicing, restore the values of EIPC and EIPSW after executing the DI instruction.

Remarks 1. a to u in the figure are the temporary names of interrupt request signals shown for the sake of explanation.

2. The default priority in the figure indicates the relative priority between two interrupt request signals.

- Port registers when UARTC0 is used

  When UARTC0 is used, port registers are set to make the TXDC0 and RXDC0 pins valid by the debug monitor program. Do not change the following register settings with the user program during debugging. (The same value can be overwritten.)

	7	6	5	4	3	2	1	0
PFC3	×	×	×	×	×	×	0	0
PFCE3	×	×	×	×	×	×	0	0
PMC3	×	×	×	×	×	×	1	1

Remark ×: don't care

- Port registers when CSIF0 is used

  When CSIF0 is used, port registers are set to make the SIF0, SOF0, $\overline{\text{SCKF0}}$, and HS (P913) pins valid by the debug monitor program. Do not change the following register settings with the user program during debugging. (The same value can be overwritten.)

(a) SIF0, SOF0, and $\overline{\text{SCKF0}}$ settings

	7	6	5	4	3	2	1	0
PMC4	×	×	×	×	×	1	1	1
PFC4	×	×	×	×	×	0	0	0
PFCE4	×	×	×	×	×	×	0	0

(b) HS (P913 pin) settings

	15	14	13	12	11	10	9	8
PM9H	×	×	0	×	×	×	×	×
P9H	×	×	**Note**	×	×	×	×	×

Note Writing to this bit is prohibited.
The port values corresponding to the HS pin are changed by the monitor program according to the debugger status. To perform port register settings in 8-bit units, the user program can usually use read-modify-write. If an interrupt for debugging occurs before writing, however, an unexpected operation may be performed.

Remark ×: don't care

32.5.2 Supply current

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = UV_{DD} = AV_{REF0} = AV_{REF1}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current[Notes 1, 2]	I_{DD1}	Normal operation	f_{XX} = 48 MHz (f_X = 6 MHz) Peripheral function operating			60	mA
			f_{XX} = 48 MHz (f_X = 6 MHz) USBF operating		42		mA
	I_{DD2}	HALT mode	f_{XX} = 48 MHz (f_X = 6 MHz) Peripheral function operating		33	42	mA
	I_{DD3}	IDLE1 mode	f_{XX} = 48 MHz (f_X = 6 MHz), PLL on		4	7	mA
	I_{DD4}	IDLE2 mode	f_{XX} = 6 MHz (f_X = 6 MHz), PLL off		0.5	0.8	mA
	I_{DD5}	Subclock operation mode	f_{XT} = 32.768 kHz, main clock stopped, internal oscillator stopped		120	600	μA
	I_{DD6}	Sub-IDLE mode	f_{XT} = 32.768 kHz, main clock stopped, internal oscillator stopped		13	95	μA
	I_{DD7}	STOP mode	Subclock stopped, internal oscillator stopped		10	90	μA
			Subclock operating, internal oscillator stopped		13	95	μA
	I_{DD8}	Flash memory programming mode	f_{XX} = 48 MHz (f_X = 6 MHz)		65	70	mA

Notes 1. Total of V_{DD}, EV_{DD}, and UV_{DD} currents. Currents flowing through the output buffers, A/D converter, D/A converter, and on-chip pull-down resistor are not included.

2. The V_{DD} of the TYP. value is 3.3 V.

APPENDIX C INSTRUCTION SET LIST

C.1 Conventions

(1) Register symbols used to describe operands

Register Symbol	Explanation
reg1	General-purpose registers: Used as source registers.
reg2	General-purpose registers: Used mainly as destination registers. Also used as source register in some instructions.
reg3	General-purpose registers: Used mainly to store the remainders of division results and the higher 32 bits of multiplication results.
bit#3	3-bit data for specifying the bit number
immX	X bit immediate data
dispX	X bit displacement data
regID	System register number
vector	5-bit data that specifies the trap vector (00H to 1FH)
cccc	4-bit data that shows the conditions code
sp	Stack pointer (r3)
ep	Element pointer (r30)
listX	X item register list

(2) Register symbols used to describe opcodes

Register Symbol	Explanation
R	1-bit data of a code that specifies reg1 or regID
r	1-bit data of the code that specifies reg2
w	1-bit data of the code that specifies reg3
d	1-bit displacement data
I	1-bit immediate data (indicates the higher bits of immediate data)
i	1-bit immediate data
cccc	4-bit data that shows the condition codes
CCCC	4-bit data that shows the condition codes of Bcond instruction
bbb	3-bit data for specifying the bit number
L	1-bit data that specifies a program register in the register list

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