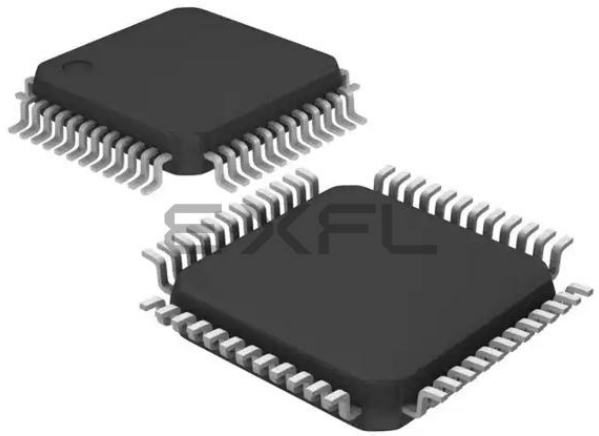
Renesas Electronics America Inc - UPD70F3815GA-GAM-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, CSI, EBI/EMI, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 6x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3815ga-gam-ax

(9) Real-time counter (for watch)

The real-time counter counts the reference time (one second) for watch counting based on the subclock (32.768 kHz) or main clock. This can simultaneously be used as the interval timer based on the main clock. Hardware counters dedicated to year, month, day of week, day, hour, minute, and second are provided, and can count up to 99 years.

(10) Watchdog timer 2

A watchdog timer is provided on chip to detect inadvertent program loops, system abnormalities, etc.
The internal oscillation clock, the main clock, or the subclock can be selected as the source clock.
Watchdog timer 2 generates a non-maskable interrupt request signal (INTWDT2) or a system reset signal (WDT2RES) after an overflow occurs.

(11) Serial interface

The V850ES/JC3-H and V850ES/JE3-H include three kinds of serial interfaces (asynchronous serial interface C (UARTC), 3-wire variable-length serial interface F (CSIF), and an I^2C bus interface (I^2C)), a CAN controller (CAN)[Note1], and a USB function controller (USBF).
UARTC transfers data via the TXDC0, TXDC2 to TXDC4 pins and RXDC0, RXDC2 to RXDC4 pins.
CSIF transfers data via the SOF0, SOF2 to SOF4 pins, SIF0, SIF2 to SIF4 pins, and $\overline{\text{SCKF0}}$, $\overline{\text{SCKF2}}$ to $\overline{\text{SCKF4}}$ pins.
In the case of I^2C, data is transferred via the (SDA00)[Note2] , SDA01 and (SCL00)[Note2] , SCL01 pins.
CAN[Note1] transfers data via the CRXD[Note1] and CTXD0[Note1] pins.
USBF transfers data via the UDMF and UDPF pins.

Notes1. μPD70F3819, 70F3825 only
2. V850ES/JC3-H (48 pin), V850ES/JE3-H only

(12) A/D converter

This 10-bit A/D converter includes 10/6/5 analog input pins. Conversion is performed using the successive approximation method.

(13) D/A converter (V850ES/JC3-H (48 pin), JE3-H only)

A one-channel, 8-bit-resolution D/A converter that uses the R-2R ladder method is provided on chip.

(14) DMA controller

A 4-channel DMA controller is provided on chip. This controller transfers data between the internal RAM, on-chip peripheral I/O devices, and external memory in response to interrupt requests sent by on-chip peripheral I/O devices.

(15) Key interrupt function

A key interrupt request signal (INTKR) can be generated by inputting a falling edge to the key input pins (4 channels).

(16) Real-time output function

The real-time output function transfers preset 4-bit data to output latches upon the occurrence of a timer compare register match signal.

(2) Port 0 mode register (PM0)

(a) V850ES/JC3-H

After reset: FFH R/W Address: FFFFF420H

	7	6	5	4	3	2	1	0
PM0	1	1	1	1	PM03	1	1	1

PM03	I/O mode control
0	Output mode
1	Input mode

(b) V850ES/JE3-H

After reset: FFH R/W Address: FFFFF420H

	7	6	5	4	3	2	1	0
PM0	1	1	1	1	PM03	PM02	1	1

PM0n	I/O mode control (n = 2, 3)
0	Output mode
1	Input mode

4.5.2 Cautions on bit manipulation instruction for port n register (Pn)

When a 1-bit manipulation instruction is executed on a port that provides both input and output functions, the value of the output latch of an input port that is not subject to manipulation may be written in addition to the targeted bit.

Therefore, it is recommended to rewrite the output latch when switching a port from input mode to output mode.

4.5.3 Cautions on on-chip debug pins (V850ES/JC3-H only)

The $\overline{\text{DRST}}$, DCK, DMS, DDI, and DDO pins are on-chip debug pins.

After reset by the $\overline{\text{RESET}}$ pin, the P56/INTP05/$\overline{\text{DRST}}$ pin is initialized to function as an on-chip debug pin ($\overline{\text{DRST}}$). If a high level is input to the $\overline{\text{DRST}}$ pin at this time, the on-chip debug mode is set, and the DCK, DMS, DDI, and DDO pins can be used.

The following action must be taken if on-chip debugging is not used.

- Clear the OCDM0 bit of the OCDM register (special register) (0)

At this time, fix the P56/INTP05/$\overline{\text{DRST}}$ pin to low level from when reset by the $\overline{\text{RESET}}$ pin is released until the above action is taken.

If a high level is input to the $\overline{\text{DRST}}$ pin before the above action is taken, it may cause a malfunction (CPU deadlock). Handle the P56 pin with the utmost care.

Caution After reset by the WDT2RES signal, clock monitor (CLM), or low-voltage detector (LVI), the P56/INTP05/$\overline{\text{DRST}}$ pin is not initialized to function as an on-chip debug pin ($\overline{\text{DRST}}$). The OCDM register holds the current value.

4.5.4 Cautions on P56/INTP05/$\overline{\text{DRST}}$ pin

The P56/INTP05/$\overline{\text{DRST}}$ pin has an internal pull-down resistor (30 kΩ TYP.). After a reset by the $\overline{\text{RESET}}$ pin, a pull-down resistor is connected. The pull-down resistor is disconnected when the OCDM0 bit is cleared (0).

4.5.5 Cautions on P10 and P53 pins when power is turned on

When the power is turned on, the following pins may output an undefined level temporarily even during reset.

- P10/ANO0 pin
- P53/SIF2/KR3/RTP03/DDO pin (V850ES/JC3-H (48 pin), V850ES/JE3-H only)

4.5.6 Hysteresis characteristics

In port mode, the following port pins do not have hysteresis characteristics.

P02, P03
P30 to P37
P40 to P42
P52 to P56
P60 to P65
P92 to P94, P96, P97, P910 to P913

(2/2)

TAAmEEE	Count clock selection
0	Disables operation with external event count input. (Performs counting with the count clock selected by the TAAmCTL0.TAAmCK0 to TAAmCK2 bits.)
1	Enables operation with external event count input. (Performs counting at every valid edge of the external event count input signal.)
The TAAmEEE bit selects whether counting is performed with the internal count clock or the valid edge of the external event count input.	

TAAnMD2	TAAnMD1	TAAnMD0	Timer mode selection
0	0	0	Interval timer mode
0	0	1	External event count mode
0	1	0	External trigger pulse output mode
0	1	1	One-shot pulse output mode
1	0	0	PWM output mode
1	0	1	Free-running timer mode
1	1	0	Pulse width measurement mode
1	1	1	Setting prohibited

Cautions 1. External event count input is selected in the external event count mode regardless of the value of the TAAmEEE bit.

2. Set the TAAmEEE and TAAmMD2 to TAAmMD0 bits when the TAAmCTL0.TAAmCE bit = 0. (The same value can be written when the TAAmCE bit = 1.) The operation is not guaranteed when rewriting is performed with the TAAmCE bit = 1. If rewriting was mistakenly performed, clear the TAAnCE bit to 0 and then set the bits again (m = 0 to 3, 5).

6.6.1 Free-running timer mode (during timer-tuned operation)

This section explains the free-running timer mode of the timer-tuned operation. For the combination of timer-tuned operations, see **Table 6-7**. In this section, an example of timer-tuned operation using TAA1 and TAA0 is shown.

(i) Selecting capture/compare registers

When the free-running timer mode of the timer-tuned operation is used with TAA1 and TAA0 connected to each other, the two capture/compare registers of TAA1 and two capture/compare registers of TAA0 can be used in combination.

How the capture and compare registers are combined is not restricted and can be selected by using the TAAnCCSn bit of the master or slave timer. When the compare register is selected, the set value of the compare register can be rewritten during operation and the rewriting method is anytime write (n = 0, 1).

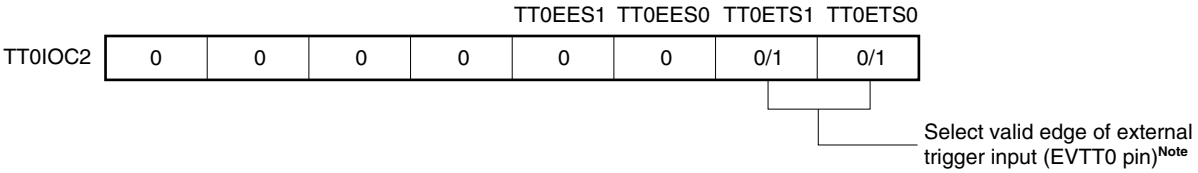
(ii) Overflow

If the counter overflows, an overflow interrupt (INTTAA1OV) of the master timer is generated and the overflow flag (TAA1OVF) is set to “1”.

The overflow interrupt (INTTAA0OV) and overflow flag (TAA0OVF) of the slave timer do not operate and are always at the low level.

Figure 8-27. Setting of Registers in One-Shot Pulse Output Mode (2/2)

(d) TMT0 I/O control register 2 (TT0IOC2)



Note Set the valid edge selection of the unused alternate external input signals to “No edge detection”.

(e) TMT0 counter read buffer register (TT0CNT)

The value of the 16-bit counter can be read by reading the TT0CNT register.

(f) TMT0 capture/compare registers 0 and 1 (TT0CCR0 and TT0CCR1)

If D_0 is set to the TT0CCR0 register and D_1 to the TT0CCR1 register, the active level width and output delay period of the one-shot pulse are as follows.

Active level width = $(D_0 - D_1 + 1) \times$ Count clock cycle

Output delay period = $D_1 \times$ Count clock cycle

Remark TMT0 control register 2 (TT0CTL2), TMT0 I/O control register 1 (TT0IOC1), TMT0 I/O control register 3 (TT0IOC3), TMT0 option register 0 (TT0OPT0), TMT0 option register 1 (TT0OPT1), and TMT0 counter write register (TT0TCW) are not used in the one-shot pulse output mode.

(a) Setting procedure

(i) Setting of high-impedance control operation

<1> Set the HZA0DCMn, HZA0DCNn, and HZA0DCPn bits.

<2> Set the HZA0DCEn bit to 1 (enable high-impedance control).

(ii) Changing setting after enabling high-impedance control operation

<1> Clear the HZA0DCEn bit to 0 (to stop the high-impedance control operation).

<2> Change the setting of the HZA0DCMn, HZA0DCNn, and HZA0DCPn bits.

<3> Set the HZA0DCEn bit to 1 (to enable the high-impedance control operation again).

(iii) Resuming output when pins are in high-impedance state

If the HZA0DCMn bit is 1, set the HZA0DCCn bit to 1 to clear the high-impedance state after the valid edge of the external pin is detected. However, the high-impedance state cannot be cleared unless this bit is set while the input level of the external pin is inactive.

<1> Set the HZA0DCCn bit to 1 (command signal to clear the high-impedance state).

<2> Read the HZA0DCFn bit and check the flag status.

<3> Return to <1> if the HZA0DCFn bit is 1. The input level of the external pin must be checked.
The pin can function as an output pin if the HZA0DCFn bit is 0.

(iv) Making pin go into high-impedance state by software

The HZA0DCTn bit must be set to 1 by software to make the pin go into a high-impedance state while the input level of the external pin is inactive. The following procedure is an example in which the setting is not dependent upon the setting of the HZA0DCMn bit.

<1> Set the HZA0DCTn bit to 1 (high-impedance output command).

<2> Read the HZA0DCFn bit to check the flag status.

<3> Return to <1> if the HZA0DCFn bit is 0. The input level of the external pin must be checked.
The pin is in a high-impedance state if the HZA0DCFn bit is 1.

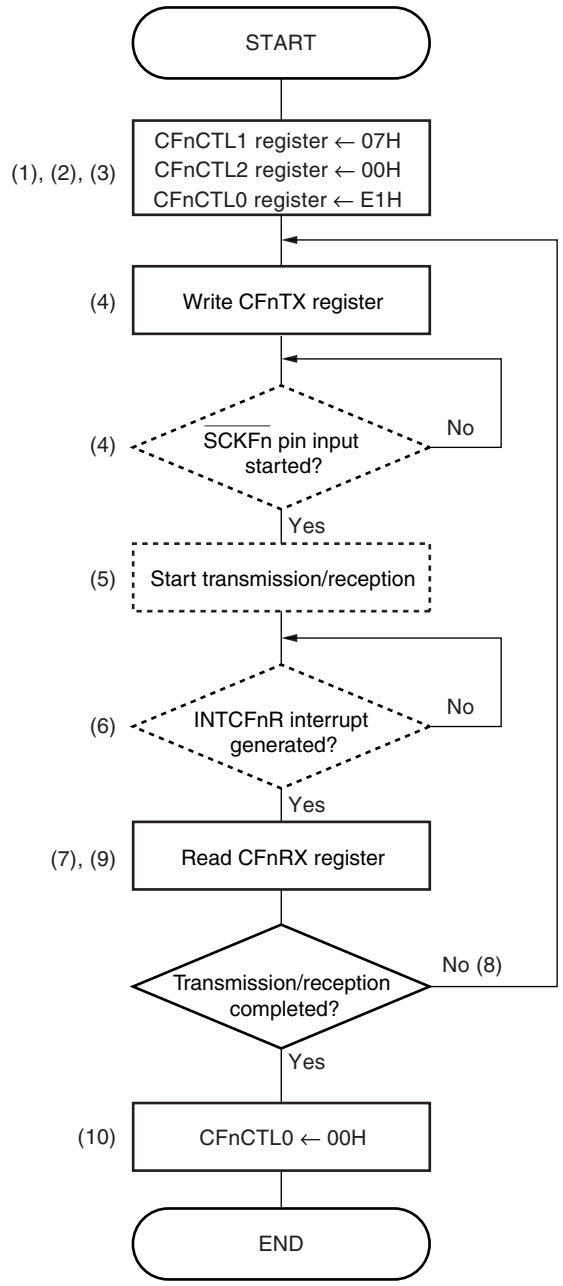
However, if the external pin is not used with the HZA0DCPn bit and HZA0DCNn bit cleared to 0, the pin goes into a high-impedance state when the HZA0DCTn bit is set to 1.

Remark n = 0, 1

17.6.6 Single transfer mode (slave mode, transmission/reception mode)

MSB first (CFnCTL0.CFnDIR bit = 0), communication type 1 (CFnCTL1.CFnCKP and CFnCTL1.CFnDAP bits = 00), communication clock (f_{CCLK}) = external clock ($\overline{SCKFn}$) (CFnCTL1.CFnCKS2 to CFnCTL1.CFnCKS0 bits = 111), transfer data length = 8 bits (CFnCTL2.CFnCL3 to CFnCTL2.CFnCL0 bits = 0000)

(1) Operation flow



Remarks 1. The broken lines indicate the hardware processing.

2. The numbers in this figure correspond to the processing numbers in **(2) Operation timing**.

3. n = 0, 2 to 4

(2) Prescaler compare registers 1 to 3 (PRSCM1 to PRSCM3)

The PRSCM1 to PRSCM3 registers are 8-bit compare registers.

These registers can be read or written in 8-bit units.

Reset sets these registers to 00H.

After reset: 00H R/W Address: PRSCM1 FFFFF321H, PRSCM2 FFFFF325H, PRSCM3 FFFFF329H

	7	6	5	4	3	2	1	0
PRSCMm	PRSCMm7	PRSCMm6	PRSCMm5	PRSCMm4	PRSCMm3	PRSCMm2	PRSCMm1	PRSCMm0

Cautions 1. Do not rewrite the PRSCMm register during operation.

2. Set the PRSCMm register before setting the PRSMm.BGCEm bit to 1.

17.8.1 Baud rate generation

The transmission/reception clock is generated by dividing the main clock. The baud rate generated from the main clock is obtained by the following equation.

$$f_{BRGm} = \frac{f_{XX}}{2^{k+1} \times N}$$

Caution Set f_{BRGm} to 8 MHz, (CSIF0, CSIF2 and CSIF4), 12 MHz (CSIF3), or lower.

Remark f_{BRGm}: BRGm count clock

f_{XX}: Main clock oscillation frequency

k: PRSMm register setting value = 0 to 3

N: PRSCMm register setting value = 1 to 256

However, N = 256 only when the PRSCMm register is set to 00H.

m = 1 to 3

(3) IIC flag registers 0, 1 (IICF0, IICF1)

The IICFn registers set the I²C0n operation mode and indicate the I²C bus status.

These registers can be read or written in 8-bit or 1-bit units. However, the STCFn and IICBSYn bits are read-only.

IICRSVn enables/disables the communication reservation function (see **18.14 Communication Reservation**).

The initial value of the IICBSYn bit is set by using the STCENn bit (see **18.15 Cautions**).

The IICRSVn and STCENn bits can be written only when operation of I²C0n is disabled (IICCn.IICEn bit = 0). After operation is enabled, IICFn can be read.

Reset sets these registers to 00H.

19.7 Bit Set/Clear Function

The CAN control registers include registers whose bits can be set or cleared via the CPU and via the CAN interface. An operation error occurs if the following registers are written directly. Do not write any values directly via bit manipulation, read/modify/write, or direct writing of target values.

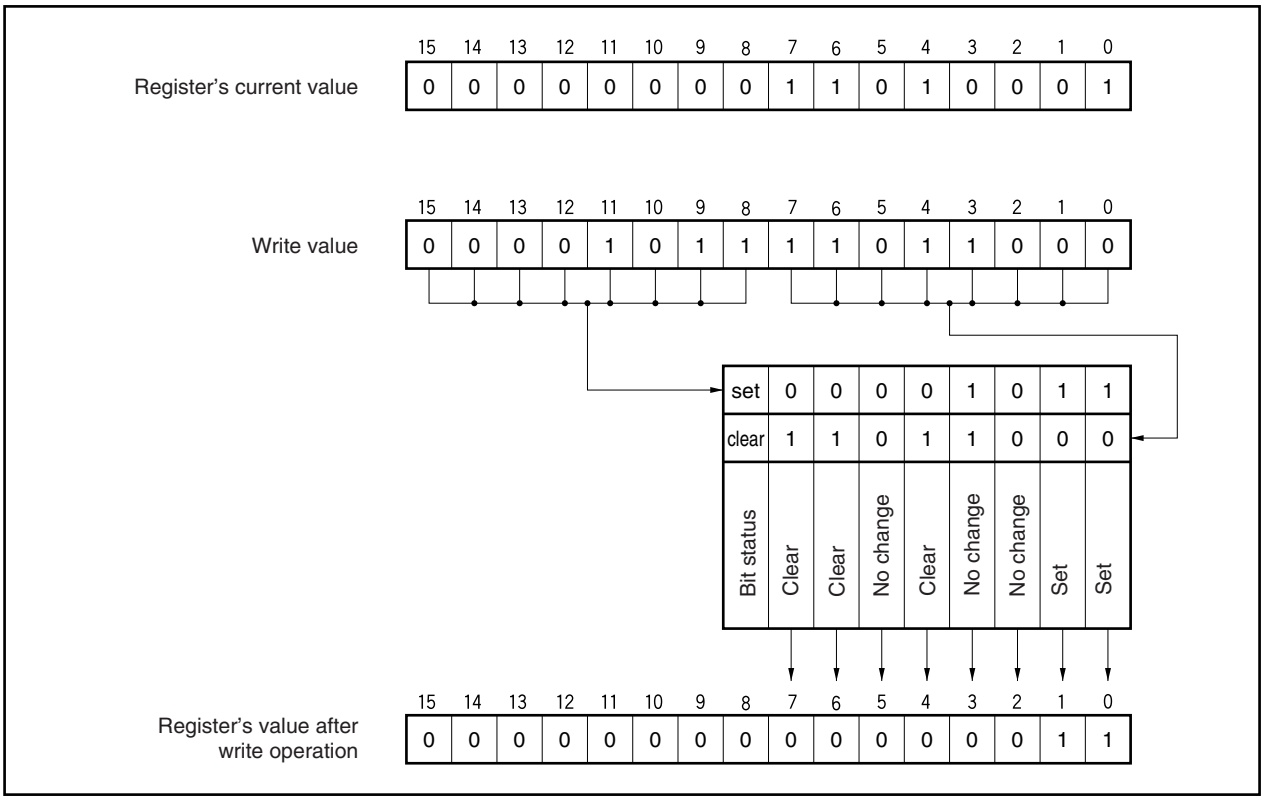
- CAN0 global control register (C0GMCTRL)
- CAN0 global automatic block transmission control register (C0GMABT)
- CAN0 module control register (C0CTRL)
- CAN0 module interrupt enable register (C0IE)
- CAN0 module interrupt status register (C0INTS)
- CAN0 module receive history list register (C0RGPT)
- CAN0 module transmit history list register (C0TGPT)
- CAN0 module time stamp register (C0TS)
- CAN0 message control register (C0MCTRLm)

Remark m = 00 to 31

All the 16 bits in the above registers can be read via the usual method. Use the procedure described in Figure 19-25 below to set or clear the lower 8 bits in these registers.

Setting or clearing of lower 8 bits in the above registers is performed in combination with the higher 8 bits (refer to the bit status after set/clear operation is specified in Figure 19-26). Figure 19-25 shows how the values of set bits or clear bits relate to set/clear/no change operations in the corresponding register.

Figure 19-25. Example of Bit Setting/Clearing Operations



19.15.2 Representative examples of baud rate settings

Tables 19-23 and 19-24 show representative examples of baud rate settings.

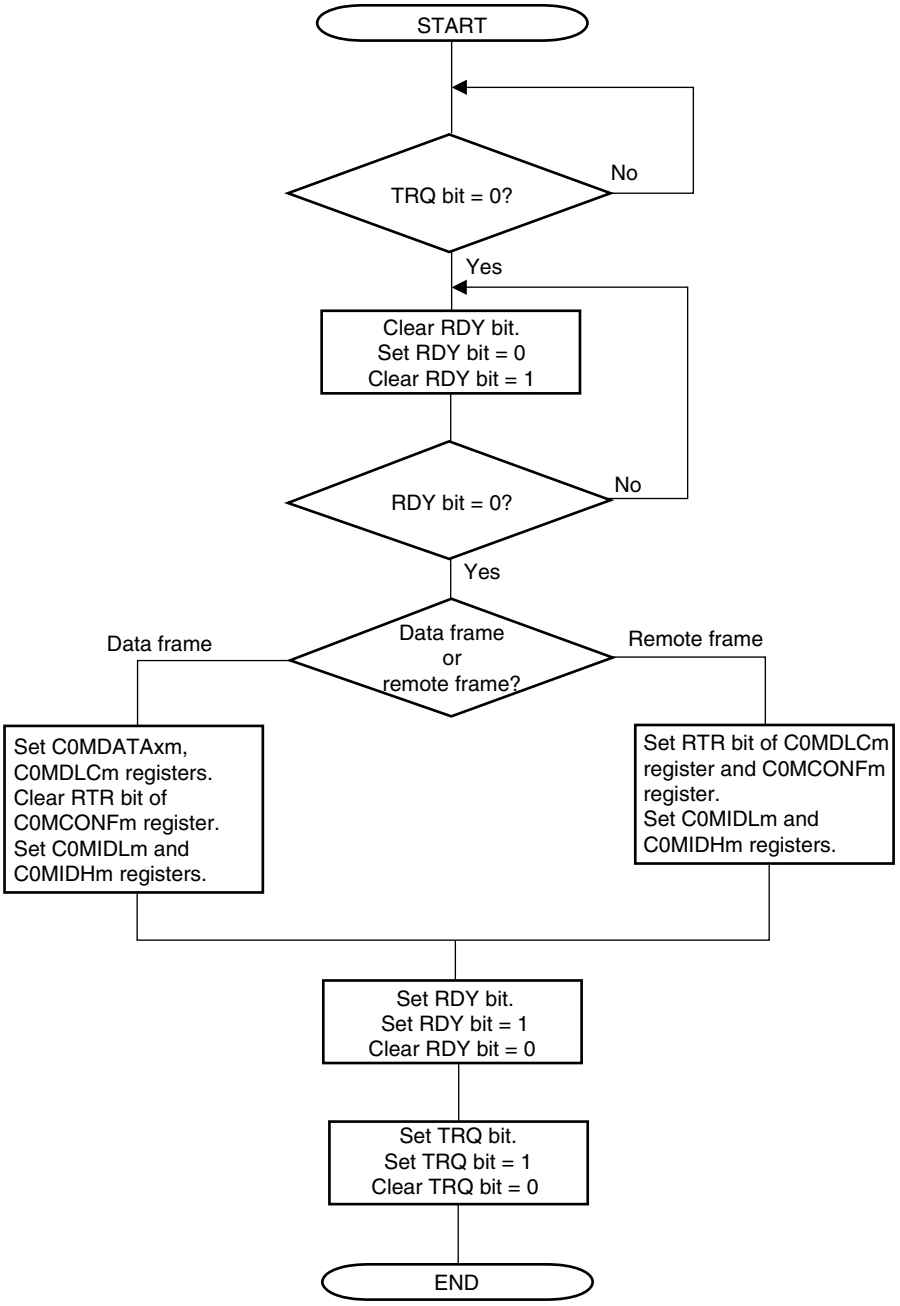
Table 19-23. Representative Examples of Baud Rate Settings (f_{CANMOD} = 8 MHz) (1/2)

Set Baud Rate Value (Unit: kbps)	Division Ratio of C0BRP Register	C0BRP Register Set Value	Valid Bit Rate Setting (Unit: kbps)					C0BTR Register Setting Value		Sampling Point (Unit: %)
			Length of DBT	SYNC SEGMENT	PROP SEGMENT	PHASE SEGMENT1	PHASE SEGMENT2	TSEG13 to TSEG10	TSEG22 to TSEG20	
1000	1	00000000	8	1	1	3	3	0011	010	62.5
1000	1	00000000	8	1	3	2	2	0100	001	75.0
1000	1	00000000	8	1	5	1	1	0101	000	87.5
500	1	00000000	16	1	1	7	7	0111	110	56.3
500	1	00000000	16	1	3	6	6	1000	101	62.5
500	1	00000000	16	1	5	5	5	1001	100	68.8
500	1	00000000	16	1	7	4	4	1010	011	75.0
500	1	00000000	16	1	9	3	3	1011	010	81.3
500	1	00000000	16	1	11	2	2	1100	001	87.5
500	1	00000000	16	1	13	1	1	1101	000	93.8
500	2	00000001	8	1	1	3	3	0011	010	62.5
500	2	00000001	8	1	3	2	2	0100	001	75.0
500	2	00000001	8	1	5	1	1	0101	000	87.5
250	2	00000001	16	1	1	7	7	0111	110	56.3
250	2	00000001	16	1	3	6	6	1000	101	62.5
250	2	00000001	16	1	5	5	5	1001	100	68.8
250	2	00000001	16	1	7	4	4	1010	011	75.0
250	2	00000001	16	1	9	3	3	1011	010	81.3
250	2	00000001	16	1	11	2	2	1100	001	87.5
250	2	00000001	16	1	13	1	1	1101	000	93.8
250	4	00000011	8	1	3	2	2	0100	001	75.0
250	4	00000011	8	1	5	1	1	0101	000	87.5
125	4	00000011	16	1	1	7	7	0111	110	56.3
125	4	00000011	16	1	3	6	6	1000	101	62.5
125	4	00000011	16	1	5	5	5	1001	100	68.8
125	4	00000011	16	1	7	4	4	1010	011	75.0
125	4	00000011	16	1	9	3	3	1011	010	81.3
125	4	00000011	16	1	11	2	2	1100	001	87.5
125	4	00000011	16	1	13	1	1	1101	000	93.8
125	8	00000111	8	1	3	2	2	0100	001	75.0
125	8	00000111	8	1	5	1	1	0101	000	87.5

Caution The values in Table 19-23 do not guarantee the operation of the network system. Thoroughly check the effect on the network system, taking into consideration oscillation errors and delays of the CAN bus and CAN transceiver.

Figure 19-41 shows the processing for a transmit message buffer (C0MCONFm.MT2 to C0MCONFm.MT0 bits = 000B).

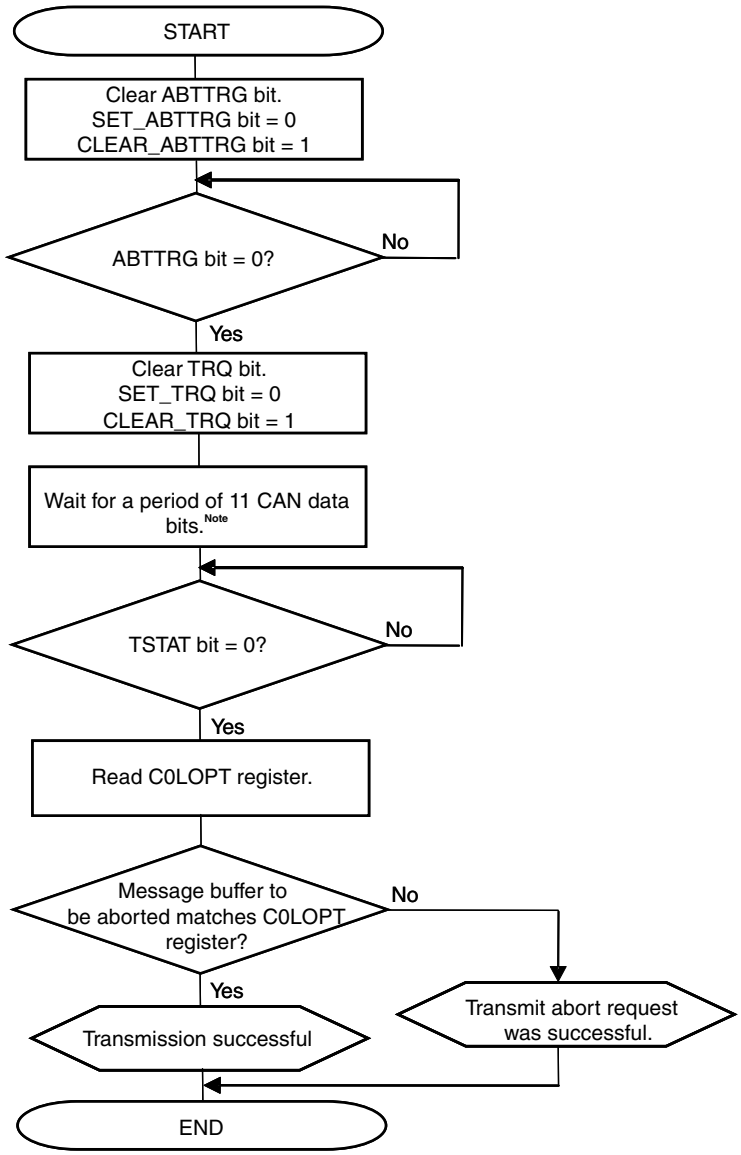
Figure 19-41. Message Transmit Processing



Cautions 1. The TRQ bit should be set after the RDY bit is set.

2. The RDY bit and TRQ bit should not be set at the same time.

Figure 19-47. Transmission Abort Processing Except for ABT Transmission (Normal Operation Mode with ABT)



Note During a period of a total of 11 bits, 3 bits of interframe space and 8 bits of suspend transmission, the transmission request may have already been acknowledged by the protocol layer. Consequently, transmission may not be aborted but started even if the TRQ bit is cleared.

Cautions 1. Execute transmission abort processing by clearing the TRQ bit, not the RDY bit.

2. Before making a sleep mode transition request, confirm that there is no transmission request left using this processing.

3. The TSTAT bit can be periodically checked by a user application or can be checked after the transmit completion interrupt.

4. Do not execute a new transmission request including in the other message buffers while transmission abort processing is in progress.

5. If data of the same message buffer are successively transmitted or if only one message buffer is used, judgments whether transmission has been successfully executed or failed may contradict. In such a case, make a judgment by using the history information of the C0TGPT register.

Notes 3. The SET_FEATURE request sets the UF0 device status register L (UF0DSTL) and UF0 EPn status register L (UF0EnSL) (n = 0 to 4, 7) when ACK is received in the status stage. If the E0HALT bit of the UF0E0SL register is set, a STALL response is made in the status stage or data stage of control transfer for a request other than the GET_STATUS Endpoint0 request, SET_FEATURE Endpoint0 request, and a request generated by the CPUDEC interrupt request, until the CLEAR_FEATURE Endpoint0 request is received. A STALL response to an unsupported request does not set the E0HALT bit of the UF0E0SL register to 1, and the STALL response is cleared as soon as the next SETUP token has been received.

4. If the wValue is not the default value, an automatic STALL response is made.

Cautions 1. The sequence of control transfer defined by the Universal Serial Bus Specification is not satisfied under the following conditions. The operation is not guaranteed under these conditions.

- **If an IN/OUT token is suddenly received without a SETUP stage**
- **If DATA PID1 is sent in the data phase of the SETUP stage**
- **If a token of 128 addresses or more is received**
- **If the request data transmitted in the SETUP stage is of less than 8 bytes**

2. An ACK response is made even when the host transmits data other than a Null packet in the status stage.

3. If the wLength value is 00H during control transfer (read) of FW processing, a Null packet is automatically transmitted for control transfer (without data). The FW request does not automatically transmit a Null packet.

Remarks 1. Df: Default state, Ad: Addressed state, Cf: Configured state

2. n = 0 to 4

It is determined by the setting of the UF0 active interface number register (UF0AIFN) whether a request with Interface number 1 to 4 is correctly responded to, depending on whether the Interface number of the target is valid or not.

3. $$: Valid endpoint number including transfer direction

The valid endpoint is determined by the currently set Alternate Setting number (see **20.6.3 (36) UF0 active alternative setting register (UF0AAS)**, **(38) UF0 endpoint 1 interface mapping register (UF0E1IM)** to **(42) UF0 endpoint 7 interface mapping register (UF0E7IM)**).

4. ? and #: Value transmitted from host (information on Interface numbers 0 to 4)

It is determined by the UF0 active interface number register (UF0AIFN) and UF0 active alternative setting register (UF0AAS) whether an Alternate Setting request corresponding to each Interface number is correctly responded to or not, depending on whether the Interface number and Alternate Setting of the target are valid or not.

Figure 20-8. Operation of UF0BO2 Register (2/2)

(b) Operation example 2

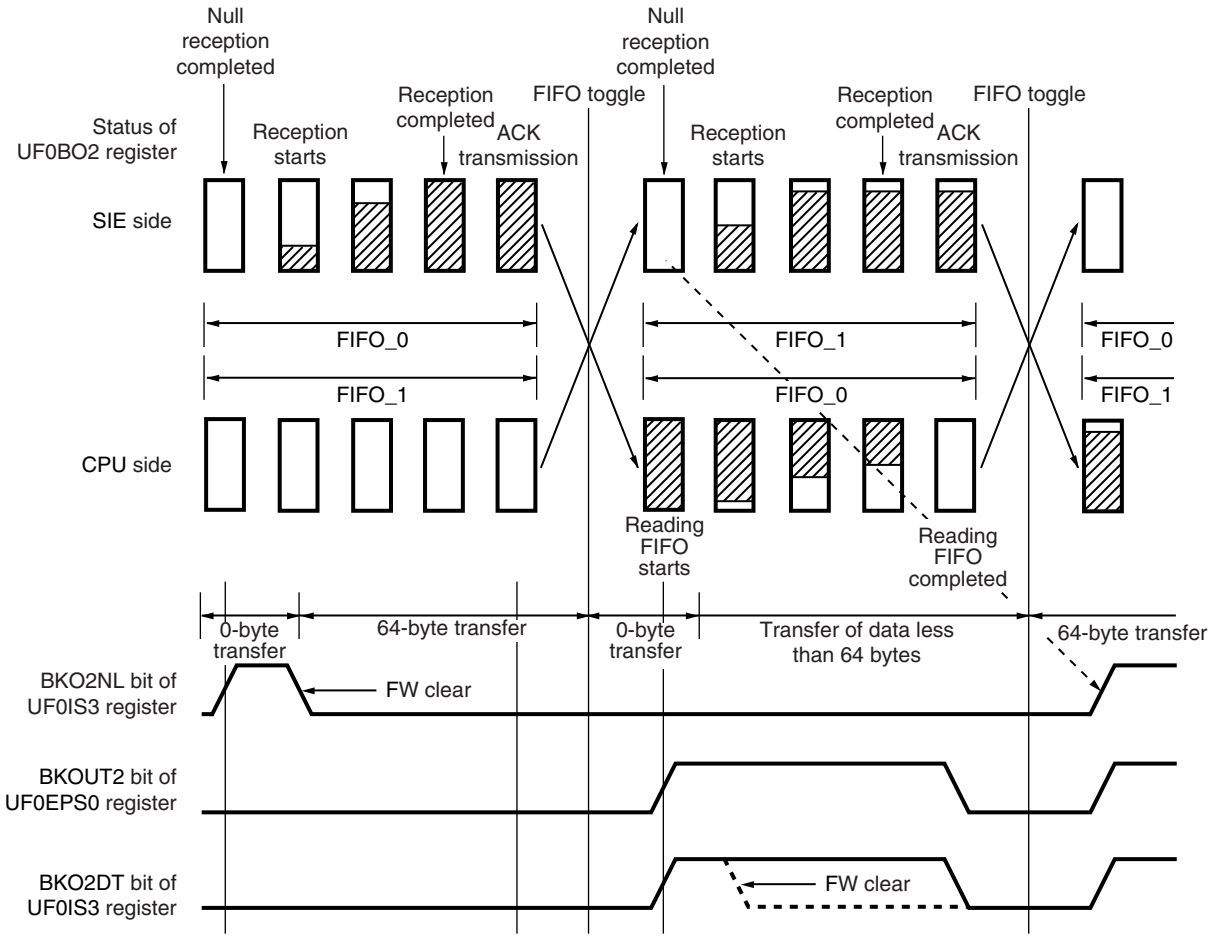
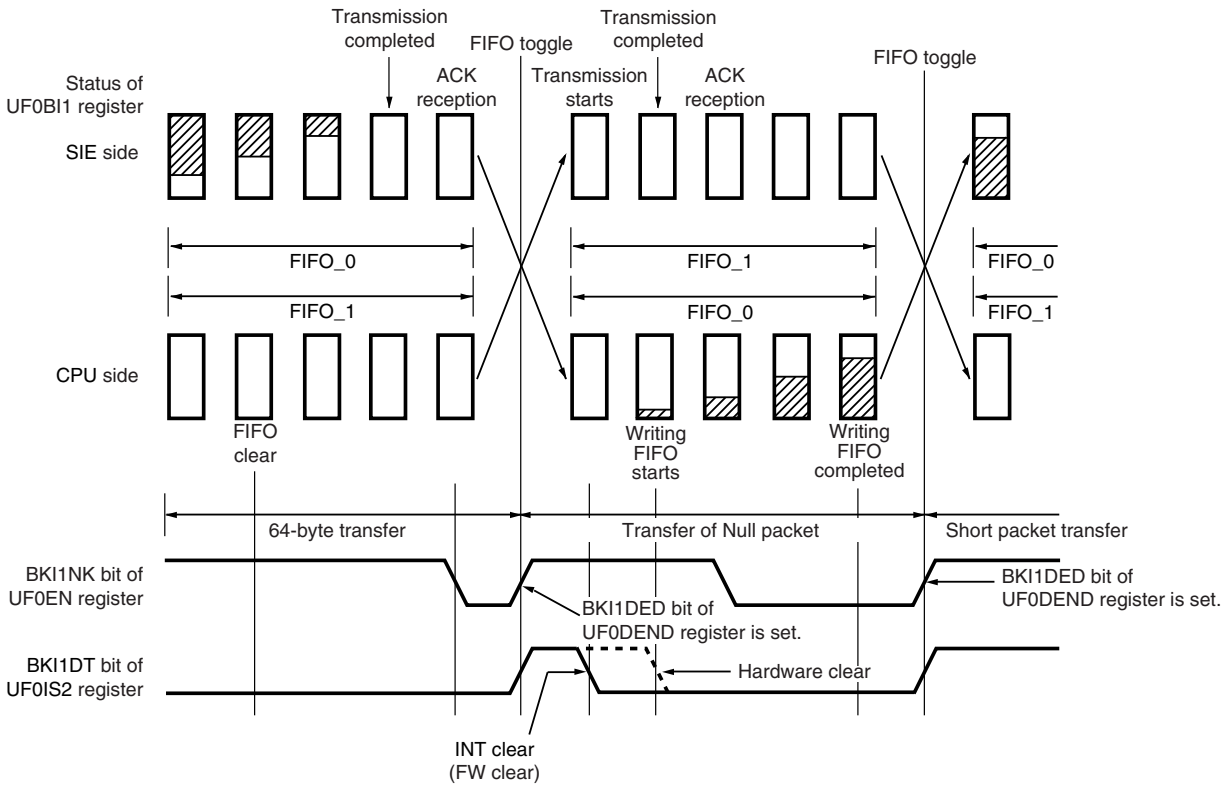


Figure 20-9. Operation of UF0BI1 Register (3/3)

(c) Operation example 3



CHAPTER 26 CLOCK MONITOR

26.1 Functions

The clock monitor samples the main clock by using the internal oscillation clock and generates a reset request signal when oscillation of the main clock is stopped.

Once the operation of the clock monitor has been enabled by an operation enable flag, it cannot be cleared to 0 by any means other than reset.

When a reset by the clock monitor occurs, the RESF.CLMRF bit is set. For details on the RESF register, see **25.2 Registers to Check Reset Source**.

The clock monitor automatically stops under the following conditions.

- During oscillation stabilization time after STOP mode is released
- When the main clock is stopped (from when the PCC.MCK bit = 1 during subclock operation, until the PCC.CLS bit = 0 during main clock operation)
- When the sampling clock (internal oscillation clock) is stopped
- When the CPU operates with the internal oscillation clock

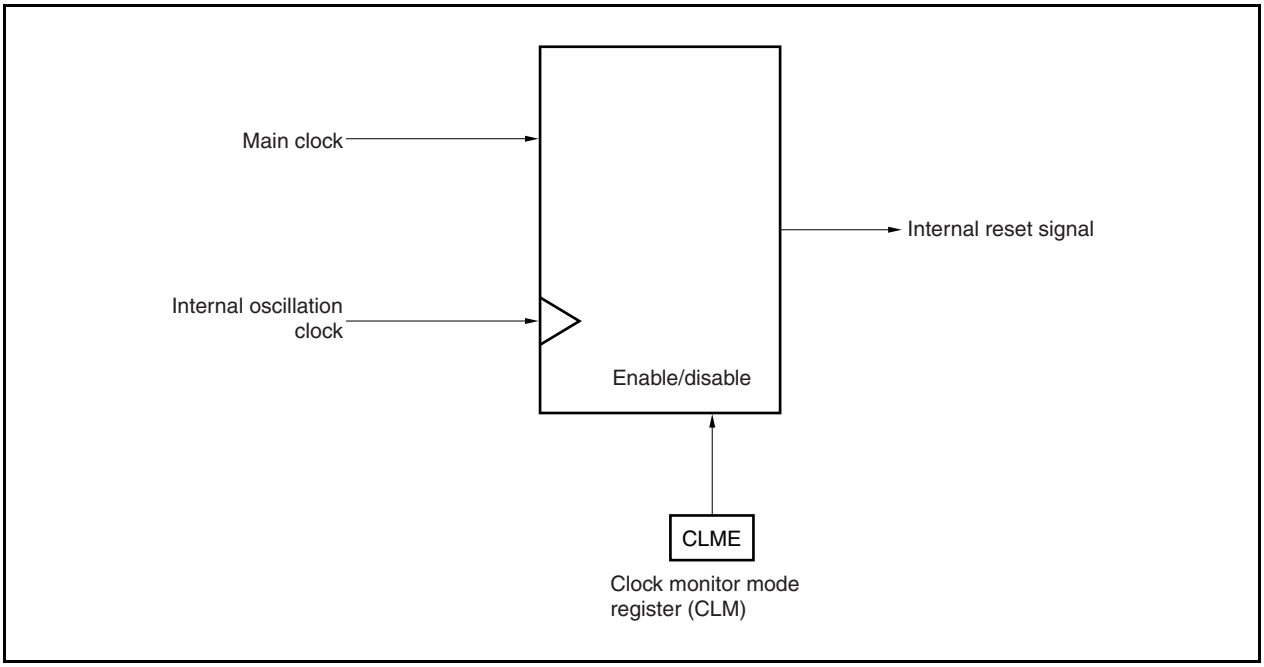
26.2 Configuration

The clock monitor includes the following hardware.

Table 26-1. Configuration of Clock Monitor

Item	Configuration
Control register	Clock monitor mode register (CLM)

Figure 26-1. Timing of Reset via $\overline{\text{RESET}}$ Pin Input



<5>	QB-V850ESJX3H[Note] In-circuit emulator	The in-circuit emulator serves to debug hardware and software when developing application systems using the V850ES/JC3-H or V850ES/JE3-H. It supports the integrated debugger ID850QB. This emulator should be used in combination with a power supply unit and emulation probe. Use the USB interface cable to connect this emulator to the host machine.
<3>	USB interface cable	Cable to connect the host machine and the QB-V850ESJX3H.
<4>	AC adapter	100 to 240 V can be supported by replacing the AC plug.
<9>	Exchange adapter	Adapter to perform pin conversion.
<10>	Check pin adapter	Adapter used in waveform monitoring using the oscilloscope, etc
<11>	Space adapter	Adapter to adjust the height.
<12>	YQ connector	Conversion adapter to connect target connector and exchange adapter.
<13>	Mount adapter	Adapter to mount the V850ES/JC3-H or V850ES/JE3-H on a socket.
<14>	Target connector	Connector to solder on the target system.

Note The QB-V850ESJX3H is supplied with a power supply unit, USB interface cable, and flash memory programmer (MINICUBE2). It is also supplied with integrated debugger ID850QB as control software.

Remark The numbers in the angle brackets correspond to the numbers in Figure A-2.

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Symbol	Name	Unit	Page
UF0CIE212	UF0 configuration/interface/endpoint descriptor register 212	USBF	1118
UF0CIE213	UF0 configuration/interface/endpoint descriptor register 213	USBF	1118
UF0CIE214	UF0 configuration/interface/endpoint descriptor register 214	USBF	1118
UF0CIE215	UF0 configuration/interface/endpoint descriptor register 215	USBF	1118
UF0CIE216	UF0 configuration/interface/endpoint descriptor register 216	USBF	1118
UF0CIE217	UF0 configuration/interface/endpoint descriptor register 217	USBF	1118
UF0CIE218	UF0 configuration/interface/endpoint descriptor register 218	USBF	1118
UF0CIE219	UF0 configuration/interface/endpoint descriptor register 219	USBF	1118
UF0CIE220	UF0 configuration/interface/endpoint descriptor register 220	USBF	1118
UF0CIE221	UF0 configuration/interface/endpoint descriptor register 221	USBF	1118
UF0CIE222	UF0 configuration/interface/endpoint descriptor register 222	USBF	1118
UF0CIE223	UF0 configuration/interface/endpoint descriptor register 223	USBF	1118
UF0CIE224	UF0 configuration/interface/endpoint descriptor register 224	USBF	1118
UF0CIE225	UF0 configuration/interface/endpoint descriptor register 225	USBF	1118
UF0CIE226	UF0 configuration/interface/endpoint descriptor register 226	USBF	1118
UF0CIE227	UF0 configuration/interface/endpoint descriptor register 227	USBF	1118
UF0CIE228	UF0 configuration/interface/endpoint descriptor register 228	USBF	1118
UF0CIE229	UF0 configuration/interface/endpoint descriptor register 229	USBF	1118
UF0CIE230	UF0 configuration/interface/endpoint descriptor register 230	USBF	1118
UF0CIE231	UF0 configuration/interface/endpoint descriptor register 231	USBF	1118
UF0CIE232	UF0 configuration/interface/endpoint descriptor register 232	USBF	1118
UF0CIE233	UF0 configuration/interface/endpoint descriptor register 233	USBF	1118
UF0CIE234	UF0 configuration/interface/endpoint descriptor register 234	USBF	1118
UF0CIE235	UF0 configuration/interface/endpoint descriptor register 235	USBF	1118
UF0CIE236	UF0 configuration/interface/endpoint descriptor register 236	USBF	1118
UF0CIE237	UF0 configuration/interface/endpoint descriptor register 237	USBF	1118
UF0CIE238	UF0 configuration/interface/endpoint descriptor register 238	USBF	1118
UF0CIE239	UF0 configuration/interface/endpoint descriptor register 239	USBF	1118
UF0CIE240	UF0 configuration/interface/endpoint descriptor register 240	USBF	1118
UF0CIE241	UF0 configuration/interface/endpoint descriptor register 241	USBF	1118
UF0CIE242	UF0 configuration/interface/endpoint descriptor register 242	USBF	1118
UF0CIE243	UF0 configuration/interface/endpoint descriptor register 243	USBF	1118
UF0CIE244	UF0 configuration/interface/endpoint descriptor register 244	USBF	1118
UF0CIE245	UF0 configuration/interface/endpoint descriptor register 245	USBF	1118
UF0CIE246	UF0 configuration/interface/endpoint descriptor register 246	USBF	1118
UF0CIE247	UF0 configuration/interface/endpoint descriptor register 247	USBF	1118
UF0CIE248	UF0 configuration/interface/endpoint descriptor register 248	USBF	1118
UF0CIE249	UF0 configuration/interface/endpoint descriptor register 249	USBF	1118
UF0CIE250	UF0 configuration/interface/endpoint descriptor register 250	USBF	1118
UF0CIE251	UF0 configuration/interface/endpoint descriptor register 251	USBF	1118
UF0CIE252	UF0 configuration/interface/endpoint descriptor register 252	USBF	1118