Renesas Electronics America Inc - UPD70F3817GA-GAM-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, CSI, EBI/EMI, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	32
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 6x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3817ga-gam-ax

(1) Port n register (Pn)

Data is input from or output to an external device by writing or reading the Pn register.

The Pn register consists of a port latch that holds output data, and a circuit that reads the status of pins.

Each bit of the Pn register corresponds to one pin of port n, and can be read or written in 1-bit units.

After reset: 00H (output latch) R/W

	7	6	5	7	3	2	1	0
Pn	Pn7	Pn6	Pn5	Pn4	Pn3	Pn2	Pn1	Pn0

Pnm	Control of output data (in output mode)
0	Outputs 0.
1	Outputs 1.

Data is written to or read from the Pn register as follows, regardless of the setting of the PMCn register.

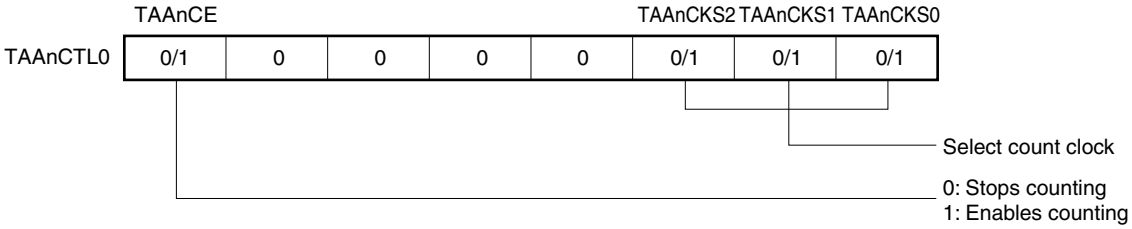
Table 4-7. Writing/Reading Pn Register

Setting of PMn Register	Writing to Pn Register	Reading from Pn Register
Output mode (PMnm = 0)	Data is written to the output latch[Note]. In the port mode (PMCn = 0), the contents of the output latch are output from the pins.	The value of the output latch is read.
Input mode (PMnm = 1)	Data is written to the output latch. The pin status is not affected[Note].	The pin status is read.

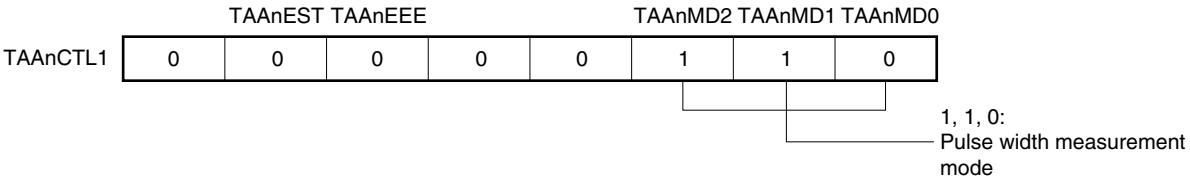
Note The value written to the output latch is retained until a new value is written to the output latch.

Figure 6-41. Register Setting in Pulse Width Measurement Mode

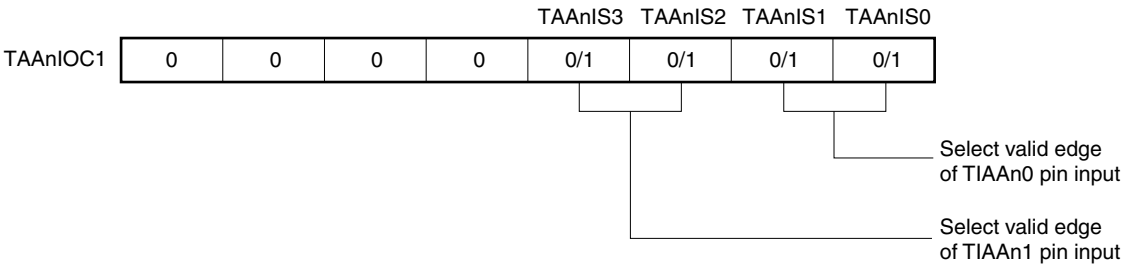
(a) TAAn control register 0 (TAAnCTL0)



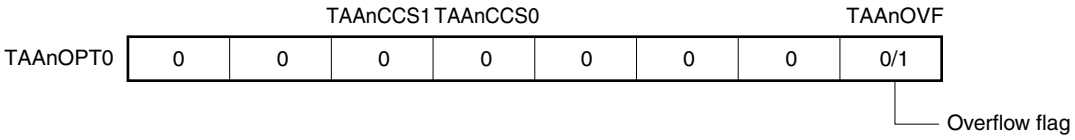
(b) TAAn control register 1 (TAAnCTL1)



(c) TAAn I/O control register 1 (TAAnIOC1)



(d) TAAn option register 0 (TAAnOPT0)



(e) TAAn counter read buffer register (TAAnCNT)

The value of the 16-bit counter can be read by reading the TAAnCNT register.

(f) TAAn capture/compare registers 0 and 1 (TAAnCCR0 and TAAnCCR1)

These registers store the count value of the 16-bit counter when the valid edge input to the TIAAnm pin is detected.

Remarks 1. TAAn I/O control register 0 (TAAnIOC0), and TAAn I/O control register 2 (TAAnIOC2) are not used in the pulse width measurement mode.

2. m = 0, 1
n = 0 to 2

(10) TAB1 capture/compare register 2 (TAB1CCR2)

The TAB1CCR2 register can be used as a capture register or a compare register depending on the mode.

This register can be used as a capture register or a compare register only in the free-running timer mode, according to the setting of the TAB1OPT0.TAB1CCS2 bit. In the pulse width measurement mode, the TAB1CCR2 register can be used only as a capture register. In any other mode, this register can be used only as a compare register.

The TAB1CCR2 register can be read or written during operation.

This register can be read or written in 16-bit units.

Reset sets this register to 0000H.

Caution Accessing the TAB1CCR2 register is prohibited in the following statuses. For details, see 3.4.9 (2) Accessing specific on-chip peripheral I/O registers.

- **When the CPU operates with the subclock and the main clock oscillation is stopped**
- **When the CPU operates with the internal oscillation clock**

After reset: 0000H R/W Address: TAB1CCR2 FFFFF56AH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAB1CCR2																

8.6.9 Encoder count function

The encoder count function includes an encoder compare mode (see **8.6.10 Encoder compare mode (TT0MD3 to TT0MD0 bits = 1000)**).

Mode	TT0CCR0 Register	TT0CCR1 Register
Encoder compare mode	Compare only	Compare only

(1) Count-up/-down control

Counting up or down by the 16-bit counter is controlled by the phase of input encoder signals (TENC00 and TENC01) and settings of the TT0CTL2.TT0UDS1 and TT0CTL2.TT0UDS0 bits.

When the encoder count function is used, the internal count clock and external event count input (EVTT0) cannot be used. Set the TT0CTL0.TT0CKS2 to TT0CTL0.TT0CKS0 bits to 000 and the TT0CTL1.TT0EEE bit to 0.

(2) Setting initial value of 16-bit counter

The initial count value set to the TT0TCW register when the TT0CTL2.TT0ECC bit = 0 is transferred to the 16-bit counter immediately after the counter starts its operation (TT0CTL0.TT0CE bit = 0 → 1), and the counter starts the operation after it detects the valid edge of the encoder input signal (TENC00 or TENC01).

(3) Basic operation

The TT0CCRn register generates a compare match interrupt request signal (INTTT0CCn) when the count value of the 16-bit counter matches the value of the CCRn buffer register.

(4) Clear operation

The 16-bit counter is cleared when the following conditions are satisfied in the encoder compare mode.

- When the value of the 16-bit counter matches the value of the compare register (the TT0CTL2.TT0ECM1 and TT0CTL2.TT0ECM0 bits are set)
- When the edge of the encoder clear input signal (TECR0) is detected (the TT0ECS1 and TT0ECS0 bits are set when the TT0IOC3.TT0SCE bit = 0)
- When the clear level condition of the TENC00, TENC01, and TECR0 pins is detected (the TT0ZCL, TT0BCL, and TT0ACL bits are set when the TT0SCE bit = 1)

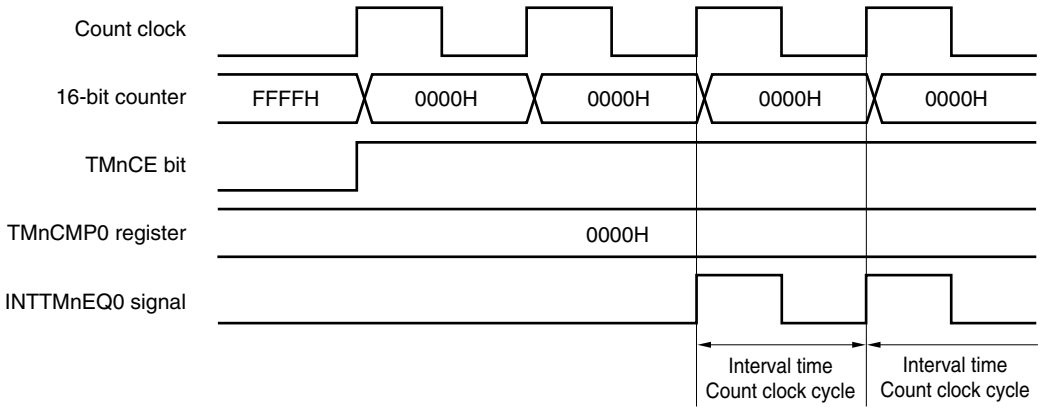
Remark n = 0, 1

(2) Interval timer mode operation timing

Caution Do not set the TMnCMP0 register to FFFFH.

(a) Operation if TMnCMP0 register is set to 0000H

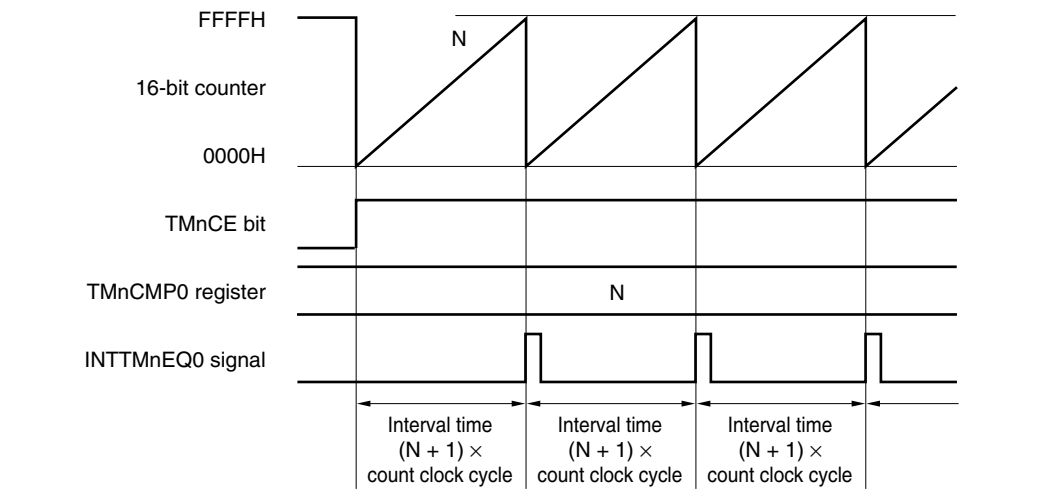
If the TMnCMP0 register is set to 0000H, the INTTMnEQ0 signal is generated at each count clock.
The value of the 16-bit counter is always 0000H.



Remark n = 0 to 3

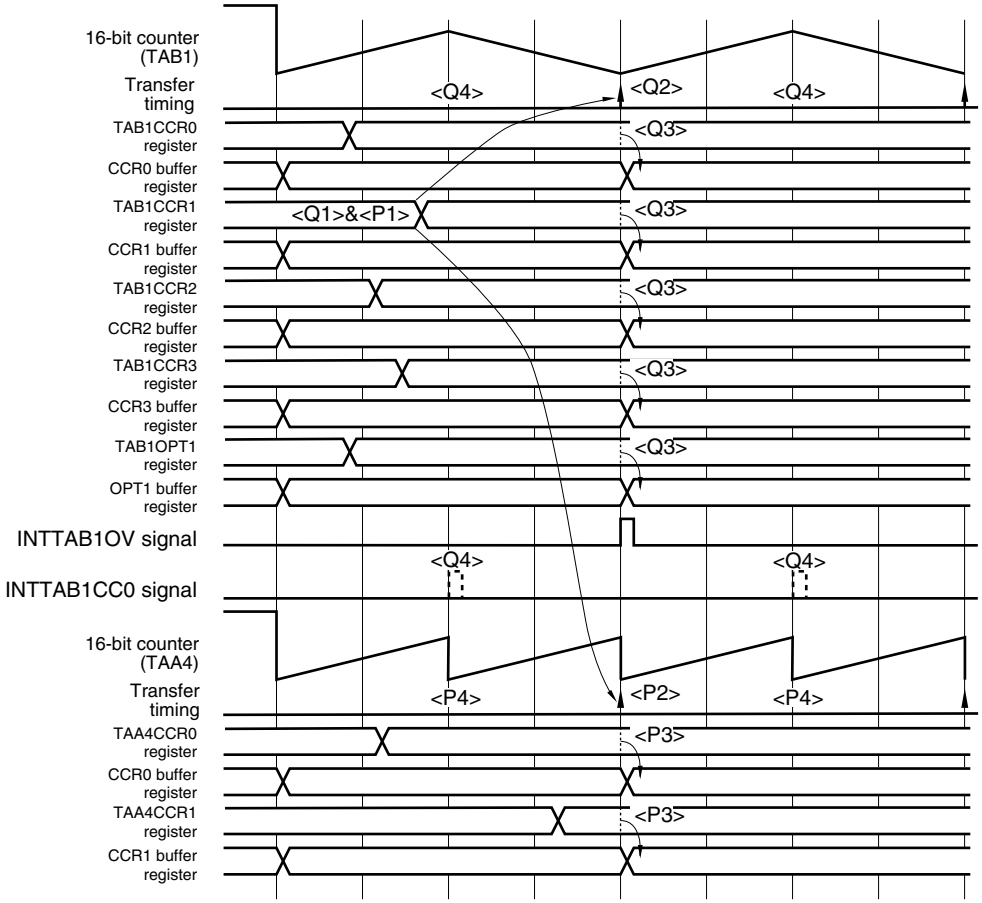
(b) Operation if TMnCMP0 register is set to N

If the TMnCMP0 register is set to N, the 16-bit counter counts up to N. The counter is cleared to 0000H in synchronization with the next count-up timing and the INTTMnEQ0 signal is generated.



Remark n = 0 to 3

Figure 10-31. Basic Operation in Intermittent Batch Rewrite Mode



[TAB1 operation]

<Q1> Write the TAB1CCR1 register.

<Q2> Rewrite the register at the transfer timing that is generated after the TAB1CCR1 register has been rewritten.

<Q3> The registers are transferred all at once at the transfer timing.

<Q4> The transfer timing is also culled as the interrupts are culled.

[TAA4 operation]

<P1> Write the TAB1CCR1 register.

<P2> Rewrite the register at the transfer timing that is generated after the TAB1CCR1 register has been rewritten.

<P3> The registers are transferred all at once at the transfer timing.

<P4> The transfer timing is also culled as the interrupts are culled.

Remark This is an example of the operation when the TAB1OPT1.TAB1ICE bit = 1, TAB1OPT1.TAB1IOE bit = 1, and TAB1OPT1.TAB1ID4 to TAB1OPT1.TAB1ID0 bits = 00001.

16.6 Operation

16.6.1 Data format

Full-duplex serial data reception and transmission is performed.

As shown in Figure 16-7, one data frame of transmit/receive data consists of a start bit, character bits, parity bit, and stop bit(s).

Specification of the character bit length within 1 data frame, parity selection, specification of the stop bit length, and specification of MSB/LSB-first transfer are performed using the UCnCTL0 register.

Moreover, control of UART output/inverted output for the TXDCn bit is performed using the UCnOPT0.UCnTDL bit.

- Start bit.....1 bit
- Character bits.....7 bits/8 bits
- Parity bit .....Even parity/odd parity/0 parity/no parity
- Stop bit .....1 bit/2 bits

Table 19-18. CAN Module Register Bit Configuration (2/2)

Address	Symbol	Bit 7/15	Bit 6/14	Bit 5/13	Bit 4/12	Bit 3/11	Bit 2/10	Bit 1/9	Bit 0/8
03FEC05AH	C0BRP	TQPRS7 to TQPRS0							
03FEC05CH	C0BTR	0	0	0	0	TSEG13 to TSEG10			
03FEC05DH		0	0	SJW1, SJW0		0	TSEG22 to TSEG20		
03FEC05EH	C0LIPT	LIPT7 to LIPT0							
03FEC060H	C0RGPT (W)	0	0	0	0	0	0	0	Clear ROVF
03FEC061H		0	0	0	0	0	0	0	0
03FEC060H	C0RGPT (R)	0	0	0	0	0	0	RHPM	ROVF
03FEC061H		RGPT7 to RGPT0							
03FEC062H	C0LOPT	LOPT7 to LOPT0							
03FEC064H	C0TGPT (W)	0	0	0	0	0	0	0	Clear TOVF
03FEC065H		0	0	0	0	0	0	0	0
03FEC064H	C0TGPT (R)	0	0	0	0	0	0	THPM	TOVF
03FEC065H		TGPT7 to TGPT0							
03FEC066H	C0TS (W)	0	0	0	0	0	Clear TSLOCK	Clear TSSEL	Clear TSEN
03FEC067H		0	0	0	0	0	Set TSLOCK	Set TSSEL	Set TSEN
03FEC066H	C0TS (R)	0	0	0	0	0	TSLOCK	TSSEL	TSEN
03FEC067H		0	0	0	0	0	0	0	0
03FEC068H to 03FEC0FFH	–	Access prohibited (reserved for future use)							

(c) GET_DESCRIPTOR() request

If the subject descriptor has a length that is a multiple of wMaxPacketSize, a Null packet is returned to indicate the end of the data stage. If the length of the descriptor at this time is less than the wLength value, the entire descriptor is returned; if the length of the descriptor is greater than the wLength value, the descriptor up to the wLength value is returned.

- Default state: The value stored in UF0 device descriptor register n (UF0DDn) and UF0 configuration/interface/endpoint descriptor register m (UF0CIEm) is returned (n = 0 to 17, m = 0 to 255) when the GET_DESCRIPTOR() request has been received.
- Addressed state: The value stored in the UF0DDn register and UF0CIEm register is returned when the GET_DESCRIPTOR() request has been received.
- Configured state: The value stored in the UF0DDn register and UF0CIEm register is returned when the GET_DESCRIPTOR() request has been received.

A descriptor of up to 256 bytes can be stored in the UF0CIEm register. To return a descriptor of more than 256 bytes, set the CDCGDST bit of the UF0MODC register to 1 and process the GET_DESCRIPTOR() request by FW.

Store the value of the total number of bytes of the descriptor set by the UF0CIEm register – 1 in the UF0 descriptor length register (UF0DSCL). The transfer data is controlled by the value of this data + 1 and wLength.

(d) GET_INTERFACE() request

If either of wValue and wLength is other than that shown in Table 20-3, or if wIndex is other than that set by the UF0 active interface number register (UF0AIFN), a STALL response is made in the data stage.

- Default state: A STALL response is made in the data stage when the GET_INTERFACE() request has been received.
- Addressed state: A STALL response is made in the data stage when the GET_INTERFACE() request has been received.
- Configured state: The value stored in the UF0 interface n register (UF0IFn) corresponding to the wIndex value is returned (n = 0 to 4) when the GET_INTERFACE() request has been received.

(3) EPC request data register

(1/13)

Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
00200144H	UF0 device status register L	UF0DSTL	R/W		√		00H
0020014CH	UF0 EP0 status register L	UF0E0SL	R/W		√		00H
00200150H	UF0 EP1 status register L	UF0E1SL	R/W		√		00H
00200154H	UF0 EP2 status register L	UF0E2SL	R/W		√		00H
00200158H	UF0 EP3 status register L	UF0E3SL	R/W		√		00H
0020015CH	UF0 EP4 status register L	UF0E4SL	R/W		√		00H
00200168H	UF0 EP7 status register L	UF0E7SL	R/W		√		00H
00200180H	UF0 address register	UF0ADRS	R		√		00H
00200182H	UF0 configuration register	UF0CNF	R		√		00H
00200184H	UF0 interface 0 register	UF0IF0	R		√		00H
00200186H	UF0 interface 1 register	UF0IF1	R		√		00H
00200188H	UF0 interface 2 register	UF0IF2	R		√		00H
0020018AH	UF0 interface 3 register	UF0IF3	R		√		00H
0020018CH	UF0 interface 4 register	UF0IF4	R		√		00H
002001A0H	UF0 descriptor length register	UF0DSCL	R/W		√		00H
002001A2H	UF0 device descriptor register 0	UF0DD0	R/W		√		Undefined
002001A4H	UF0 device descriptor register 1	UF0DD1	R/W		√		Undefined
002001A6H	UF0 device descriptor register 2	UF0DD2	R/W		√		Undefined
002001A8H	UF0 device descriptor register 3	UF0DD3	R/W		√		Undefined
002001AAH	UF0 device descriptor register 4	UF0DD4	R/W		√		Undefined
002001ACH	UF0 device descriptor register 5	UF0DD5	R/W		√		Undefined
002001AEH	UF0 device descriptor register 6	UF0DD6	R/W		√		Undefined
002001B0H	UF0 device descriptor register 7	UF0DD7	R/W		√		Undefined
002001B2H	UF0 device descriptor register 8	UF0DD8	R/W		√		Undefined
002001B4H	UF0 device descriptor register 9	UF0DD9	R/W		√		Undefined
002001B6H	UF0 device descriptor register 10	UF0DD10	R/W		√		Undefined
002001B8H	UF0 device descriptor register 11	UF0DD11	R/W		√		Undefined
002001BAH	UF0 device descriptor register 12	UF0DD12	R/W		√		Undefined
002001BCH	UF0 device descriptor register 13	UF0DD13	R/W		√		Undefined
002001BEH	UF0 device descriptor register 14	UF0DD14	R/W		√		Undefined
002001C0H	UF0 device descriptor register 15	UF0DD15	R/W		√		Undefined
002001C2H	UF0 device descriptor register 16	UF0DD16	R/W		√		Undefined
002001C4H	UF0 device descriptor register 17	UF0DD17	R/W		√		Undefined
002001C6H	UF0 configuration/interface/endpoint descriptor register 0	UF0CIE0	R/W		√		Undefined
002001C8H	UF0 configuration/interface/endpoint descriptor register 1	UF0CIE1	R/W		√		Undefined
002001CAH	UF0 configuration/interface/endpoint descriptor register 2	UF0CIE2	R/W		√		Undefined
002001CCH	UF0 configuration/interface/endpoint descriptor register 3	UF0CIE3	R/W		√		Undefined

(8) UF0 EP status 0 register (UF0EPS0)

This register indicates the USB bus status and the presence or absence of register data.

This register is read-only, in 8-bit units.

The related bits are invalid if each endpoint is not supported by the setting of the UF0EnIM register (n = 1 to 4, 7) and the current setting of the interface.

It takes five USB clocks to reflect the status on this register after the UF0FIC0 and UF0FIC1 registers have been set. If it is necessary to read the status correctly, therefore, separate writing to the UF0FIC0 and UF0FIC1 registers from reading from the UF0EPS0, UF0EPS1, UF0EPS2, UF0E0N, and UF0EN registers by at least four USB clocks.

(1/2)

	7	6	5	4	3	2	1	0	Address	After reset
UF0EPS0	0	IT1	BKOUT2	BKOUT1	BKIN2	BKIN1	EP0W	EP0R	0020000EH	00H

Bit position	Bit name	Function
6	IT1	These bits indicate that data is in the UF0INT1 register (FIFO). By setting the IT1DEND bit of the UF0DEND register to 1, the status in which data is in the UF0INT1 register can be created even if data is not written to the register (Null data transmission). As soon as the IT1DEND bit of the UF0DEND register is set to 1 even when the counter of the UF0INT1 register is 0, this bit is set to 1 by hardware. It is cleared to 0 after correct transmission. 1: Data is in the register. 0: No data is in the register (default value).
5, 4	BKOUTn	These bits indicate that data is in the UF0BOn register (FIFO) connected to the CPU side. When the FIFO configuring the UF0BOn register is toggled, this bit is automatically set to 1 by hardware. It is automatically cleared to 0 by hardware when reading the UF0BOn register (FIFO) connected to the CPU side has been completed (counter value = 0). It is not set to 1 when Null data is received (toggling the FIFO does not take place either). 1: Data is in the register. 0: No data is in the register (default value).
3, 2	BKINn	These bits indicate that data is in the UF0BIn register (FIFO) connected to the CPU side. By setting the BKInDED bit of the UF0DEND register to 1, the status in which data is in the UF0BIn register can be created even if data is not written to the register (Null data transmission). As soon as the BKInDED bit of the UF0DEND register has been set to 1 while the counter of the UF0BIn register is 0, this bit is set to 1 by hardware. It is cleared to 0 when a toggle operation is performed. 1: Data is in the register. 0: No data is in the register (default value).

Remark n = 1, 2

(33) UF0 mode control register (UF0MODC)

This register controls CPUDEC processing.

This register can be read or written in 8-bit units.

By setting each bit of this register, the setting of the UF0MODS register can be changed. The bit of this register is automatically cleared to 0 only at hardware reset and when the MRST bit of the UF0GRP register has been set to 1.

Even if the bit of this register has automatically been set to 1 by hardware, the setting by FW takes precedence.

Be sure to clear bits 7 and 5 to 2 to “0”. If they are set to 1, the operation is not guaranteed.

Caution This register is provided for debugging purposes. Usually, do not set this register except for verifying the operation or when a special mode is used.

	7	6	5	4	3	2	1	0	Address	After reset
UF0MODC	0	CDC GDST	0	0	0	0	0	0	00200074H	00H

Bit position	Bit name	Function
6	CDCGDST	Set this bit to 1 to switch the GET_DESCRIPTOR Configuration request to CPUDEC processing. By setting this bit to 1, the CDCGD bit of the UF0MODS register can be forcibly set to 1. 1: Forcibly change the GET_DESCRIPTOR Configuration request to CPUDEC processing (sets the CDCGD bit of the UF0MODS register to 1). 0: Automatically process the GET_DESCRIPTOR Configuration request (default value).

(2) EPn DMA control register 2 (UF0E1DC2 to UF0E4DC2)

The UF0E1DC2 to UF0E4DC2 register controls the DMA transfer of end point n (EPn). (n = 1 to 4)

The UF0E1DC2 to UF0E4DC2 register can be read or written in 16-bit units.

(1/2)

After reset: 0000H R/W Address: 00200502H

UF0E1DC2

15	14	13	12	11	10	9	8
EP1 TCNT15	EP1 TCNT14	EP1 TCNT13	EP1 TCNT12	EP1 TCNT11	EP1 TCNT10	EP1 TCNT9	EP1 TCNT8

7	6	5	4	3	2	1	0
EP1 TCNT7	EP1 TCNT6	EP1 TCNT5	EP1 TCNT4	EP1 TCNT3	EP1 TCNT2	EP1 TCNT1	EP1 TCNT0

After reset: 0000H R/W Address: 00200506H

UF0E2DC2

15	14	13	12	11	10	9	8
EP2 TCNT15	EP2 TCNT14	EP2 TCNT13	EP2 TCNT12	EP2 TCNT11	EP2 TCNT10	EP2 TCNT9	EP2 TCNT8

7	6	5	4	3	2	1	0
EP2 TCNT7	EP2 TCNT6	EP2 TCNT5	EP2 TCNT4	EP2 TCNT3	EP2 TCNT2	EP2 TCNT1	EP2 TCNT0

After reset: 0000H R/W Address: 0020050AH

UF0E3DC2

15	14	13	12	11	10	9	8
EP3 TCNT15	EP3 TCNT14	EP3 TCNT13	EP3 TCNT12	EP3 TCNT11	EP3 TCNT10	EP3 TCNT9	EP3 TCNT8

7	6	5	4	3	2	1	0
EP3 TCNT7	EP3 TCNT6	EP3 TCNT5	EP3 TCNT4	EP3 TCNT3	EP3 TCNT2	EP3 TCNT1	EP3 TCNT0

After reset: 0000H R/W Address: 0020050EH

UF0E4DC2

15	14	13	12	11	10	9	8
EP4 TCNT15	EP4 TCNT14	EP4 TCNT13	EP4 TCNT12	EP4 TCNT11	EP4 TCNT10	EP4 TCNT9	EP4 TCNT8

7	6	5	4	3	2	1	0
EP4 TCNT7	EP4 TCNT6	EP4 TCNT5	EP4 TCNT4	EP4 TCNT3	EP4 TCNT2	EP4 TCNT1	EP4 TCNT0

Table 22-3. Interrupt Control Register (xxICn) (1/2)

Address	Register	Bit							
		<7>	<6>	5	4	3	2	1	0
FFFFF110H	LVIIC	LVIIF	LVIMK	0	0	0	LVIPR2	LVIPR1	LVIPR0
FFFFF116H	PIC02	PIF02	PMK02	0	0	0	PPR022	PPR021	PPR020
FFFFF11CH	PIC05	PIF05	PMK05	0	0	0	PPR052	PPR051	PPR050
FFFFF120H	PIC07	PIF07	PMK07	0	0	0	PPR072	PPR071	PPR070
FFFFF122H	PIC08	PIF08	PMK08	0	0	0	PPR082	PPR081	PPR080
FFFFF124H	PIC09	PIF09	PMK09	0	0	0	PPR092	PPR091	PPR090
FFFFF126H	PIC10	PIF10	PMK10	0	0	0	PPR102	PPR101	PPR100
FFFFF128H	PIC11	PIF11	PMK11	0	0	0	PPR112	PPR111	PPR110
FFFFF12EH	PIC14	PIF14	PMK14	0	0	0	PPR142	PPR141	PPR140
FFFFF130H	PIC15	PIF15	PMK15	0	0	0	PPR152	PPR151	PPR150
FFFFF132H	PIC16	PIF16	PMK16	0	0	0	PPR162	PPR161	PPR160
FFFFF142H	TAB1OVIC Note	TAB1OVIF	TAB1OVMK	0	0	0	TAB1OVPPR2	TAB1OVPPR1	TAB1OVPPR0
FFFFF144H	TAB1CCIC0 Note	TAB1CCIF0	TAB1CCMK0	0	0	0	TAB1CCPPR02	TAB1CCPPR01	TAB1CCPPR00
FFFFF146H	TAB1CCIC1 Note	TAB1CCIF1	TAB1CCMK1	0	0	0	TAB1CCPPR12	TAB1CCPPR11	TAB1CCPPR10
FFFFF148H	TAB1CCIC2 Note	TAB1CCIF2	TAB1CCMK2	0	0	0	TAB1CCPPR22	TAB1CCPPR21	TAB1CCPPR20
FFFFF14AH	TAB1CCIC3 Note	TAB1CCIF3	TAB1CCMK3	0	0	0	TAB1CCPPR32	TAB1CCPPR31	TAB1CCPPR30
FFFFF14CH	TT0OVIC Note	TT0OVIF	TT0OVMK	0	0	0	TT0OVPPR2	TT0OVPPR1	TT0OVPPR0
FFFFF14EH	TT0CCIC0	TT0CCIF0	TT0CCMK0	0	0	0	TT0CCPPR02	TT0CCPPR01	TT0CCPPR00
FFFFF150H	TT0CCIC1	TT0CCIF1	TT0CCMK1	0	0	0	TT0CCPPR12	TT0CCPPR11	TT0CCPPR10
FFFFF152H	TT0IECIC	TT0IECIF	TT0IECMK	0	0	0	TT0IECPPR2	TT0IECPPR1	TT0IECPPR0
FFFFF154H	TAA0OVIC	TAA0OVIF	TAA0OVMK	0	0	0	TAA0OVPPR2	TAA0OVPPR1	TAA0OVPPR0
FFFFF156H	TAA0CCIC0	TAA0CCIF0	TAA0CCMK0	0	0	0	TAA0CCPPR02	TAA0CCPPR01	TAA0CCPPR00
FFFFF158H	TAA0CCIC1	TAA0CCIF1	TAA0CCMK1	0	0	0	TAA0CCPPR12	TAA0CCPPR11	TAA0CCPPR10
FFFFF15AH	TAA1OVIC	TAA1OVIF	TAA1OVMK	0	0	0	TAA1OVPPR2	TAA1OVPPR1	TAA1OVPPR0
FFFFF15CH	TAA1CCIC0	TAA1CCIF0	TAA1CCMK0	0	0	0	TAA1CCPPR02	TAA1CCPPR01	TAA1CCPPR00
FFFFF15EH	TAA1CCIC1	TAA1CCIF1	TAA1CCMK1	0	0	0	TAA1CCPPR12	TAA1CCPPR11	TAA1CCPPR10
FFFFF160H	TAA2OVIC	TAA2OVIF	TAA2OVMK	0	0	0	TAA2OVPPR2	TAA2OVPPR1	TAA2OVPPR0
FFFFF162H	TAA2CCIC0	TAA2CCIF0	TAA2CCMK0	0	0	0	TAA2CCPPR02	TAA2CCPPR01	TAA2CCPPR00
FFFFF164H	TAA2CCIC1	TAA2CCIF1	TAA2CCMK1	0	0	0	TAA2CCPPR12	TAA2CCPPR11	TAA2CCPPR10
FFFFF178H	TM0EQIC0	TM0EQIF0	TM0EQMK0	0	0	0	TM0EQPR02	TM0EQPR01	TM0EQPR00
FFFFF17AH	TM1EQIC0	TM1EQIF0	TM1EQMK0	0	0	0	TM1EQPR02	TM1EQPR01	TM1EQPR00
FFFFF17CH	TM2EQIC0	TM2EQIF0	TM2EQMK0	0	0	0	TM2EQPR02	TM2EQPR01	TM2EQPR00
FFFFF17EH	TM3EQIC0	TM3EQIF0	TM3EQMK0	0	0	0	TM3EQPR02	TM3EQPR01	TM3EQPR00
FFFFF180H	CF0RIC/ IICIC1	CF0RIF/ IICIF1	CF0RMK/ IICMK1	0	0	0	CF0RPPR2/ IICPPR12	CF0RPPR1/ IICPPR11	CF0RPPR0/ IICPPR10
FFFFF182H	CF0TIC	CF0TIF	CF0TMK	0	0	0	CF0TPPR2	CF0TPPR1	CF0TPPR0
FFFFF188H	CF2RIC	CF2RIF	CF2RMK	0	0	0	CF2RPPR2	CF2RPPR1	CF2RPPR0
FFFFF18AH	CF2TIC	CF2TIF	CF2TMK	0	0	0	CF2TPPR2	CF2TPPR1	CF2TPPR0
FFFFF18CH	CF3RIC	CF3RIF	CF3RMK	0	0	0	CF3RPPR2	CF3RPPR1	CF3RPPR0
FFFFF18EH	CF3TIC	CF3TIF	CF3TMK	0	0	0	CF3TPPR2	CF3TPPR1	CF3TPPR0
FFFFF190H	CF4RIC	CF4RIF	CF4RMK	0	0	0	CF4RPPR2	CF4RPPR1	CF4RPPR0
FFFFF192H	CF4TIC	CF4TIF	CF4TMK	0	0	0	CF4TPPR2	CF4TPPR1	CF4TPPR0

Note V850ES/JE3-H only

CHAPTER 24 STANDBY FUNCTION

24.1 Overview

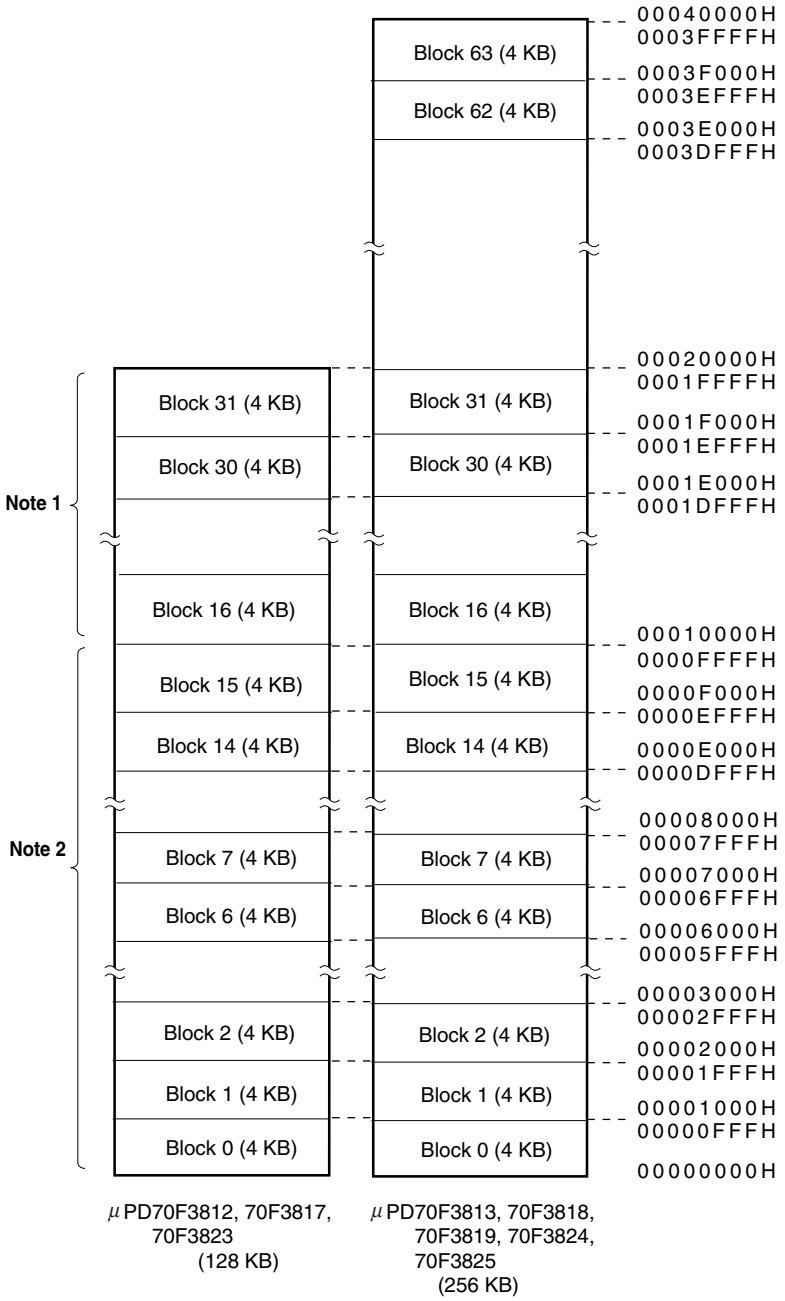
The power consumption of the system can be effectively reduced by using the standby modes in combination and selecting the appropriate mode for the application. The available standby modes are listed in Table 24-1.

Table 24-1. Standby Modes

Mode	Functional Outline
HALT mode	Mode in which only the operating clock of the CPU is stopped
IDLE1 mode	Mode in which all the operations of the internal circuits except the oscillator, PLL[Note], and flash memory are stopped
IDLE2 mode	Mode in which all the operations of internal circuits except the oscillator are stopped
STOP mode	Mode in which all the operations of internal circuits except the subclock oscillator are stopped
Subclock operation mode	Mode in which the subclock is used as the internal system clock
Sub-IDLE mode	Mode in which all the operations of internal circuits except the oscillator are stopped, in the subclock operation mode

Note The PLL holds the previous operating status.

Figure 30-1. Flash Memory Mapping (2/2)



Notes 1. Area to be replaced with the boot area by the boot swap function

2. Boot area

Table 30-6. Wiring of V850ES/JC3-H (40 pin) Flash Writing Adapters (2/2)

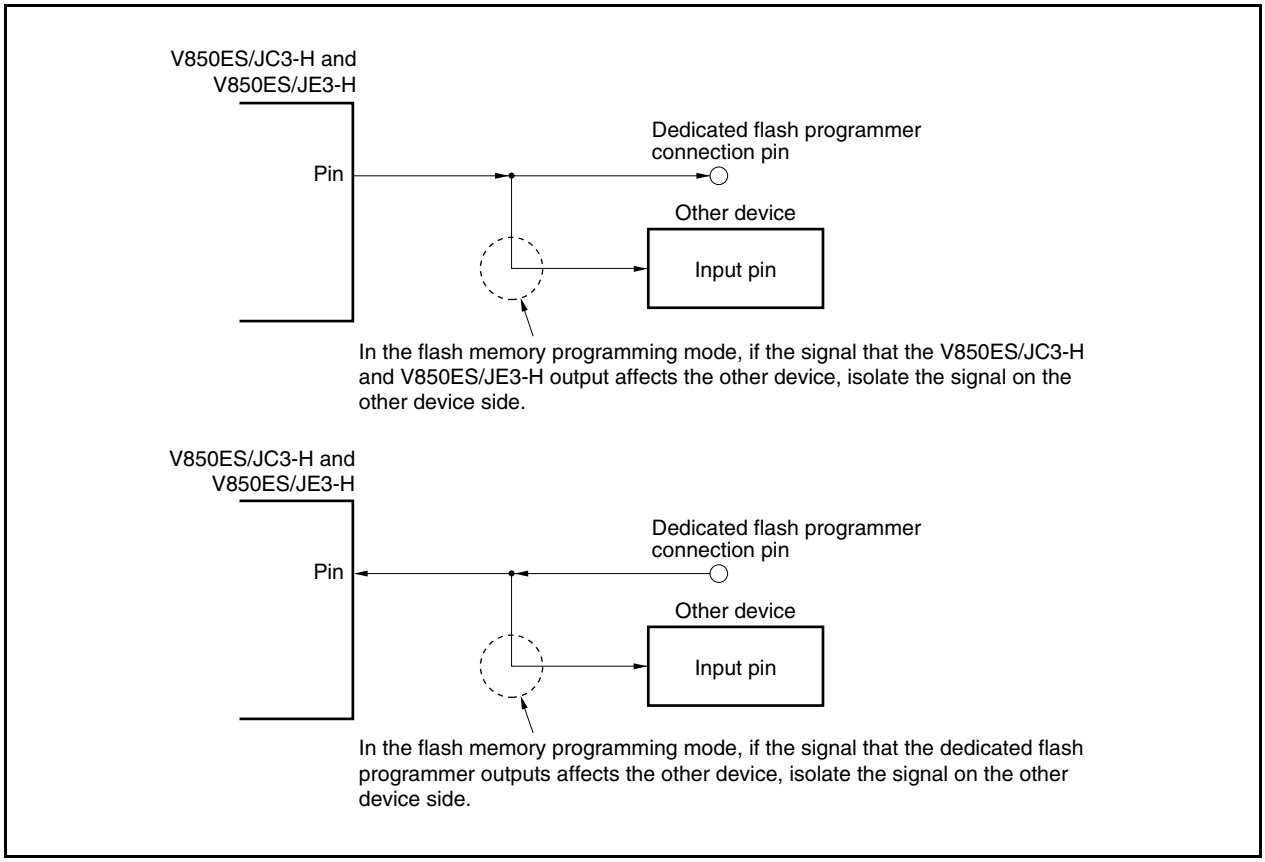
Pin No.	Pin Name	Recommended Connection
29	P96/TIAA21/TOAA21/INTP11	-
30	P97/SIF1/TIAA20/TOAA20	-
31	PDL5/FLMD1	Connect to FLMD1 (output) pin of the programmer
32	P910/SIF3/TXDC2/INTP14	When CSI (CSIF3) is used : connect to SO (output) pin of the programmer When CSI (CSIF3) is not used : pull-down[Note]
33	P911/SOF3/RXDC2/INTP15	When CSI (CSIF3) is used : connect to SI (input) pin of the programmer When CSI (CSIF3) is not used : pull-down[Note]
34	P912/$\overline{\text{SCKF3}}$	When CSI (CSIF3) is used : connect to SCK (output) pin of the programmer When CSI (CSIF3) is not used : pull-down[Note]
35	P913/TOAB1OFF/INTP16 (HS)	When CSI-HS (CSIF3) is used : connect to H/S (input) pin of the programmer When CSI-HS (CSIF3) is not used : pull-down[Note]
36	P74/ANI4	-
37	P73/ANI3	-
38	P72/ANI2	-
39	P71/ANI1	-
40	P70/ANI0	-

Note Independently connect to V_{SS} or V_{DD} via a resistor.

(b) Malfunction of other device

When the dedicated flash programmer (output or input) is connected to a serial interface pin (input or output) that is connected to another device (input), the signal is output to the other device, causing the device to malfunction. To avoid this, isolate the connection to the other device.

Figure 30-15. Malfunction of Other Device



(11) D/A converter

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = UV_{DD} = AV_{REF0} = AV_{REF1}, 3.0 V ≤ AV_{REF1} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Overall error[Note 1]		R = 2 MΩ			±1.2	%FSR
Settling time		C = 20 pF			3	μs
Output resistor	R_O	Output data 55H		6.42		kΩ
Reference voltage	AV_{REF1}		3.0		3.6	V
AV_{REF1} current[Note 2]	AI_{REF1}	D/A conversion operating		1	2.5	mA
		D/A conversion stopped			5	μA

Notes 1. Excluding quantization error (±0.5 %LSB).

2. Value of 1 channel of D/A converter

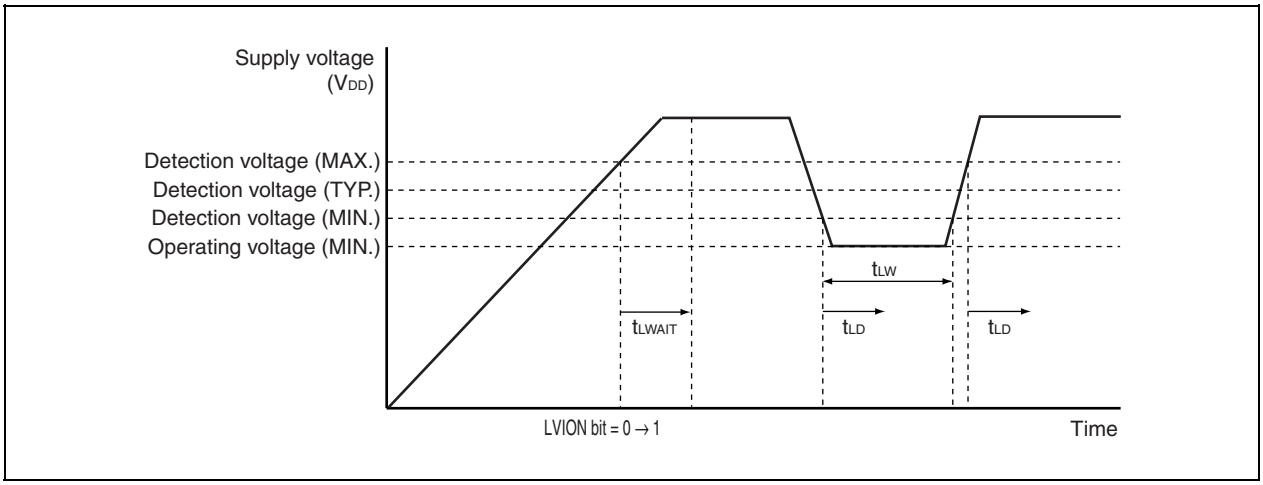
Remark R is the output pin load resistance and C is the output pin load capacitance.

(12) LVI circuit characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = UV_{DD} = AV_{REF0} = AV_{REF1}, V_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LVI0}		2.85	2.95	3.05	V
Response time[Note]	t_{LD}	After V_{DD} reaches V_{LVI0} (MAX.), or after V_{DD} has dropped to V_{LVI0} (MAX.)		0.2	2.0	ms
Minimum pulse width	t_{LW}		0.2			ms
Reference voltage stabilization wait time	t_{LWAIT}	After V_{DD} reaches 2.85 V(MIN.)		0.1	0.2	ms

Note Time required to detect the detection voltage and output an interrupt or reset signal.



(11/34)

Symbol	Name	Unit	Page
C0MDATA522	CAN0 message data byte 5 register 22	CAN	920
C0MDATA523	CAN0 message data byte 5 register 23	CAN	920
C0MDATA524	CAN0 message data byte 5 register 24	CAN	920
C0MDATA525	CAN0 message data byte 5 register 25	CAN	920
C0MDATA526	CAN0 message data byte 5 register 26	CAN	920
C0MDATA527	CAN0 message data byte 5 register 27	CAN	920
C0MDATA528	CAN0 message data byte 5 register 28	CAN	920
C0MDATA529	CAN0 message data byte 5 register 29	CAN	920
C0MDATA530	CAN0 message data byte 5 register 30	CAN	920
C0MDATA531	CAN0 message data byte 5 register 31	CAN	920
C0MDATA600	CAN0 message data byte 6 register 00	CAN	920
C0MDATA601	CAN0 message data byte 6 register 01	CAN	920
C0MDATA602	CAN0 message data byte 6 register 02	CAN	920
C0MDATA603	CAN0 message data byte 6 register 03	CAN	920
C0MDATA604	CAN0 message data byte 6 register 04	CAN	920
C0MDATA605	CAN0 message data byte 6 register 05	CAN	920
C0MDATA606	CAN0 message data byte 6 register 06	CAN	920
C0MDATA607	CAN0 message data byte 6 register 07	CAN	920
C0MDATA608	CAN0 message data byte 6 register 08	CAN	920
C0MDATA609	CAN0 message data byte 6 register 09	CAN	920
C0MDATA610	CAN0 message data byte 6 register 10	CAN	920
C0MDATA611	CAN0 message data byte 6 register 11	CAN	920
C0MDATA612	CAN0 message data byte 6 register 12	CAN	920
C0MDATA613	CAN0 message data byte 6 register 13	CAN	920
C0MDATA614	CAN0 message data byte 6 register 14	CAN	920
C0MDATA615	CAN0 message data byte 6 register 15	CAN	920
C0MDATA616	CAN0 message data byte 6 register 16	CAN	920
C0MDATA617	CAN0 message data byte 6 register 17	CAN	920
C0MDATA618	CAN0 message data byte 6 register 18	CAN	920
C0MDATA619	CAN0 message data byte 6 register 19	CAN	920
C0MDATA620	CAN0 message data byte 6 register 20	CAN	920
C0MDATA621	CAN0 message data byte 6 register 21	CAN	920
C0MDATA622	CAN0 message data byte 6 register 22	CAN	920
C0MDATA623	CAN0 message data byte 6 register 23	CAN	920
C0MDATA624	CAN0 message data byte 6 register 24	CAN	920
C0MDATA625	CAN0 message data byte 6 register 25	CAN	920
C0MDATA626	CAN0 message data byte 6 register 26	CAN	920
C0MDATA627	CAN0 message data byte 6 register 27	CAN	920
C0MDATA628	CAN0 message data byte 6 register 28	CAN	920
C0MDATA629	CAN0 message data byte 6 register 29	CAN	920
C0MDATA630	CAN0 message data byte 6 register 30	CAN	920