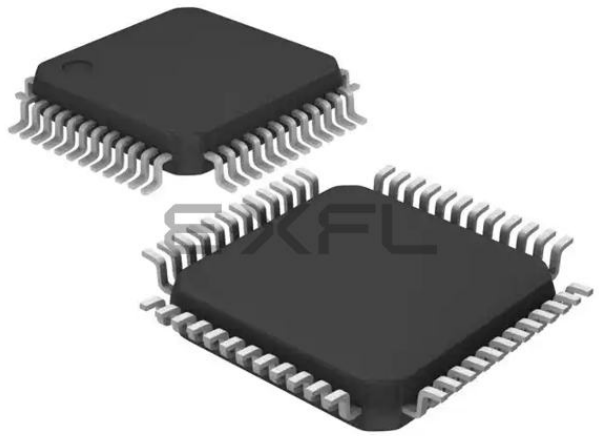
Renesas Electronics America Inc - UPD70F3819GA-GAM-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, CSI, EBI/EMI, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	32
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 6x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3819ga-gam-ax

Figure 4-1. Port Configuration Diagram (V850ES/JC3-H (40 pin))

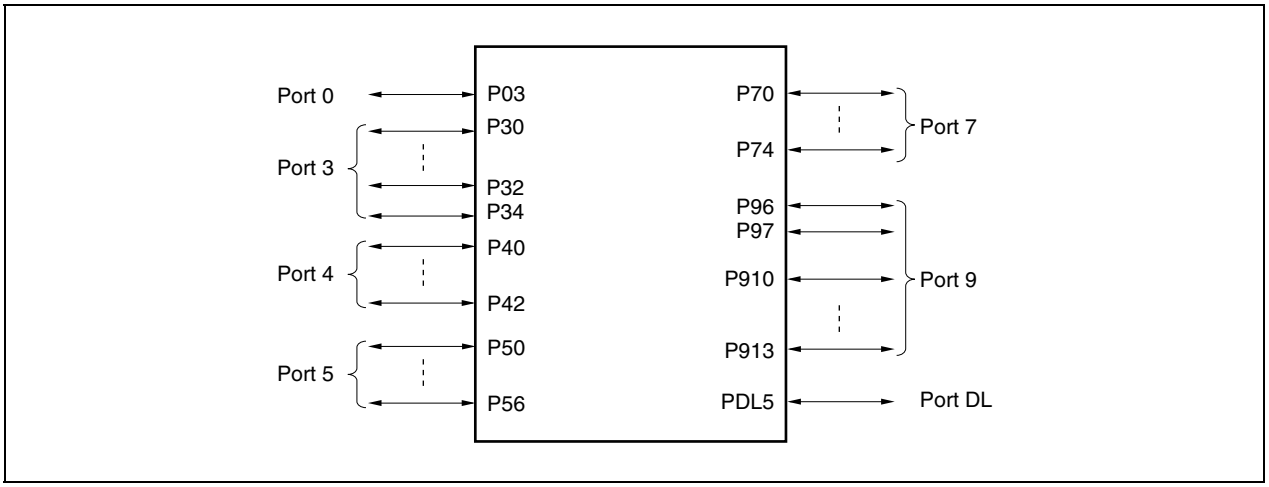
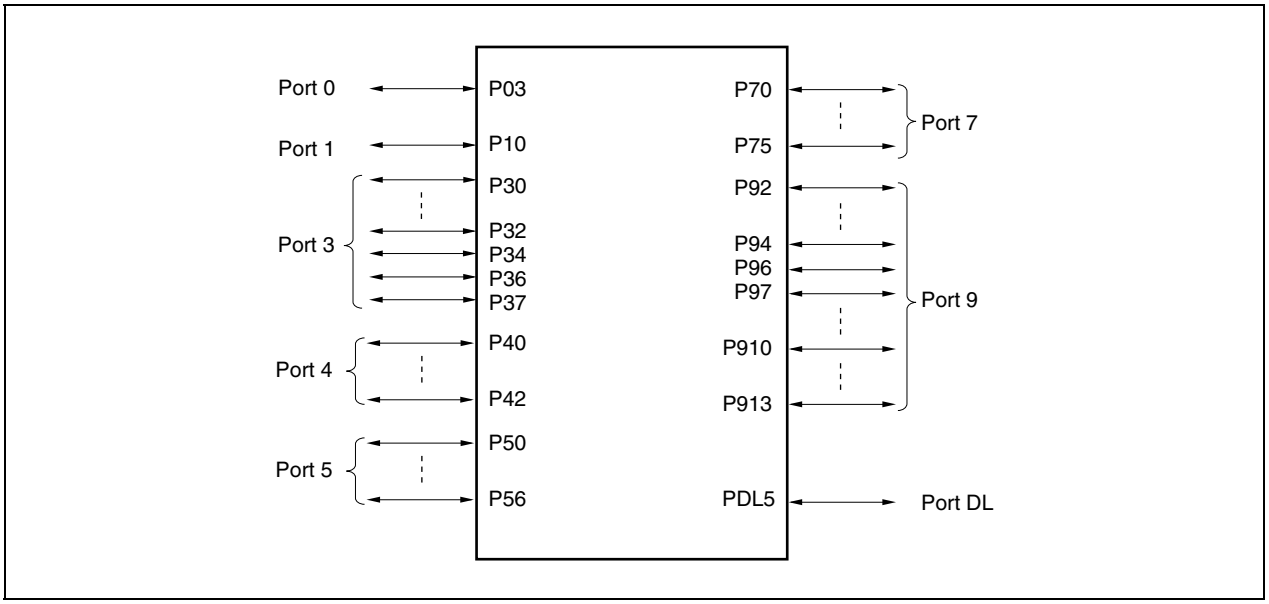


Figure 4-2. Port Configuration Diagram (V850ES/JC3-H (48 pin))



PFCE34	PFC34	Specification of P34 pin alternate function
0	0	TIAA10 input
0	1	TOAA10 output
1	0	TOAA1OFF input/INTP09 input
1	1	Setting prohibited

PFCE33 Note	PFC33 Note	Specification of P33 pin alternate function
0	0	TIAA01 input
0	1	TOAA01 output
1	0	RTCDIV output
1	1	RTCCL output

Note V850ES/JE3-H only

PFCE32	PFC32	Specification of P32 pin alternate function
0	0	ASCKC0 input
0	1	$\overline{\text{SCKF4}}$ I/O
1	0	TIAA00 input
1	1	TOAA00 output

PFCE31	PFC31	Specification of P31 pin alternate function
0	0	RXDC0 input
0	1	SIF4 input
1	0	INTP08 input
1	1	Setting prohibited

PFCE30	PFC30	Specification of P30 pin alternate function
0	0	TXDC0 output
0	1	SOF4 output
1	0	INTP07 input
1	1	Setting prohibited

(10) TAAn capture/compare register 1 (TAAnCCR1)

The TAAnCCR1 register can be used as a capture register or a compare register depending on the mode.

This register can be used as a capture register or a compare register only in the free-running timer mode, depending on the setting of the TAAnOPT0.TAAnCCS1 bit. In the pulse width measurement mode, the TAAnCCR1 register can be used only as a capture register. In any other mode, this register can be used only as a compare register.

The TAAnCCR1 register can be read or written during operation.

This register can be read or written in 16-bit units.

Reset sets this register to 0000H.

Caution Accessing the TAAnCCR1 register is prohibited in the following statuses. For details, see 3.4.9 (2) Accessing specific on-chip peripheral I/O registers.

- **When the CPU operates with the subclock and the main clock oscillation is stopped**
- **When the CPU operates with the internal oscillation clock**

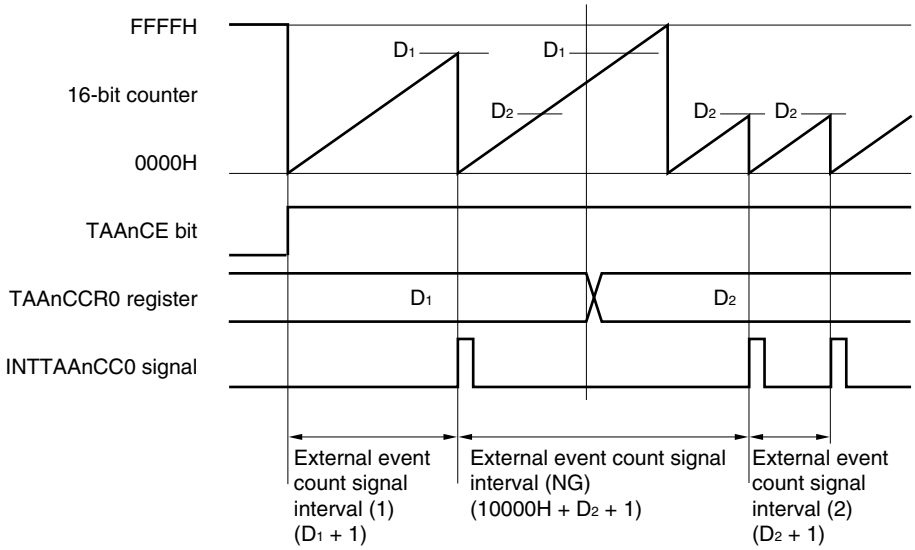
After reset: 0000H R/W Address: TAA0CCR1 FFFFF638H, TAA1CCR1 FFFFF648H, TAA2CCR1 FFFFF658H, TAA4CCR1 FFFFF678H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAAnCCR1 (n = 0 to 2, 4)																

(b) Notes on rewriting the TAAnCCR0 register

To change the value of the TAAnCCR0 register to a smaller value, stop counting once and then change the set value.

If the value of the TAAnCCR0 register is rewritten to a smaller value during counting, the 16-bit counter may overflow.



Remark n = 0 to 2

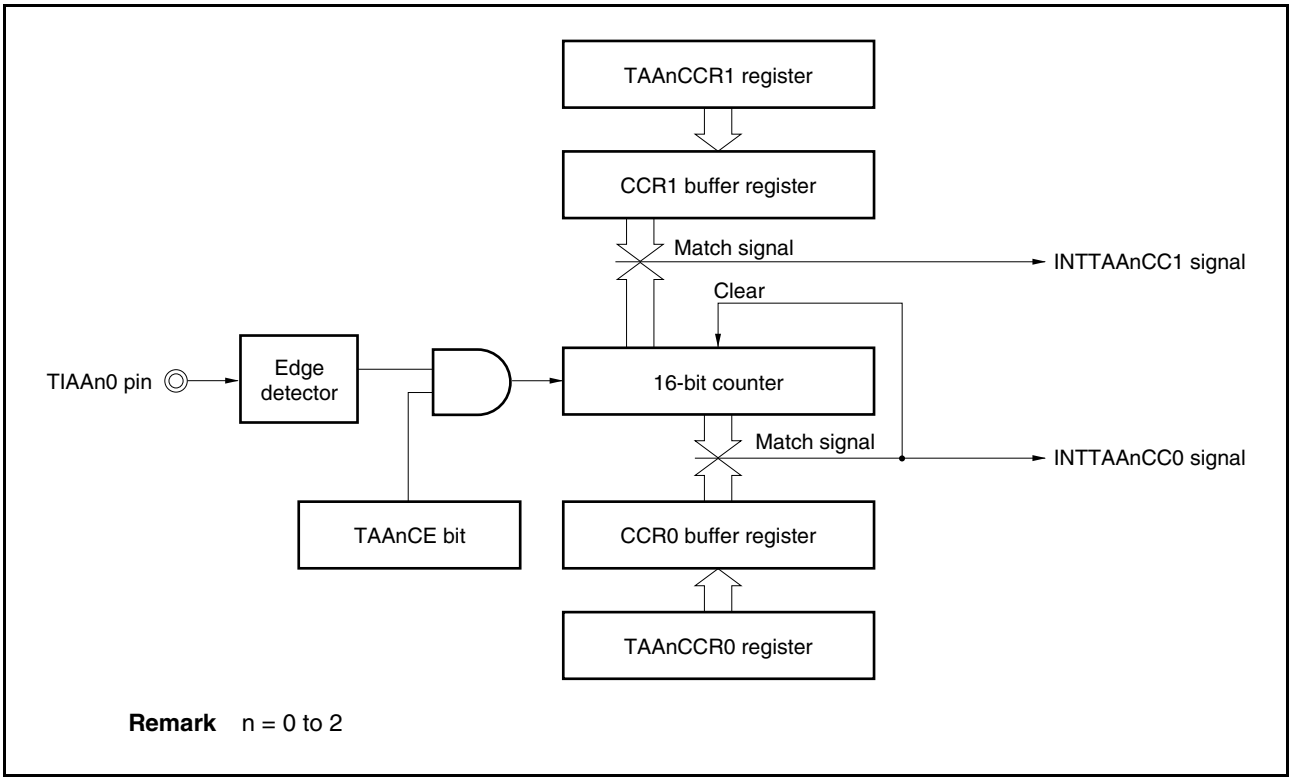
If the value of the TAAnCCR0 register is changed from D_1 to D_2 while the count value is greater than D_2 but less than D_1, the count value is transferred to the CCR0 buffer register as soon as the TAAnCCR0 register has been rewritten. Consequently, the value that is compared with the 16-bit counter is D_2.

Because the count value has already exceeded D_2, however, the 16-bit counter counts up to FFFFH, overflows, and then counts up again from 0000H. When the count value matches D_2, the INTTAAnCC0 signal is generated.

Therefore, the INTTAAnCC0 signal may not be generated at the valid edge count of "(D_1 + 1) times" or "(D_2 + 1) times" as originally expected, but may be generated at the valid edge count of "(10000H + D_2 + 1) times".

(c) Operation of TAAnCCR1 register

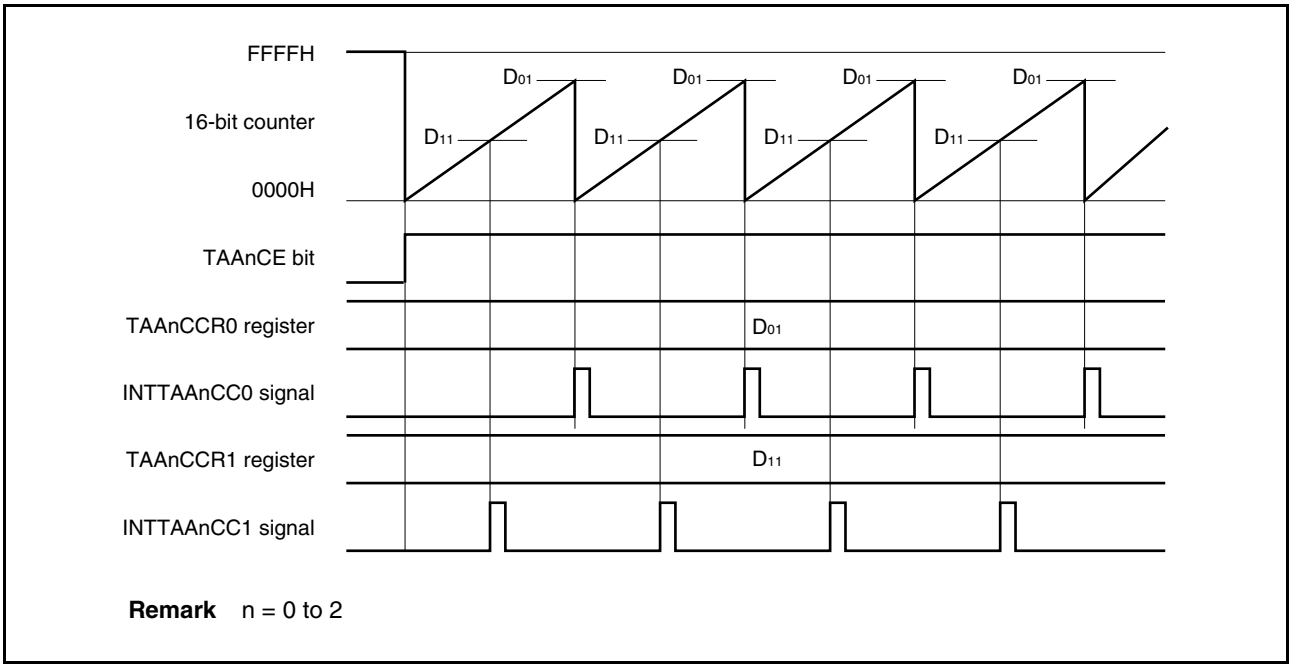
Figure 6-18. Configuration of TAAnCCR1 Register



Remark n = 0 to 2

If the set value of the TAAnCCR1 register is smaller than the set value of the TAAnCCR0 register, the INTTAAnCC1 signal is generated once per cycle.

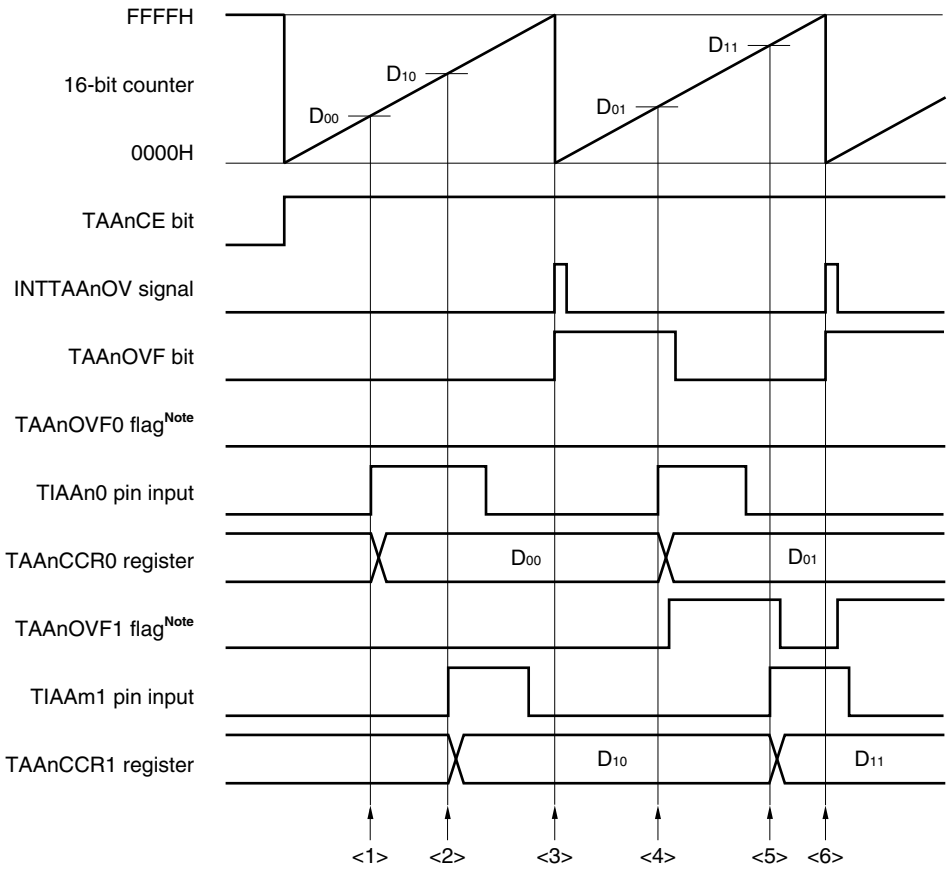
Figure 6-19. Timing Chart When $D_{01} \geq D_{11}$



Remark n = 0 to 2

(b) When using capture/compare register as capture register

Figure 6-38. Software Processing Flow in Free-Running Timer Mode (Capture Function) (1/2)



Remark n = 0 to 2
m = 2 (V850ES/JC3-H)
m = 0 to 2 (V850ES/JE3-H)

When the TT0CE bit is set to 1, the value of the 16-bit counter is cleared from FFFFH to 0000H in synchronization with the count clock, and the counter starts counting. At this time, the output of the TOT00 pin is inverted. Additionally, the set value of the TT0CCR0 register is transferred to the CCR0 buffer register.

When the count value of the 16-bit counter matches the value of the CCR0 buffer register, the 16-bit counter is cleared to 0000H, the output of the TOT00 pin is inverted, and a compare match interrupt request signal (INTTT0CC0) is generated.

The interval can be calculated by the following expression.

Interval = (Set value of TT0CCR0 register + 1) × Count clock cycle

Figure 8-9. Register Setting for Interval Timer Mode Operation (1/2)

(a) TMT0 control register 0 (TT0CTL0)

	TT0CE					TT0CKS2	TT0CKS1	TT0CKS0
TT0CTL0	0/1	0	0	0	0	0/1	0/1	0/1

Select count clock

0: Stops counting
1: Enables counting

(b) TMT0 control register 1 (TT0CTL1)

		TT0EST	TT0EEE		TT0MD3	TT0MD2	TT0MD1	TT0MD0
TT0CTL1	0	0	0	0	0	0	0	0

0, 0, 0, 0:
Interval timer mode

(c) TMT0 I/O control register 0 (TT0IOC0)

					TT0OL1	TT0OE1	TT0OL0	TT0OE0
TT0IOC0	0	0	0	0	0/1	0/1	0/1	0/1

0: Disables TOT00 pin output
1: Enables TOT00 pin output

Setting of TOT00 pin output level before count operation
0: Low level
1: High level

0: Disables TOT01 pin output
1: Enables TOT01 pin output

Setting of TOT01 pin output level before count operation
0: Low level
1: High level

<2> TT0ECM1 and TT0ECM0 bits: Timer/counter clear function upon match of the compare register

The 16-bit counter performs its count operation in accordance with the set value of the TT0ECM1 and TT0ECM0 bits when the count value of the counter matches the value of the CCRn buffer register.

- When TT0ECM1 and TT0ECM0 bits = 00

  The 16-bit counter is not cleared when its count value matches the value of the CCRn buffer register.

- When TT0ECM1 and TT0ECM0 bits = 01

  The 16-bit counter performs a count operation under the following condition when its count value matches the value of the CCR0 buffer register.

Next Count Operation	Description
Count up	16-bit counter is cleared to 0000H.
Count down	Count value of 16-bit counter is counted down.

- When TT0ECM1 and TT0ECM0 bits = 10

  The 16-bit counter performs a count operation under the following condition when its count value matches the value of the CCR1 buffer register.

Next Count Operation	Description
Count up	Count value of 16-bit counter is counted up.
Count down	16-bit counter is cleared to 0000H.

- When TT0ECM1 and TT0ECM0 bits = 11

  The 16-bit counter performs a count operation under the following condition when its count value matches the value of the CCR0 buffer register.

Next Count Operation	Description
Count up	16-bit counter is cleared to 0000H.
Count down	Count value of 16-bit counter is counted down.

  The 16-bit counter performs a count operation under the following condition when its count value matches the value of the CCR1 buffer register.

Next Count Operation	Description
Count up	Count value of 16-bit counter is counted up.
Count down	16-bit counter is cleared to 0000H.

11.3 Registers

The real-time counter is controlled by the following 18 registers.

(1) Real-time counter control register 0 (RC1CC0)

The RC1CC0 register selects the real-time counter input clock.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFFADDH

	7	6	5	4	3	2	1	0
RC1CC0	RC1PWR	RC1CKS	0	0	0	0	0	0

RC1PWR	Real-time counter operation control
0	Stops real-time counter operation.
1	Enables real-time counter operation.

RC1CKS	Operation clock selection
0	Selects f_{XT} as operation clock.
1	Selects f_{BRG} as operation clock.

Cautions 1. Follow the description in 11.4.8 Initializing real-time counter when stopping (RC1PWR = 1 → 0) the real-time counter while it is operating.

2. The RC1CKS bit can be rewritten only when the real-time counter is stopped (RC1PWR bit = 0). Furthermore, rewriting the RC1CKS bit at the same time as setting the RC1PWR bit from 0 to 1 is prohibited.

(2) Real-time counter control register 1 (RC1CC1)

The RC1CC1 register is an 8-bit register that starts or stops the real-time counter, controls the RTCCL and RTC1HZ pins, selects the 12-hour or 24-hour system, and sets the fixed-cycle interrupt function.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

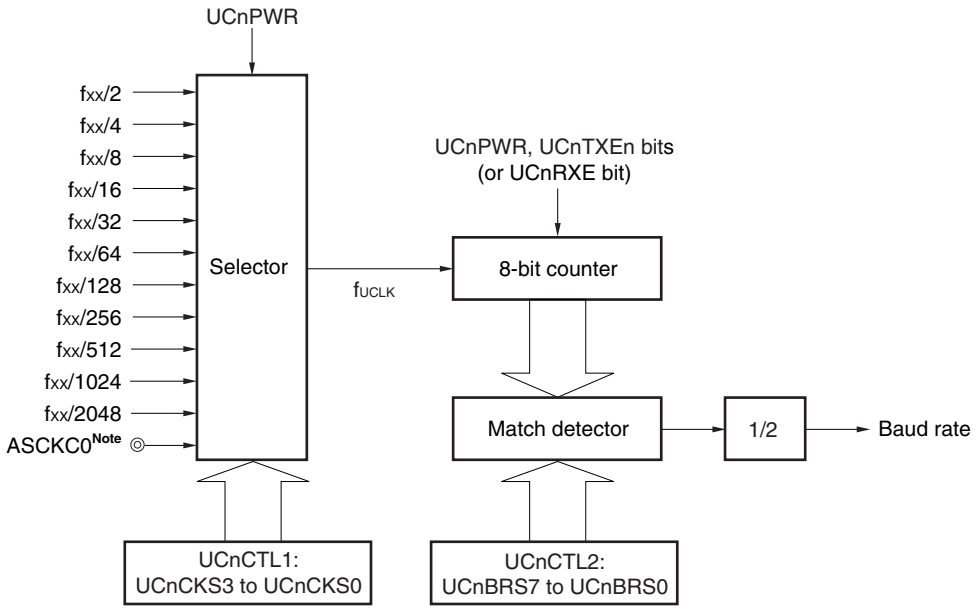
16.7 Dedicated Baud Rate Generator

The dedicated baud rate generator consists of a source clock selector block and an 8-bit programmable counter, and generates a serial clock during transmission and reception with UARTCn. Regarding the serial clock, a dedicated baud rate generator output can be selected for each channel.

There is an 8-bit counter for transmission and another one for reception.

(1) Baud rate generator configuration

Figure 16-18. Configuration of Baud Rate Generator



Note Only UARTC0 is valid; setting UARTC4 is prohibited.

Remarks1. n = 0, 2, 4 (V850ES/JC3-H (40 pin))
n = 0, 2 to 4 (V850ES/JC3-H (48 pin), V850ES/JE3-H)

2. fxx: Main clock frequency
fUCLK: Base clock frequency

(a) Base clock

When the UCnCTL0.UCnPWR bit is 1, the clock selected by the UCnCTL1.UCnCKS3 to UCnCTL1.UCnCKS0 bits is supplied to the 8-bit counter. This clock is called the base clock (fUCLK).

(b) Serial clock generation

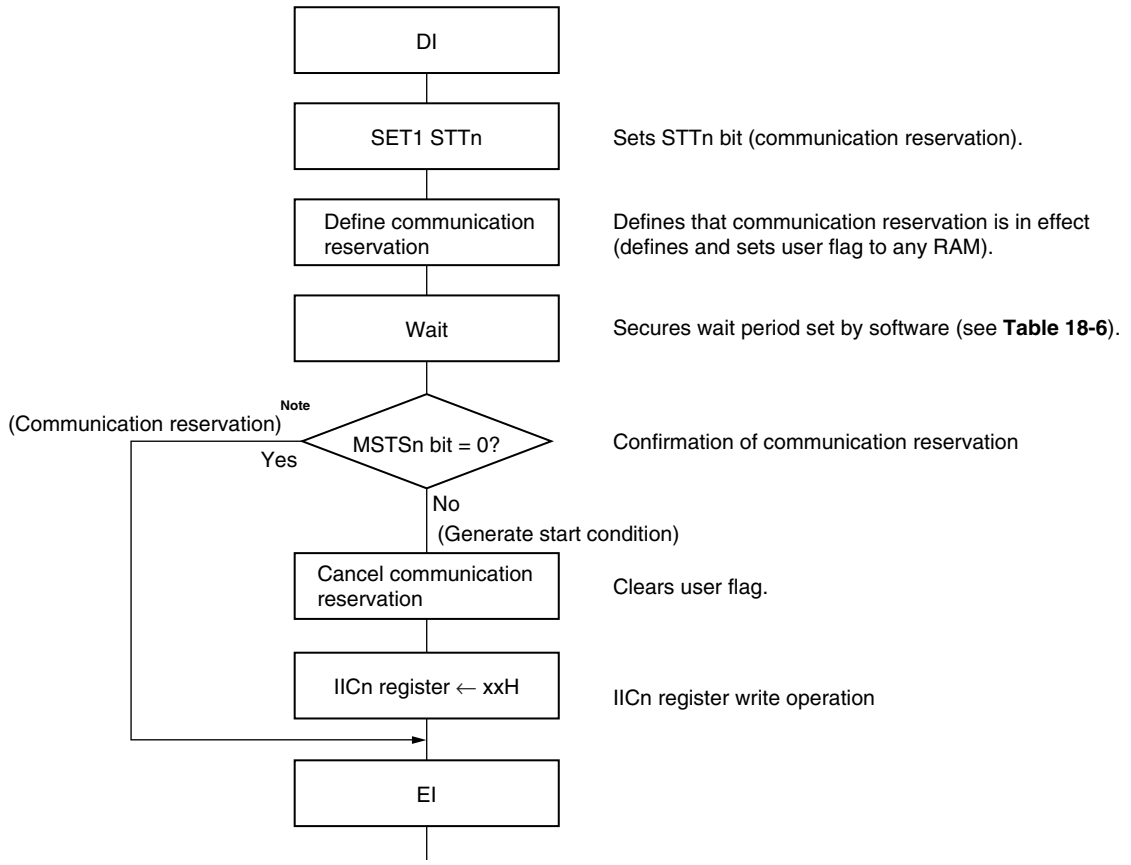
A serial clock can be generated by setting the UCnCTL1 register and the UCnCTL2 register (n = 0 to 4).

The base clock is selected by UCnCTL1.UCnCKS3 to UCnCTL1.UCnCKS0 bits.

The frequency division value for the 8-bit counter can be set using the UCnCTL2.UCnBRS7 to UCnCTL2.UCnBRS0 bits.

The communication reservation flowchart is illustrated below.

Figure 18-17. Communication Reservation Flowchart



Note The communication reservation operation executes a write to the IICn register when a stop condition interrupt request occurs.

(3) CAN0 global automatic block transmission control register (C0GMABT)

The C0GMABT register is used to control the automatic block transmission (ABT) operation.

(1/2)

After reset: 0000H R/W Address: 03FEC006H

(a) Read

	15	14	13	12	11	10	9	8
C0GMABT	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	ABTCLR	ABTTRG

(b) Write

	15	14	13	12	11	10	9	8
C0GMABT	0	0	0	0	0	0	Set ABTCLR	Set ABTTRG
	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	Clear ABTTRG

Caution Before changing the normal operation mode with ABT to the initialization mode, be sure to set the C0GMABT register to the default value (0000H). After setting, confirm that the C0GMABT register is initialized to 0000H.

(a) Read

ABTCLR	Automatic block transmission engine clear status bit
0	Clearing the automatic transmission engine is completed.
1	The automatic transmission engine is being cleared.

Remarks 1. Set the ABTCLR bit to 1 while the ABTTRG bit is cleared to 0.
The operation is not guaranteed if the ABTCLR bit is set to 1 while the ABTTRG bit is set to 1.

2. When the automatic block transmission engine is cleared by setting the ABTCLR bit to 1, the ABTCLR bit is automatically cleared to 0 as soon as the requested clearing processing is complete.

ABTTRG	Automatic block transmission status bit
0	Automatic block transmission is stopped.
1	Automatic block transmission is under execution.

Cautions 1. Do not set the ABTTRG bit to 1 in the initialization mode. If the ABTTRG bit is set to 1 in the initialization mode, the operation is not guaranteed after the CAN module has entered the normal operation mode with ABT.

2. Do not set the ABTTRG bit to 1 while the C0CTRL.TSTAT bit is set to 1. Directly confirm that the TSTAT bit = 0 before setting the ABTTRG bit to 1.

(17) CAN0 module transmit history list register (C0TGPT)

The C0TGPT register is used to read the transmit history list.

(1/2)

After reset: xx02H R/W Address: 03FEC064H

(a) Read

	15	14	13	12	11	10	9	8
C0TGPT	TGPT7	TGPT6	TGPT5	TGPT4	TGPT3	TGPT2	TGPT1	TGPT0
	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	THPM	TOVF

(b) Write

	15	14	13	12	11	10	9	8
C0TGPT	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	Clear TOVF

(a) Read

TGPT7 to TGPT0	Transmit history list read pointer
0 to 31	When the C0TGPT register is read, the contents of the element indexed by the read pointer (TGPT) of the transmit history list are read. These contents indicate the number of the message buffer to which a data frame or a remote frame was transmitted last.

THPM[Note 1]	Transmit history pointer match
0	The transmit history list has at least one message buffer number that has not been read.
1	The transmit history list has no message buffer numbers that have not been read.

TOVF[Note 2]	Transmit history list overflow bit
0	All the message buffer numbers that have not been read are preserved. All the numbers of the message buffers to which a new data frame or remote frame has been transmitted are recorded to the transmit history list (the transmit history list has a vacant element).
1	At least 7 entries have been stored since the host processor serviced the THL last time (i.e. read C0TGPT). The first 6 entries are sequentially stored whereas the last entry might have been overwritten by newly transmitted messages a number of times because all buffer numbers are stored at position LOPT-1 when TOVF bit is set to 1. As a consequence receptions cannot be completely recovered in the order that they were received.

Notes 1. The read value of the TGPT0 to TGPT7 bits is invalid when the THPM bit = 1.

2. If all the transmit history is read by the C0TGPT register while the TOVF bit is set (1), the THPM bit is not cleared (0) but kept set (1), even if transmission of new data has been completed.

Remark Transmission from message buffers 0 to 7 is not recorded to the transmit history list in the normal operation mode with ABT.

(13) UF0 device descriptor registers 0 to 17 (UF0DD0 to UF0DD17)

These registers store the value to be returned in response to the GET_DESCRIPTOR Device request.

These registers can be read or written in 8-bit units. However, data can be written to these registers only when the EP0NKA bit is set to 1.

Cautions 1. To rewrite these registers, set the EP0NKA bit to 1 before reading the register contents, and rewrite the register contents after confirming that the bit has been set, in order to prevent conflict between a read access and a write access.

2. Use the value defined by USB Specification Ver. 2.0 and the latest Class Specification as the set value.

	7	6	5	4	3	2	1	0	Address	After reset
UF0DDn (n = 0 to 17)									See **Table 21-5**.	Undefined

Table 20-5. Mapping and Data of UF0 Device Descriptor Registers

Symbol	Address	Field Name	Contents
UF0DD0	002001A2H	bLength	Size of this descriptor
UF0DD1	002001A4H	bDescriptorType	Device descriptor type
UF0DD2	002001A6H	bcdUSB	Value below decimal point of Rev. number of USB specification
UF0DD3	002001A8H		Value above decimal point of Rev. number of USB specification
UF0DD4	002001AAH	bDeviceClass	Class code
UF0DD5	002001ACH	bDeviceSubClass	Subclass code
UF0DD6	002001AEH	bDeviceProtocol	Protocol code
UF0DD7	002001B0H	bMaxPacketSize0	Maximum packet size of Endpoint0
UF0DD8	002001B2H	idVendor	Lower value of vendor ID
UF0DD9	002001B4H		Higher value of vendor ID
UF0DD10	002001B6H	idProduct	Lower value of product ID
UF0DD11	002001B8H		Higher value of product ID
UF0DD12	002001BAH	bcdDevice	Lower value of device release number
UF0DD13	002001BCH		Higher value of device release number
UF0DD14	002001BEH	iManufacturer	Index of string descriptor describing manufacturer
UF0DD15	002001C0H	iProduct	Index of string descriptor describing product
UF0DD16	002001C2H	lSerialNumber	Index of string descriptor describing device serial number
UF0DD17	002001C4H	BNumConfigurations	Number of settable configurations

(1) Initial settings for a bulk transfer (OUT: EP2, EP4)

(a) Initial settings for DMAC

- The DSAn registers (n = 0 to 3) are set to 00210000H (for EP2) or 00220000H (for EP4).
- The DADCn registers (n = 0 to 3) are set to 0080H.
  (8-bit transfer, transfer source address: fixed, transfer destination address: incremental)
- The DTFRn registers (n = 0 to 3) are set to 0000H.
- The UFDRQEN register is set up according to the DMA channel to be used.
  (For details, see 20.6.10 (1) USBF DMA request enable register (UFDRQEN).)

(b) Initial settings for EPC

- The UF0IDR register is set to 12H (for EP2) or 22H (for EP4) (demand mode).
- The UF0IM0.DMAEDM bit = 0
- The UF0IM3.BKO1NLM bit = 0 (for EP2)
- The UF0IM3.BKO1DTM bit = 0 (for EP2)
- The UF0IM3.BKO2NLM bit = 0 (for EP4)
- The UF0IM3.BKO2DTM bit = 0 (for EP4)

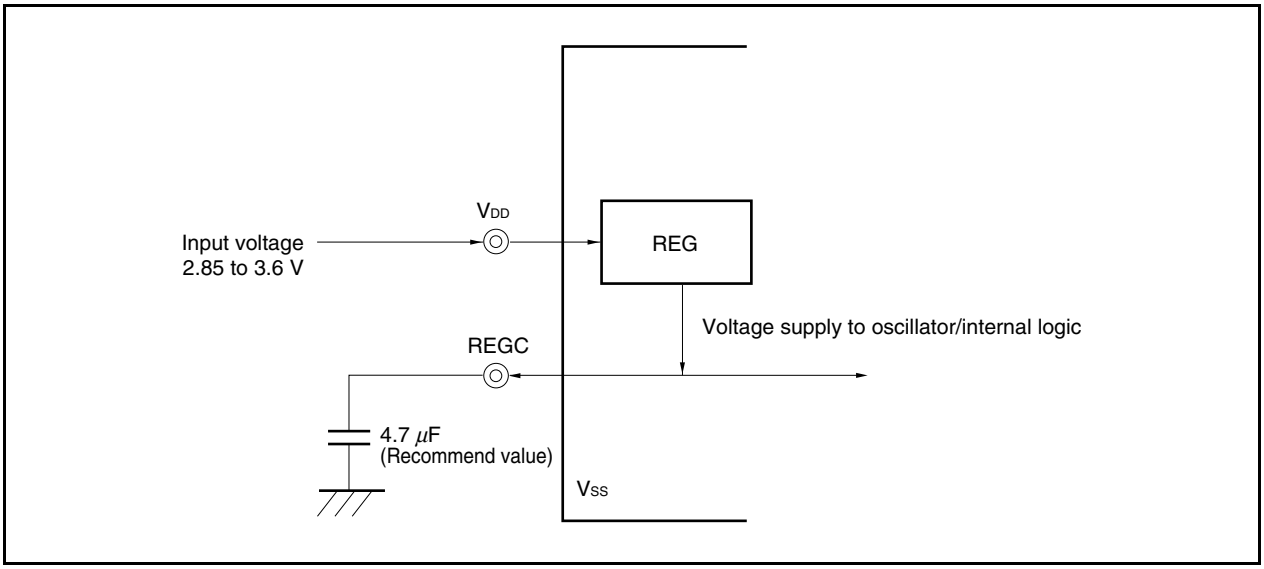
29.2 Operation

The regulators of the V850ES/JC3-H and V850ES/JE3-H always operate in any mode (normal operation mode, HALT mode, IDLE1 mode, IDLE2 mode, STOP mode, subclock operation mode, sub IDLE mode, or during reset).

Be sure to connect a capacitor (4.7 μF (Recommend value)) to the REGC pin to stabilize the regulator output.

A diagram of the regulator pin connection method is shown below.

Figure 29-2. REGC Pin Connection



[Program example (when using CA850 Ver. 3.10 or later)]

```
#-------------------------------------
#       SECURITYID
#-------------------------------------
        .section    "SECURITY_ID"   --Interrupt handler address 0x70
        .word       0x78563412      --0-3 byte code
        .word       0xF1DEBC9A      --4-7 byte code
        .hword      0xD423          --8-9 byte code
```

Remark Add the above program example to the startup files.

CHAPTER 32 ELECTRICAL SPECIFICATIONS

32.1 Absolute Maximum Ratings

(T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	$V_{DD} = EV_{DD} = UV_{DD} = AV_{REF0} = AV_{REF1}$	−0.5 to +4.6	V
	EV_{DD}	$V_{DD} = EV_{DD} = UV_{DD} = AV_{REF0} = AV_{REF1}$	−0.5 to +4.6	V
	UV_{DD}	$V_{DD} = EV_{DD} = UV_{DD} = AV_{REF0} = AV_{REF1}$	−0.5 to +4.6	V
	AV_{REF0}	$V_{DD} = EV_{DD} = UV_{DD} = AV_{REF0} = AV_{REF1}$	−0.5 to +4.6	V
	AV_{REF1}	$V_{DD} = EV_{DD} = UV_{DD} = AV_{REF0} = AV_{REF1}$	−0.5 to +4.6	V
	V_{SS}	$V_{SS} = AV_{SS}$	−0.5 to +0.5	V
	AV_{SS}	$V_{SS} = AV_{SS}$	−0.5 to +0.5	V
Input voltage	V_{I1}	P60 to P65, P92 to P94, P96, P97, P910 to P913, PDL5, $\overline{\text{RESET}}$, FLMD0	−0.5 to EV_{DD} + 0.5 Note 1	V
	V_{I2}	UDMF, UDPF	−0.5 to UV_{DD} + 0.5 Note 1	V
	V_{I3}	P10	−0.5 to AV_{REF1} + 0.5 Note 1	V
	V_{I4}	X1, X2, XT1, XT2	−0.5 to V_{RO} Note 2 + 0.5 Note 1	V
	V_{I5}	P02, P03, P30 to P37, P40 to P42, P52 to P56	−0.5 to +6.0	V
Analog input voltage	V_{IAN}	P70 to P79	−0.5 to AV_{REF0} + 0.5 Note 1	V

Cautions 1. Do not directly connect the output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open-drain pins or open-collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage. Therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Notes 1. Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

2. On-chip regulator output voltage (2.5 V (TYP.))

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

(6/34)

Symbol	Name	Unit	Page
C0MDATA115	CAN0 message data byte 1 register 15	CAN	920
C0MDATA116	CAN0 message data byte 1 register 16	CAN	920
C0MDATA117	CAN0 message data byte 1 register 17	CAN	920
C0MDATA118	CAN0 message data byte 1 register 18	CAN	920
C0MDATA119	CAN0 message data byte 1 register 19	CAN	920
C0MDATA120	CAN0 message data byte 1 register 20	CAN	920
C0MDATA121	CAN0 message data byte 1 register 21	CAN	920
C0MDATA122	CAN0 message data byte 1 register 22	CAN	920
C0MDATA123	CAN0 message data byte 1 register 23	CAN	920
C0MDATA124	CAN0 message data byte 1 register 24	CAN	920
C0MDATA125	CAN0 message data byte 1 register 25	CAN	920
C0MDATA126	CAN0 message data byte 1 register 26	CAN	920
C0MDATA127	CAN0 message data byte 1 register 27	CAN	920
C0MDATA128	CAN0 message data byte 1 register 28	CAN	920
C0MDATA129	CAN0 message data byte 1 register 29	CAN	920
C0MDATA130	CAN0 message data byte 1 register 30	CAN	920
C0MDATA131	CAN0 message data byte 1 register 31	CAN	920
C0MDATA200	CAN0 message data byte 2 register 00	CAN	920
C0MDATA201	CAN0 message data byte 2 register 01	CAN	920
C0MDATA202	CAN0 message data byte 2 register 02	CAN	920
C0MDATA203	CAN0 message data byte 2 register 03	CAN	920
C0MDATA204	CAN0 message data byte 2 register 04	CAN	920
C0MDATA205	CAN0 message data byte 2 register 05	CAN	920
C0MDATA206	CAN0 message data byte 2 register 06	CAN	920
C0MDATA207	CAN0 message data byte 2 register 07	CAN	920
C0MDATA208	CAN0 message data byte 2 register 08	CAN	920
C0MDATA209	CAN0 message data byte 2 register 09	CAN	920
C0MDATA210	CAN0 message data byte 2 register 10	CAN	920
C0MDATA211	CAN0 message data byte 2 register 11	CAN	920
C0MDATA212	CAN0 message data byte 2 register 12	CAN	920
C0MDATA213	CAN0 message data byte 2 register 13	CAN	920
C0MDATA214	CAN0 message data byte 2 register 14	CAN	920
C0MDATA215	CAN0 message data byte 2 register 15	CAN	920
C0MDATA216	CAN0 message data byte 2 register 16	CAN	920
C0MDATA217	CAN0 message data byte 2 register 17	CAN	920
C0MDATA218	CAN0 message data byte 2 register 18	CAN	920
C0MDATA219	CAN0 message data byte 2 register 19	CAN	920
C0MDATA220	CAN0 message data byte 2 register 20	CAN	920
C0MDATA221	CAN0 message data byte 2 register 21	CAN	920