Renesas Electronics America Inc - UPD70F3821GB-GAH-AX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, CSI, EBI/EMI, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	45
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 10x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3821gb-gah-ax

- A/D converter: 10-bit resolution: 5/6/10 channels
- D/A converter[Note3]: 8-bit resolution: 1 channel
- DMA controller: 4 channels
- DCU (debug control unit): JTAG interface
- Clock generator: Main clock or subclock operation:
  7-level CPU clock (f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, f_{XT})
  Clock-through mode/PLL mode selectable
- Internal oscillation clock: 220 kHz (TYP.)
- Power-save functions: HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE mode
- Package: 40-pin plastic WQFN (6 × 6 mm) (V850ES/JC3-H)
  48-pin plastic LQFP (fine pitch) (7 × 7 mm) (V850ES/JC3-H)
  48-pin plastic WQFN (7 × 7 mm) (V850ES/JC3-H)
  64-pin plastic LQFP (fine pitch) (10 × 10 mm) (V850ES/JE3-H)

Notes1. In the μPD70F3819 and 70F3825, one channel is shared with CAN.

2. μPD70F3819, 70F3825 only

3. V850ES/JC3-H (48 pin), V850ES/JE3-H only

6.3.1 Pin configuration

The timer inputs and outputs that configure TAAn are shared with the following ports. The port functions must be set when using each pin (see **Table 4-17 When Using Port Pins as Alternate-Function Pins**).

Table 6-2 Pin Configuration

Channel	Port	Timer AA Input	Timer AA Output	Other Alternate Function
TAA0	P32	TIAA00 Note 1	TOAA00	ASCK0/$\overline{\text{SCKF4}}$
	P33 Note 2	TIAA01	TOAA01	RTCDIV/RTCCL
TAA1	P34	TIAA10 Note 1	TOAA10	TOAA1OFF Note 2/INTP09
	P35 Note 2	TIAA11	TOAA11	RTC1HZ
TAA2	P97	TIAA20 Note 1	TOAA20	SIF1
	P96	TIAA21	TOAA21	INTP11
TAA4	–	–	–	–
	–	–	–	–

Notes 1. The TAAm0 pin functions alternately as a capture trigger input function, external event input function, and external trigger input function.

2. The V850ES/JE3-H only

Cautions1. When using the external trigger pulse output mode, one-shot pulse output mode, and pulse width measurement mode, select the internal clock as the count clock (by clearing the TAAnCTL1.TAAnEEE bit to 0).

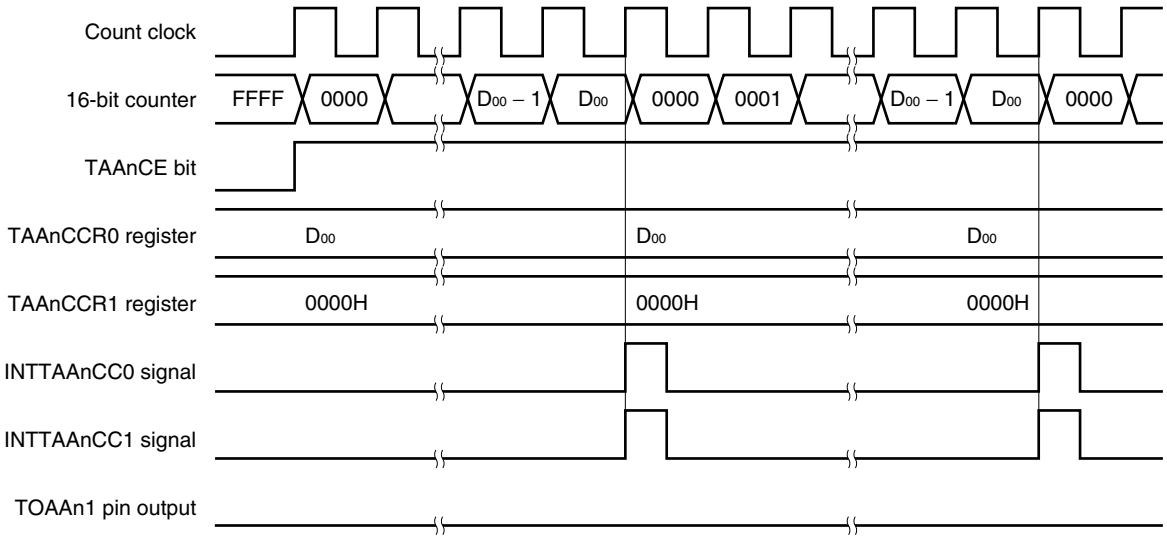
2. To use the external event count mode, specify that the valid edge of the TIAAn0 pin capture trigger input is not detected (by setting the TAAnCTL1.TAAnEEE bit to 1).

Remarks1. TAA4 has no timer input pin and output pin functions. When TAA4 is used solely, therefore, only the interval timer function can be used. The 6-phase PWM output function is available by using TAA4 in combination with TAB1.

2. n = 0 to 2, 4
m = 0 to 2

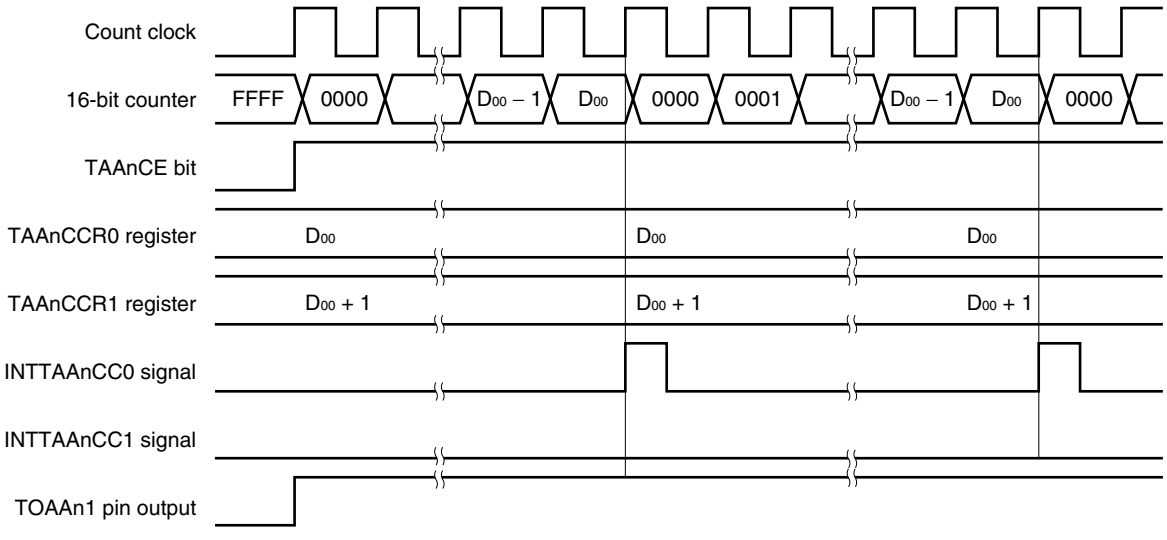
(b) 0%/100% output of PWM waveform

To output a 0% waveform, set the TAAnCCR1 register to 0000H. If the set value of the TAAnCCR0 register is FFFFH, the INTTAAnCC1 signal is generated periodically.



Remark n = 0 to 2

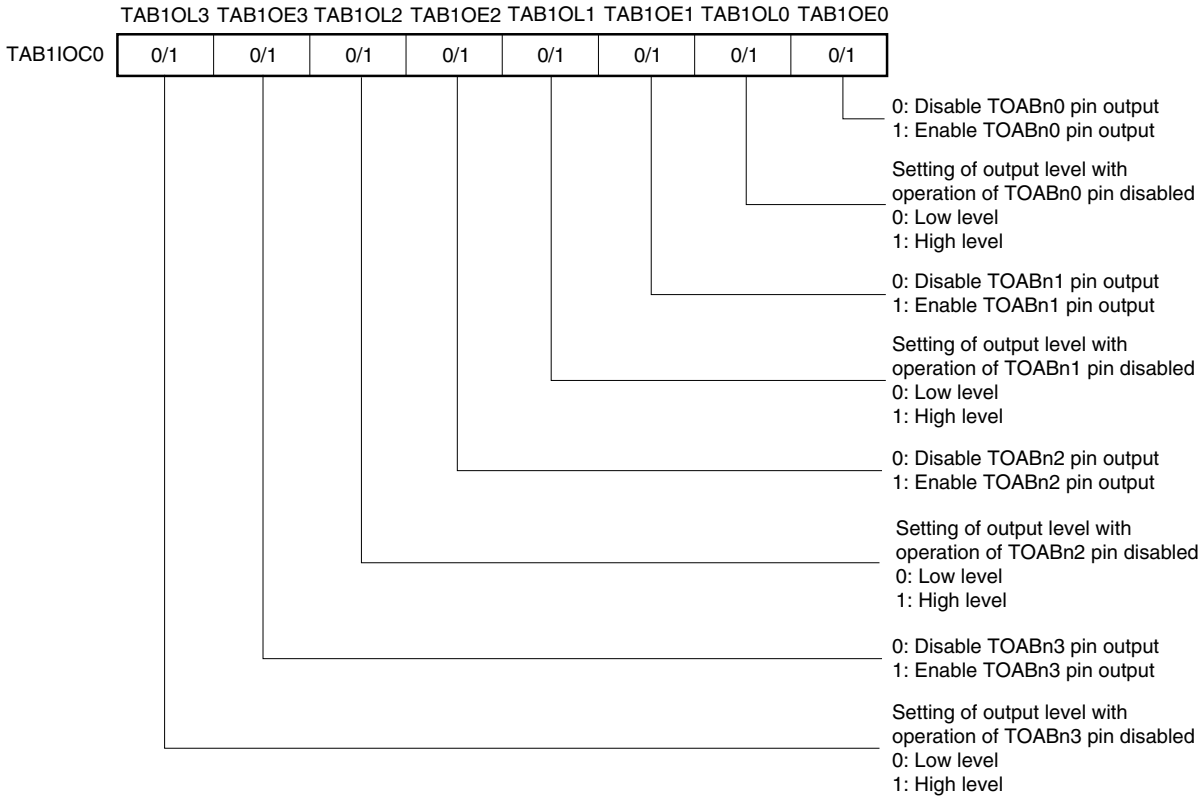
To output a 100% waveform, set a value of (set value of TAAnCCR0 register + 1) to the TAAnCCR1 register. If the set value of the TAAnCCR0 register is FFFFH, 100% output cannot be produced.



Remark n = 0 to 2

Figure 7-4. Register Setting for Interval Timer Mode Operation (2/2)

(c) TAB1 I/O control register 0 (TAB1IOC0)



(d) TAB1 counter read buffer register (TAB1CNT)

By reading the TAB1CNT register, the count value of the 16-bit counter can be read.

(e) TAB1 capture/compare register 0 (TAB1CCR0)

If the TAB1CCR0 register is set to D_0, the interval is as follows.

Interval = $(D_0 + 1) \times$ Count clock cycle

(f) TAB1 capture/compare registers 1 to 3 (TAB1CCR1 to TAB1CCR3)

Usually, the TAB1CCR1 to TAB1CCR3 registers are not used in the interval timer mode. However, the set value of the TAB1CCR1 to TAB1CCR3 registers is transferred to the CCR1 to CCR3 buffer registers. The compare match interrupt request signals (INTTAB1CCR1 to INTTAB1CCR3) are generated when the count value of the 16-bit counter matches the value of the CCR1 to CCR3 buffer registers.

Therefore, mask the interrupt requests by using the corresponding interrupt mask flags (TAB1CCMK1 to TAB1CCMK3).

Remark TAB1 I/O control register 1 (TAB1IOC1), TAB1 I/O control register 2 (TAB1IOC2), and TAB1 option register 0 (TAB1OPT0) are not used in the interval timer mode.

8.3.1 Pin configuration

The timer inputs and outputs that configure TMT0 are shared with the following ports. The port functions must be set when using each pin (see **Table 4-17 Using Port Pin as Alternate-Function Pin**).

Table 8-2. Pin Configuration

Port	Timer Input Pin		Timer Output	Other Alternate Function
P92	TIT01 (capture trigger input 1)	TENC01 (encoder input)	TOT01	–
P93	TIT00 (capture trigger input 0)	TECR0 (encoder clear input)	TOT00	–
P94	EVTT0/TENC00[Note]	–	–	–

Note The external event count input (EVTT0), encoder input (TENC00), and external trigger input are shared in a state that cannot be controlled by using the port functions. To use each function, set them by using the TT0IOC2 and TT0IOC3 registers after setting their corresponding ports.

(a) Function as compare register

The TT0CCR0 register can be rewritten even when the TT0CTL0.TT0CE bit = 1.

The set value of the TT0CCR0 register is transferred to the CCR0 buffer register. When the value of the 16-bit counter matches the value of the CCR0 buffer register, a compare match interrupt request signal (INTTT0CC0) is generated. If TOT00 pin output is enabled at this time, the output of the TOT00 pin is inverted.

When the TT0CCR0 register is used as a cycle register in the interval timer mode, or when the TT0CCR0 register is used as a cycle register in the external event count mode, external trigger pulse output mode, one-shot pulse output mode, PWM output mode, triangular-wave PWM output mode, or encoder compare mode, the value of the 16-bit counter is cleared (0000H) if its count value matches the value of the CCR0 buffer register.

The compare register is not cleared by setting the TT0CTL0.TT0CE bit to 0.

(b) Function as capture register

In the free-running timer mode (when the TT0CCR0 register is used as a capture register), the count value of the 16-bit counter is stored in the TT0CCR0 register if the valid edge of the capture trigger input pin (TIT00 pin) is detected. In the pulse width measurement mode, the count value of the 16-bit counter is stored in the TT0CCR0 register and the 16-bit counter is cleared (0000H) if the valid edge of the capture trigger input pin (TIT00 pin) is detected.

Even if the capture operation and reading the TT0CCR0 register conflict, the correct value of the TT0CCR0 register can be read.

The capture register is cleared by setting the TT0CTL0.TT0CE bit to 0.

The following table shows the functions of the capture/compare register in each mode, and how to write data to the compare register.

Table 8-3. Function of Capture/Compare Register in Each Mode and How to Write Compare Register

Operation Mode	TT0CCR0 Register	How to Write Compare Register
Interval timer	Compare register	Anytime write
External event counter	Compare register	Anytime write
External trigger pulse output	Compare register	Batch write[Note]
One-shot pulse output	Compare register	Anytime write
PWM output	Compare register	Batch write[Note]
Free-running timer	Capture/compare register	Anytime write
Pulse width measurement	Capture register	None
Triangular-wave WPM output	Compare register	Batch write[Note]
Encoder compare	Compare register	Anytime write

Note Writing to the TT0CCR1 register is the trigger.

Remark For anytime write and batch write, see **8.6 (2) Anytime write and batch write**.

Figure 8-9. Register Setting for Interval Timer Mode Operation (2/2)

(d) TMT0 counter read buffer register (TT0CNT)

By reading the TT0CNT register, the count value of the 16-bit counter can be read.

(e) TMT0 capture/compare register 0 (TT0CCR0)

If the TT0CCR0 register is set to D_0, the interval is as follows.

Interval = $(D_0 + 1) \times$ Count clock cycle

(f) TMT0 capture/compare register 1 (TT0CCR1)

The TT0CCR1 register is not used in the interval timer mode. However, the set value of the TT0CCR1 register is transferred to the CCR1 buffer register. When the count value of the 16-bit counter matches the value of the CCR1 buffer register, the TOT01 pin output is inverted and a compare match interrupt request signal (INTTT0CC1) is generated.

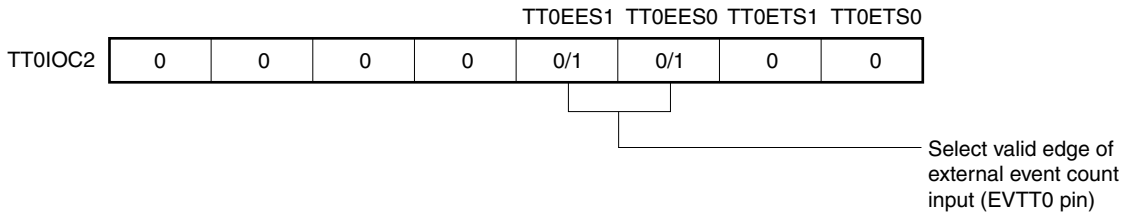
By setting this register to the same value as the value set in the TT0CCR0 register, a square wave with a duty factor of 50% can be output from the TOT01 pin.

When the TT0CCR1 register is not used, it is recommended to set its value to FFFFH. Also mask the register by the interrupt mask flag (TT0CCIC1.TT0CCMK1).

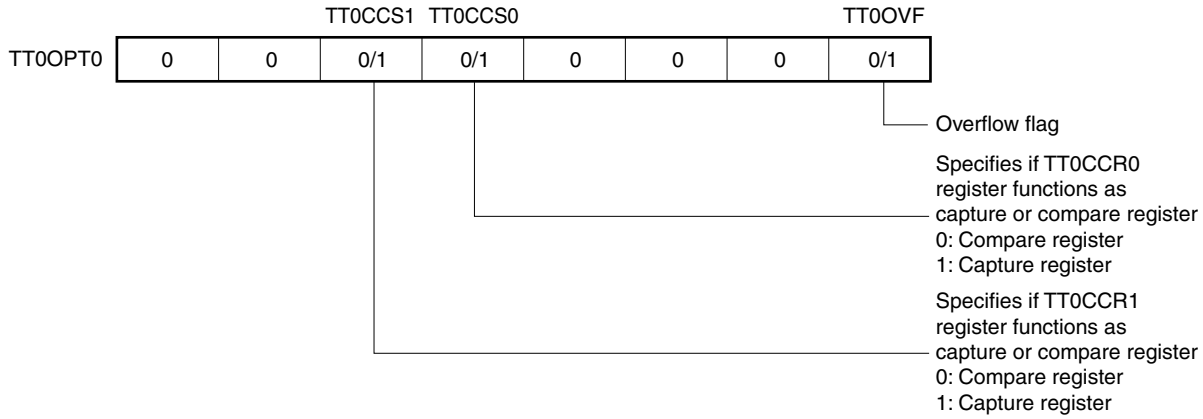
Remark TMT0 control register 2 (TT0CTL2), TMT0 I/O control register 1 (TT0IOC1), TMT0 I/O control register 2 (TT0IOC2), TMT0 I/O control register 3 (TT0IOC3), TMT0 option register 0 (TT0OPT0), TMT0 option register 1 (TT0OPT1), and TMT0 counter write register (TT0TCW) are not used in the interval timer mode.

Figure 8-36. Register Setting in Free-Running Timer Mode (2/2)

(e) TMT0 I/O control register 2 (TT0IOC2)



(f) TMT0 option register 0 (TT0OPT0)



(g) TMT0 counter read buffer register (TT0CNT)

The value of the 16-bit counter can be read by reading the TT0CNT register.

(h) TMT0 capture/compare registers 0 and 1 (TT0CCR0 and TT0CCR1)

These registers function as capture registers or compare registers depending on the setting of the TT0OPT0.TT0CCSn bit.

When the registers function as capture registers, they store the count value of the 16-bit counter when the valid edge input to the TIT0n pin is detected.

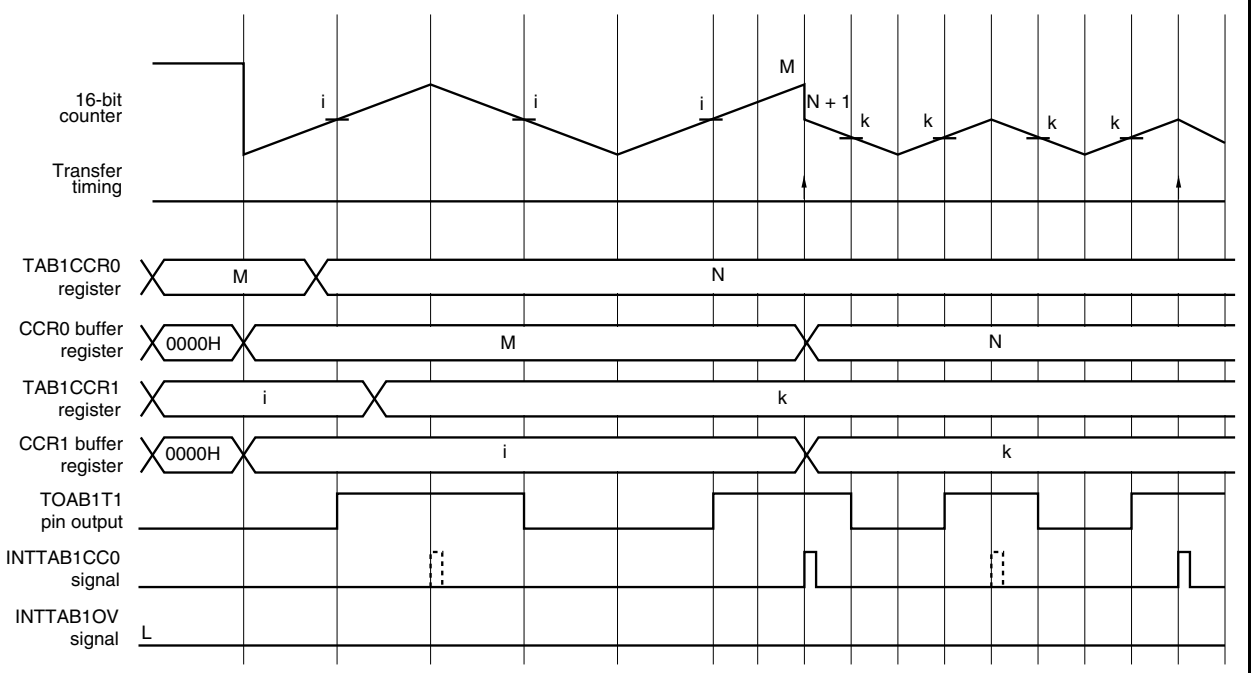
When the registers function as compare registers and when D_a is set to the TT0CCRn register, the INTTT0CCn signal is generated when the counter reaches (D_a + 1), and the output signals of the TOT00 and TOT01 pins are inverted.

Remark n = 0, 1

(b) Rewriting TAB1CCR0 register

When rewriting the TAB1CCR0 register in the intermittent batch mode, the output waveform differs depending on where the occurrence of the crest or valley interrupt is specified by the interrupt culling setting. The following figure illustrates the change of the output waveform when interrupts are culled.

Figure 10-32. Rewriting TAB1CCR0 Register (When Crest Interrupt Is Set)



The transfer timing is generated when the crest interrupt occurs, the cycle of counting up and counting down changes, and an asymmetrical triangular wave is output.

Remarks 1. This is an example of the operation when the TAB1OPT1.TAB1ICE bit = 1, TAB1OPT1.TAB1IOE bit = 0, and TAB1OPT1.TAB1ID4 to TAB1OPT1.TAB1ID0 bits = 00001.

2. : Culled interrupt

(3) Real-time counter control register 2 (RC1CC2)

The RC1CC2 register is an 8-bit register that controls the alarm interrupt function and waiting of counters.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFFADFH

	7	6	5	4	3	2	1	0
RC1CC2	WALE	0	0	0	0	0	RWST	RWAIT

WALE	Alarm interrupt (INTRTC1) operation control
0	Does not generate interrupt upon alarm match.
1	Generates interrupt upon alarm match.

RWST	Real-time counter wait state
0	Counter operating
1	Counting up of second to year counters stopped (Reading and writing of counter values enabled)
This is a status flag indicating whether the RWAIT bit setting is valid. Read or write counter values after confirming that the RWST bit is 1.	

RWAIT	Real-time counter wait control
0	Sets counter operation.
1	Stops count operation of second to year counters. (Counter value read/write mode)
This bit controls the operation of the counters. Be sure to write 1 to this bit when reading or writing counter values. If the RC1SUBC register overflows while the RWAIT bit is 1, the overflow information is retained internally and the RC1SEC register is counted up after two clocks or less (2 × 32.768 kHz) after 0 is written to the RWAIT bit. However, if the second counter value is rewritten while the RWAIT bit is 1, the retained overflow information is discarded.	

Cautions 1. See 11.4.5 Changing INTRTC1 interrupt setting during real-time counter operation when rewriting the WALE bit while the real-time counter operates (RC1PWR bit = 1).

2. Confirm that the RWST bit is set to 1 when reading or writing each counter value.

3. The RWST bit does not become 0 while each counter is being written, even if the RWAIT bit is set to 0. It becomes 0 when writing to each counter is completed.

17.2 Features

- Transfer rate: 12 Mbps max. (f_{XX} = 48 MHz, using internal clock, CSIF3)
  8 Mbps (f_{XX} = 48 MHz, using internal clock, CSIF0, CSIF2, CSIF4)
- Master mode and slave mode selectable
- 8-bit to 16-bit transfer, 3-wire serial interface
- Interrupt request signals (INTCFnT, INTCFnR) × 2
- Serial clock and data phase switchable
- Transfer data length selectable in 1-bit units between 8 and 16 bits
- Transfer data MSB-first/LSB-first switchable
- 3-wire transfer SOFn: Serial data output
  SIFn: Serial data input
  $\overline{\text{SCKFn}}$: Serial clock I/O
- Transmission mode, reception mode, and transmission/reception mode specifiable

Remark n = 0, 2 to 4

(9) Slave address registers 0, 1 (SVA0, SVA1)

The SVAn registers hold the I2C bus's slave address.

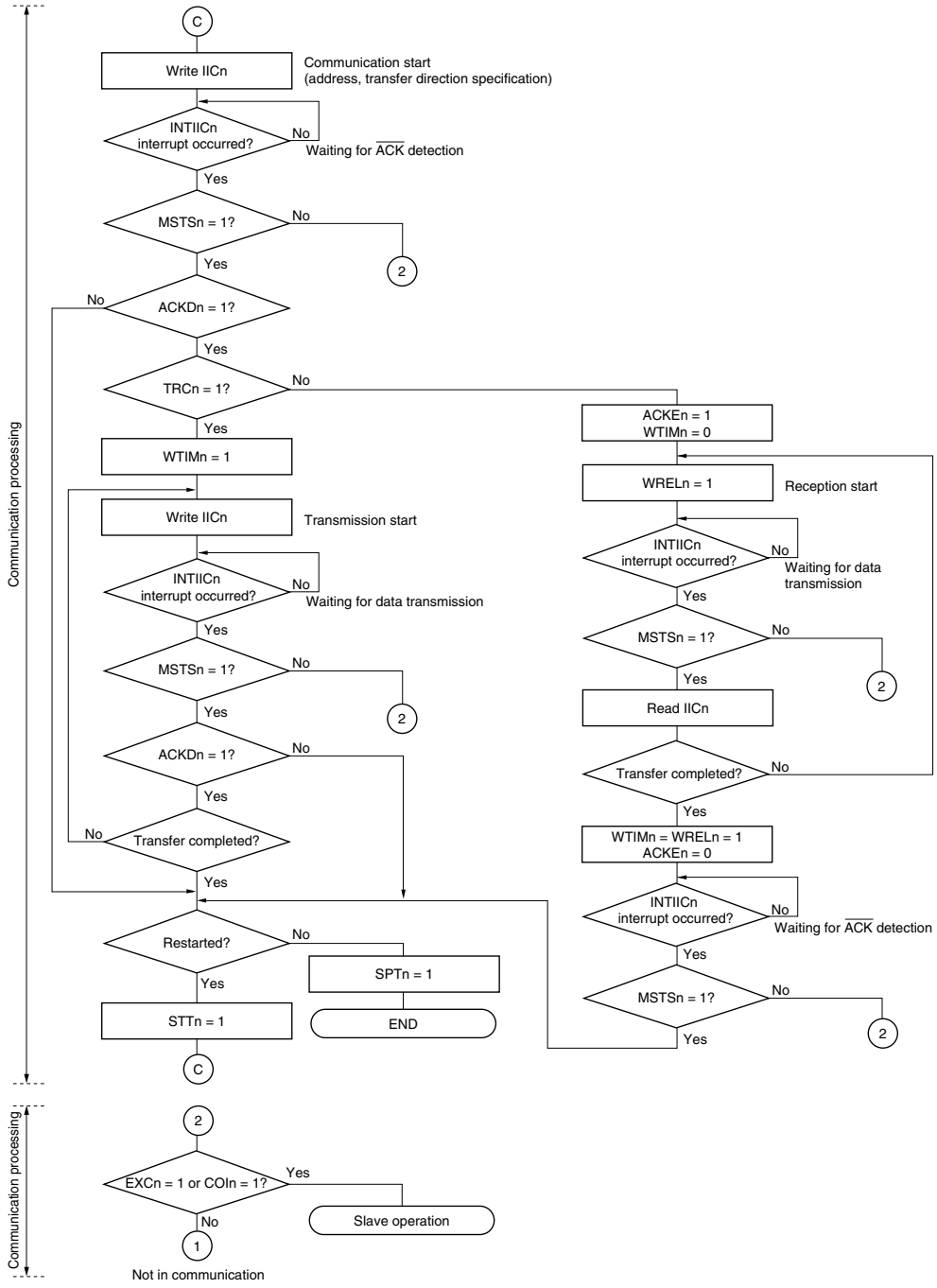
These registers can be read or written in 8-bit units, but bit 0 should be fixed to 0. However, rewriting these registers is prohibited when the IICSn.STDn bit = 1 (start condition detection).

Reset sets these registers to 00H.

After reset: 00H R/W Address: SVA0 FFFFFD83H, SVA1 FFFFFD93H, SVA2 FFFFFDA3H

	7	6	5	4	3	2	1	0
SVAn								0

Figure 18-19. Master Operation in Multimaster System (3/3)



Remarks 1. For the transmission and reception formats, comply with the specifications of the communicating product.

2. When using the V850ES/JC3-H or V850ES/JE3-H as the master in a multimaster system, read the IICSn.MSTSn bit for each INTIICn interrupt occurrence to confirm the arbitration result.

3. When using the V850ES/JC3-H or V850ES/JE3-H as the slave in a multimaster system, confirm the status using the IICSn and IICFn registers for each INTIICn interrupt occurrence to determine the next processing.

(4) Error state

(a) Types of error states

The following three types of error states are defined by the CAN specification.

- Error active
- Error passive
- Bus-off

These types of error states are classified by the values of the C0ERC.TEC7 to C0ERC.TEC0 bits (transmission error counter bits) and the C0ERC.REC6 to C0ERC.REC0 bits (reception error counter bits) as shown in Table 19-13.

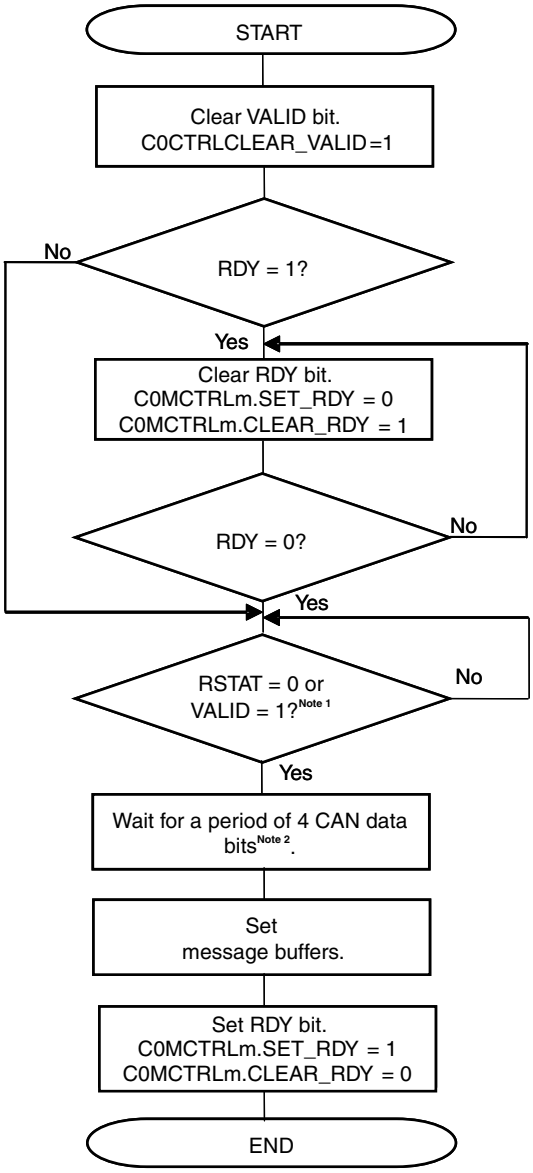
The present error state is indicated by the C0INFO register.

When each error counter value becomes equal to or greater than the error warning level (96), the C0INFO.TECS0 or C0INFO.RECS0 bit is set to 1. In this case, the bus state must be tested because it is considered that the bus has a serious fault. An error counter value of 128 or more indicates an error passive state and the TECS1 or RECS1 bit is set to 1.

- If the value of the transmission error counter is greater than or equal to 256 (actually, the transmission error counter does not indicate a value greater than or equal to 256), the bus-off state is reached and the C0INFO.BOFF bit is set to 1.
- If only one node is active on the bus at startup (i.e., when the bus is connected only to the local station), ACK is not returned even if data is transmitted. Consequently, re-transmission of the error frame and data is repeated. In the error passive state, however, the transmission error counter is not incremented and the bus-off state is not reached.

Figure 19-39 shows the processing for a receive message buffer (C0MCONFm.MT2 to C0MCONFm.MT0 bits = 001B to 101B).

Figure 19-39. Message Buffer Redefinition



Notes 1. If redefinition is performed during a message reception, confirm that a message is being received because the RDY bit must be set after a message is completely received.

2. This 4-bit period may redefine the message buffer while a message is received and stored.

(21) UF0 INT clear 0 register (UF0IC0)

This register controls clearing the interrupt sources indicated by the UF0IS0 register.

This register is write-only, in 8-bit units. If this register is read, the value FFH is read.

FW can clear an interrupt source by writing 0 to the corresponding bit of this register. Even a bit that is automatically cleared to 0 by hardware can be cleared by FW before it is cleared by hardware. Writing 0 to a bit of this register automatically sets the bit to 1. Writing 1 is invalid.

	7	6	5	4	3	2	1	0	Address	After reset
UF0IC0	BUSRSTC	RSUSPDC	1	SHORTC	DMAEDC	SETRQC	CLRRQC	EPHALTC	0020003CH	FFH

Bit position	Bit name	Function
7	BUSRSTC	This bit clears the Bus Reset interrupt. 0: Clear
6	RSUSPDC	This bit clears the Resume/Suspend interrupt. 0: Clear
4	SHORTC	This bit clears the Short interrupt. 0: Clear
3	DMAEDC	This bit clears the DMA_END interrupt. 0: Clear
2	SETRQC	This bit clears the SET_RQ interrupt. 0: Clear
1	CLRRQC	This bit clears the CLR_RQ interrupt. 0: Clear
0	EPHALTC	This bit clears the EP_Halt interrupt. 0: Clear

(41) UF0 endpoint 4 interface mapping register (UF0E4IM)

This register specifies for which Interface and Alternative Setting Endpoint4 is valid.

This register can be read or written in 8-bit units.

The setting of this register and the Alternative Setting selected by the SET_INTERFACE request indicate whether Endpoint4 is currently valid, and the hardware determines how the GET_STATUS/CLEAR_FEATURE/SET_FEATURE Endpoint4 request and the OUT transaction to Endpoint4 are responded to, and whether the related bits are valid or invalid.

	7	6	5	4	3	2	1	0	Address	After reset
UF0E4IM	E4EN2	E4EN1	E4EN0	E42AL1	E45AL4	E45AL3	E45AL2	E45AL1	0020008CH	00H

Bit position	Bit name	Function
7 to 5	E4EN2 to E4EN0	These bits set a link between the Interface of Endpoint4 and the two-/five-series Alternative Setting. The endpoint is linked with Alternative Setting 0. The endpoint linked with Alternative Setting 0 cannot be excluded from Alternative Setting 1 to 4.

E4EN2	E4EN1	E4EN0	Link status
1	1	1	Not linked with Interface
1	1	0	
1	0	1	Linked with Interface 4 and Alternative Setting 0
1	0	0	Linked with Interface 3 and Alternative Setting 0
0	1	1	Linked with Interface 2 and Alternative Setting 0
0	1	0	Linked with Interface 1 and Alternative Setting 0
0	0	1	Linked with Interface 0 and Alternative Setting 0
0	0	0	Not linked with Interface (default value)

When these bits are set to 110 or 111, they are invalid even if the E42AL1 bit is cleared to 0.

If the endpoint is linked, setting of the CONF bit of the UF0MODS register to 1 indicates that Endpoint4 is valid.

4	E42AL1	This bit validates Endpoint4 when the two-series Alternative Setting and the Alternative Setting of the linked Interface are set to 1. 1: Validate the endpoint when Alternative Setting 1 is set with CONF bit = 1. 0: Do not validate the endpoint even when Alternative Setting 1 is set with CONF bit = 1 (default value). This bit is valid when the E45AL4 to E45AL1 bits are 0000.
3 to 0	E45ALn	These bits validate Endpoint4 when the five-series Alternative Setting and the Alternative Setting of the linked Interface are set to n. 1: Validate the endpoint when Alternative Setting n is set with CONF bit = 1. 0: Do not validate the endpoint even when Alternative Setting n is set with CONF bit = 1 (default value).

Remark n = 1 to 4

20.6.8 Bulk-in register

(1) UF0 EP1 bulk-in transfer data register (UF0EP1BI)

The UF0EP1BI register writes the bulk-in transfer data of EP1.

The UF0EP1BI register can be read or written in 8-bit or 16-bit units.

After reset: 0000H R/W Address: 00201000H

	15	14	13	12	11	10	9	8
UF0EP1BI	0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	0
EP1BI7	EP1BI6	EP1BI5	EP1BI4	EP1BI3	EP1BI2	EP1BI1	EP1BI0

Bit position	Bit name	Function
7 to 0	EP1BI7 to EP1BI0	Writing the bulk-out transfer data of EP1. Data outputting to the EPC macro by writing data to this register. If using this register, setting the address (00201000H) in DMA destination address register (DDAn (n = 0 to 3)) of DMAC. In addition, set the RQnUR1E (n = 0 to 3) bit of the UFDRQEN register to 1 to assign a DMA channel.

(2) UF0 EP3 bulk-in transfer data register (UF0EP3BI)

The UF0EP3BI register writes the bulk-in transfer data of EP1.

The UF0EP3BI register can be read or written in 8-bit or 16-bit units.

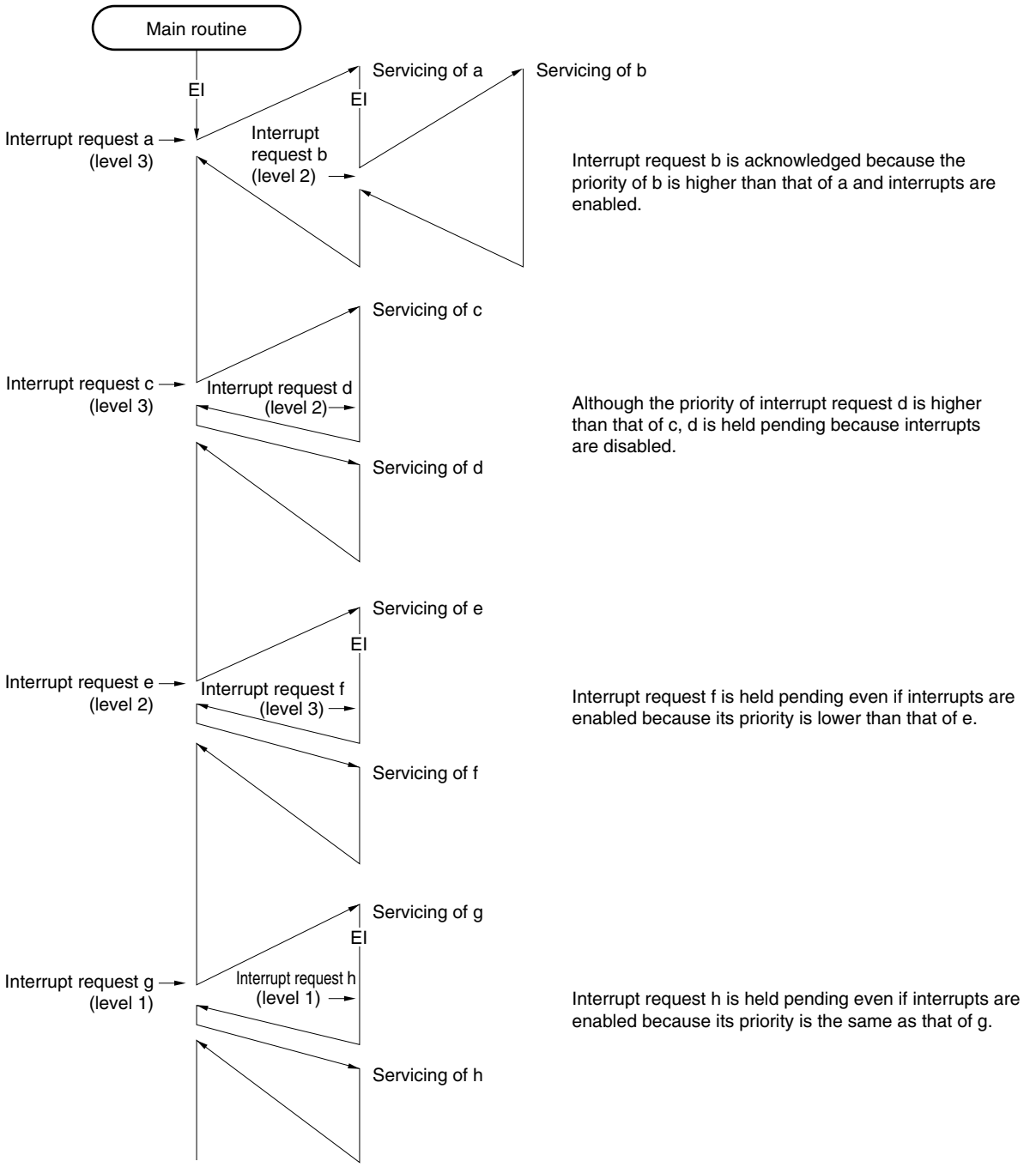
After reset: 0000H R/W Address: 00202000H

	15	14	13	12	11	10	9	8
UF0EP3BI	0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	0
EP3BI7	EP3BI6	EP3BI5	EP3BI4	EP3BI3	EP3BI2	EP3BI1	EP3BI0

Bit position	Bit name	Function
7 to 0	EP3BI7 to EP3BI0	Writing the bulk-out transfer data of EP3. Data outputting to the EPC macro by writing data to this register. If using this register, setting the address (00202000H) in DMA destination address register (DDAn (n = 0 to 3)) of DMAC. In addition, set the RQnUR3E (n = 0 to 3) bit of the UFDRQEN register to 1 to assign a DMA channel.

Figure 22-7. Example of Processing in Which Another Interrupt Request Signal Is Issued While an Interrupt Is Being Serviced (1/2)



Caution To perform multiple interrupt servicing, the values of the EIPC and EIPSW registers must be saved before executing the EI instruction. When returning from multiple interrupt servicing, restore the values of EIPC and EIPSW after executing the DI instruction.

Remarks 1. a to u in the figure are the temporary names of interrupt request signals shown for the sake of explanation.

2. The default priority in the figure indicates the relative priority between two interrupt request signals.

(14/34)

Symbol	Name	Unit	Page
C0MDLC15	CAN0 message data length register 15	CAN	922
C0MDLC16	CAN0 message data length register 16	CAN	922
C0MDLC17	CAN0 message data length register 17	CAN	922
C0MDLC18	CAN0 message data length register 18	CAN	922
C0MDLC19	CAN0 message data length register 19	CAN	922
C0MDLC20	CAN0 message data length register 20	CAN	922
C0MDLC21	CAN0 message data length register 21	CAN	922
C0MDLC22	CAN0 message data length register 22	CAN	922
C0MDLC23	CAN0 message data length register 23	CAN	922
C0MDLC24	CAN0 message data length register 24	CAN	922
C0MDLC25	CAN0 message data length register 25	CAN	922
C0MDLC26	CAN0 message data length register 26	CAN	922
C0MDLC27	CAN0 message data length register 27	CAN	922
C0MDLC28	CAN0 message data length register 28	CAN	922
C0MDLC29	CAN0 message data length register 29	CAN	922
C0MDLC30	CAN0 message data length register 30	CAN	922
C0MDLC31	CAN0 message data length register 31	CAN	922
C0MIDH00	CAN0 message identifier register 00H	CAN	924
C0MIDH01	CAN0 message identifier register 01H	CAN	924
C0MIDH02	CAN0 message identifier register 02H	CAN	924
C0MIDH03	CAN0 message identifier register 03H	CAN	924
C0MIDH04	CAN0 message identifier register 04H	CAN	924
C0MIDH05	CAN0 message identifier register 05H	CAN	924
C0MIDH06	CAN0 message identifier register 06H	CAN	924
C0MIDH07	CAN0 message identifier register 07H	CAN	924
C0MIDH08	CAN0 message identifier register 08H	CAN	924
C0MIDH09	CAN0 message identifier register 09H	CAN	924
C0MIDH10	CAN0 message identifier register 10H	CAN	924
C0MIDH11	CAN0 message identifier register 11H	CAN	924
C0MIDH12	CAN0 message identifier register 12H	CAN	924
C0MIDH13	CAN0 message identifier register 13H	CAN	924
C0MIDH14	CAN0 message identifier register 14H	CAN	924
C0MIDH15	CAN0 message identifier register 15H	CAN	924
C0MIDH16	CAN0 message identifier register 16H	CAN	924
C0MIDH17	CAN0 message identifier register 17H	CAN	924
C0MIDH18	CAN0 message identifier register 18H	CAN	924
C0MIDH19	CAN0 message identifier register 19H	CAN	924
C0MIDH20	CAN0 message identifier register 20H	CAN	924
C0MIDH21	CAN0 message identifier register 21H	CAN	924
C0MIDH22	CAN0 message identifier register 22H	CAN	924