Renesas Electronics America Inc - UPD70F3822GB-GAH-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, CSI, EBI/EMI, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	45
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 10x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3822gb-gah-ax

(9) Real-time counter (for watch)

The real-time counter counts the reference time (one second) for watch counting based on the subclock (32.768 kHz) or main clock. This can simultaneously be used as the interval timer based on the main clock. Hardware counters dedicated to year, month, day of week, day, hour, minute, and second are provided, and can count up to 99 years.

(10) Watchdog timer 2

A watchdog timer is provided on chip to detect inadvertent program loops, system abnormalities, etc.
The internal oscillation clock, the main clock, or the subclock can be selected as the source clock.
Watchdog timer 2 generates a non-maskable interrupt request signal (INTWDT2) or a system reset signal (WDT2RES) after an overflow occurs.

(11) Serial interface

The V850ES/JC3-H and V850ES/JE3-H include three kinds of serial interfaces (asynchronous serial interface C (UARTC), 3-wire variable-length serial interface F (CSIF), and an I^2C bus interface (I^2C)), a CAN controller (CAN)[Note1], and a USB function controller (USBF).
UARTC transfers data via the TXDC0, TXDC2 to TXDC4 pins and RXDC0, RXDC2 to RXDC4 pins.
CSIF transfers data via the SOF0, SOF2 to SOF4 pins, SIF0, SIF2 to SIF4 pins, and $\overline{\text{SCKF0}}$, $\overline{\text{SCKF2}}$ to $\overline{\text{SCKF4}}$ pins.
In the case of I^2C, data is transferred via the (SDA00)[Note2] , SDA01 and (SCL00)[Note2] , SCL01 pins.
CAN[Note1] transfers data via the CRXD[Note1] and CTXD0[Note1] pins.
USBF transfers data via the UDMF and UDPF pins.

Notes1. μPD70F3819, 70F3825 only
2. V850ES/JC3-H (48 pin), V850ES/JE3-H only

(12) A/D converter

This 10-bit A/D converter includes 10/6/5 analog input pins. Conversion is performed using the successive approximation method.

(13) D/A converter (V850ES/JC3-H (48 pin), JE3-H only)

A one-channel, 8-bit-resolution D/A converter that uses the R-2R ladder method is provided on chip.

(14) DMA controller

A 4-channel DMA controller is provided on chip. This controller transfers data between the internal RAM, on-chip peripheral I/O devices, and external memory in response to interrupt requests sent by on-chip peripheral I/O devices.

(15) Key interrupt function

A key interrupt request signal (INTKR) can be generated by inputting a falling edge to the key input pins (4 channels).

(16) Real-time output function

The real-time output function transfers preset 4-bit data to output latches upon the occurrence of a timer compare register match signal.

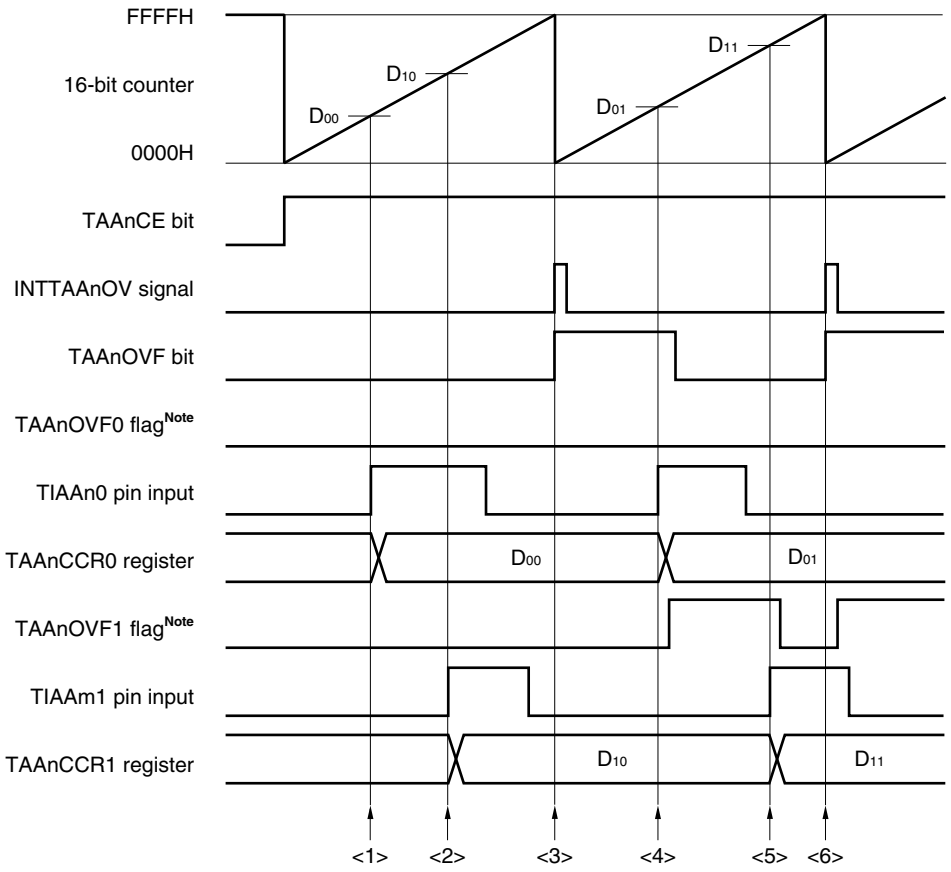
(b) Batch write

In this mode, data is transferred all at once from the TAAnCCR0 and TAAnCCR1 registers to the CCR0 and CCR1 buffer registers during timer operation. This data is transferred upon a match between the value of the CCR0 buffer register and the value of the 16-bit counter. Transfer is enabled by writing to the TAAnCCR1 register. Whether to enable or disable the next transfer timing is controlled by writing or not writing to the TAAnCCR1 register.

In order for the set value when the TAAnCCR0 and TAAnCCR1 registers are rewritten to become the 16-bit counter comparison value (in other words, in order for this value to be transferred to the CCR0 and CCR1 buffer registers), it is necessary to rewrite the TAAnCCR0 register and then write to the TAAnCCR1 register before the 16-bit counter value and the CCR0 buffer register value match. Therefore, the values of the TAAnCCR0 and TAAnCCR1 registers are transferred to the CCR0 and CCR1 buffer registers upon a match between the count value of the 16-bit counter and the value of the CCR0 buffer register. Thus even when wishing only to rewrite the value of the TAAnCCR0 register, also write the same value (same as preset value of the TAAnCCR1 register) to the TAAnCCR1 register.

(b) When using capture/compare register as capture register

Figure 6-38. Software Processing Flow in Free-Running Timer Mode (Capture Function) (1/2)



Remark n = 0 to 2
m = 2 (V850ES/JC3-H)
m = 0 to 2 (V850ES/JE3-H)

Figure 6-46. Example of Timing in Free-Running Mode (Capture/Compare Used Together)

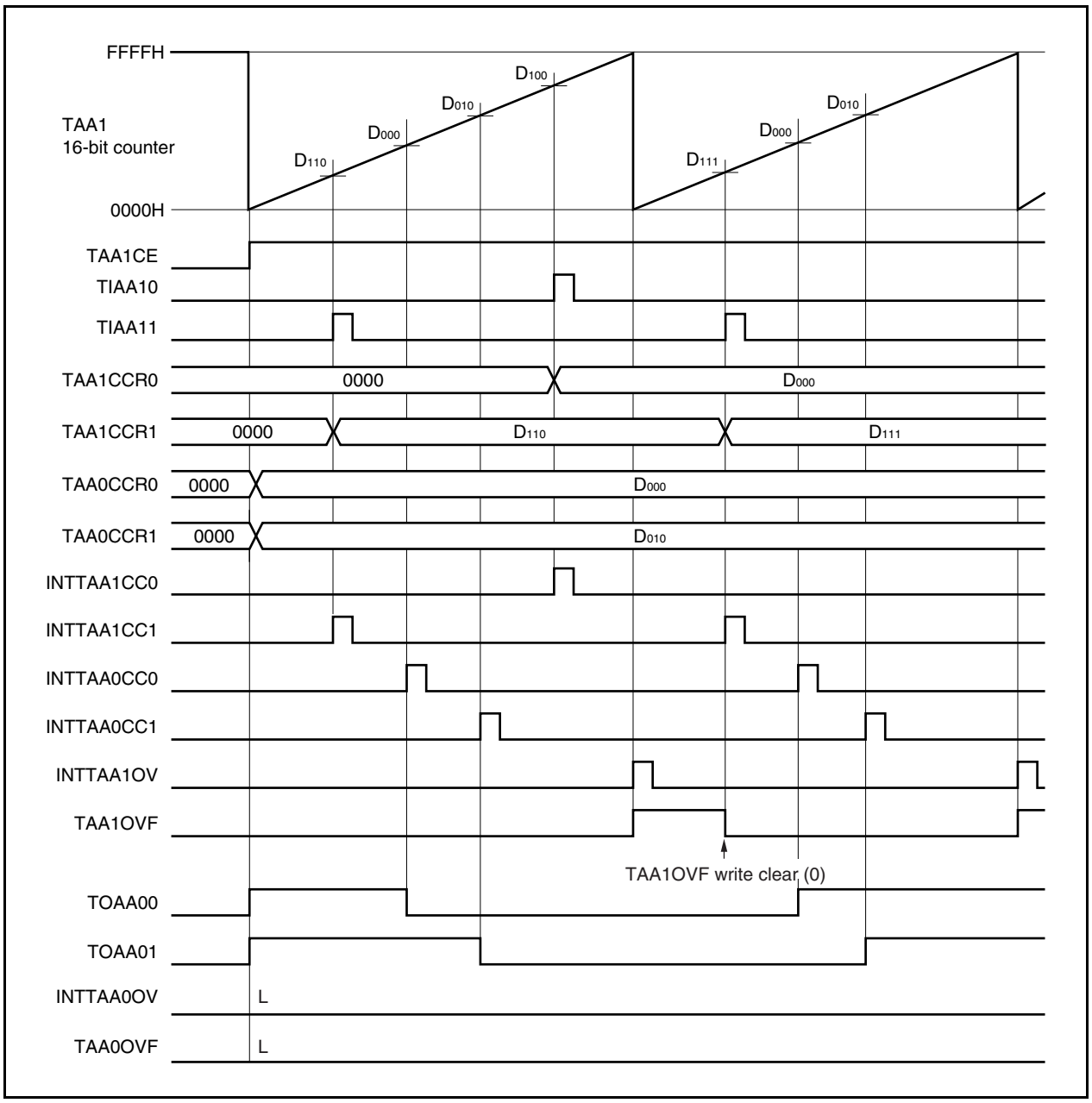


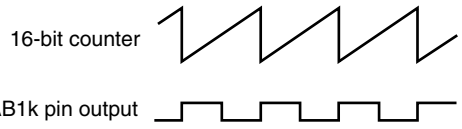
Figure 7-26. Setting of Registers in PWM Output Mode (2/3)

(c) TAB1 I/O control register 0 (TAB1IOC0)

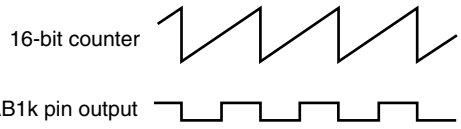
	TAB1OL3	TAB1OE3	TAB1OL2	TAB1OE2	TAB1OL1	TAB1OE1	TAB1OL0	TAB1OE0
TAB1IOC0	0/1	0/1	0/1	0/1	0/1	0/1	0/1 Note	0/1 Note

- TAB1OE0: 0: Disable TOAB10 pin output / 1: Enable TOAB10 pin output
- TAB1OL0: Setting of output level while operation of TOAB10 pin is disabled / 0: Low level / 1: High level
- TAB1OE1: 0: Disable TOAB11 pin output / 1: Enable TOAB11 pin output
- TAB1OL1: Specification of active level of TOAB11 pin output / 0: Active-high / 1: Active-low
- TAB1OE2: 0: Disable TOAB12 pin output / 1: Enable TOAB12 pin output
- TAB1OL2: Specification of active level of TOAB12 pin output / 0: Active-high / 1: Active-low
- TAB1OE3: 0: Disable TOAB13 pin output / 1: Enable TOAB13 pin output
- TAB1OL3: Specification of active level of TOAB13 pin output / 0: Active-high / 1: Active-low

- When TAB1OLk bit = 0



- When TAB1OLk bit = 1



(d) TAB1 I/O control register 2 (TAB1IOC2)

	TAB1EES1	TAB1EES0	TAB1ETS1	TAB1ETS0				
TAB1IOC2	0	0	0	0	0/1	0/1	0	0

- TAB1EES1, TAB1EES0: Select valid edge of external event count input.

(e) TAB1 counter read buffer register (TAB1CNT)

The value of the 16-bit counter can be read by reading the TAB1CNT register.

Note Clear this bit to 0 when the TOAB10 pin is not used in the PWM output mode.

In order to transfer data from the TT0CCRn register to the CCRn buffer register, the TT0CCR1 register must be written.

To change both the cycle and active level width of the PWM waveform at this time, first set the cycle to the TT0CCR0 register and then set the active level width to the TT0CCR1 register.

To change only the cycle of the PWM waveform, first set the cycle to the TT0CCR0 register, and then write the same value (same as preset value of the TT0CCR1 register) to the TT0CCR1 register.

To change only the active level width (duty factor) of the PWM waveform, only the TT0CCR1 register has to be set.

After data is written to the TT0CCR1 register, the value written to the TT0CCRn register is transferred to the CCRn buffer register in synchronization with clearing of the 16-bit counter, and is used as the value compared with the 16-bit counter.

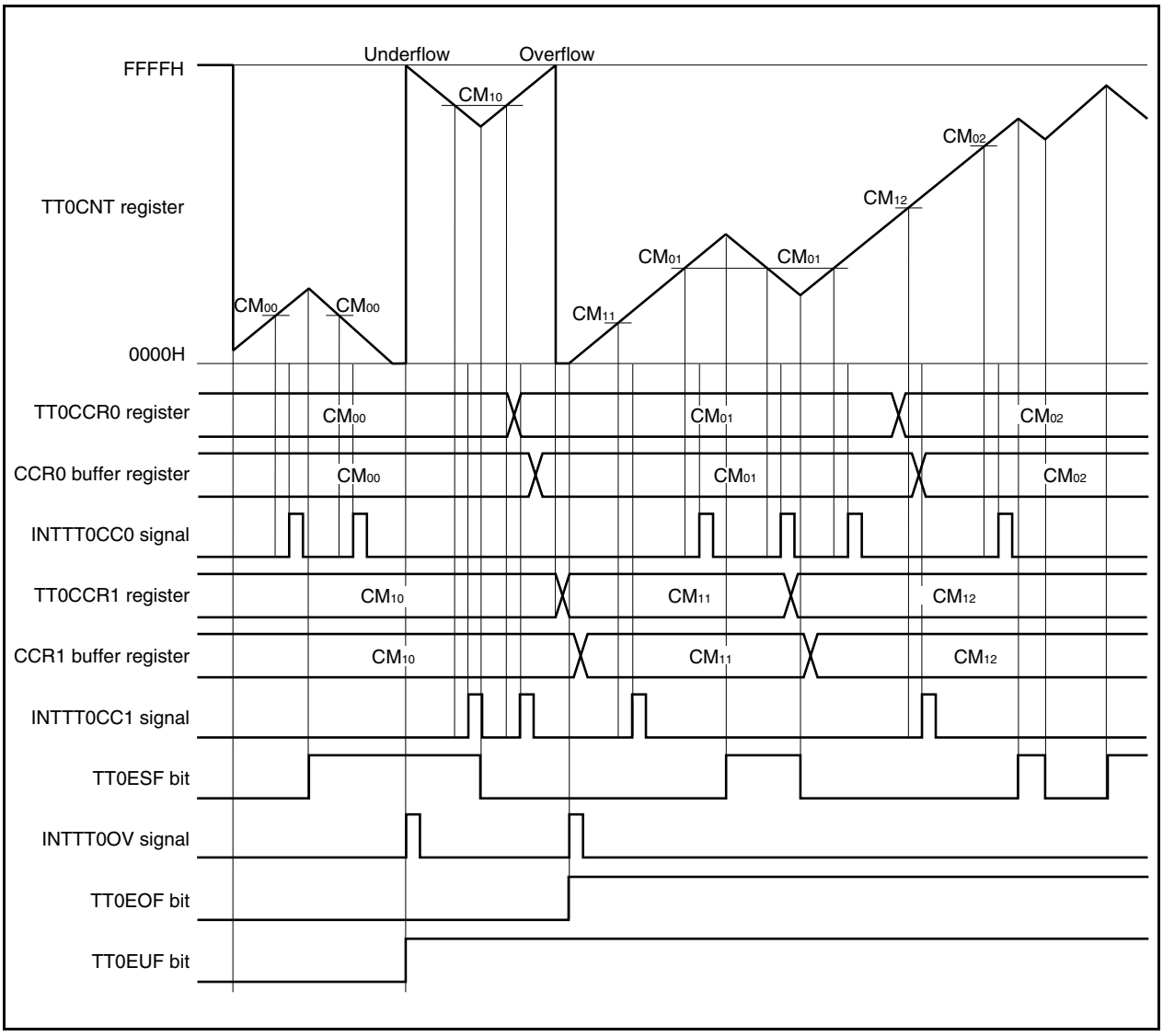
To write the TT0CCR0 or TT0CCR1 register again after writing the TT0CCR1 register once, do so after the INTTT0CC0 signal is generated. Otherwise, the value of the CCRn buffer register may become undefined because the timing of transferring data from the TT0CCRn register to the CCRn buffer register conflicts with writing the TT0CCRn register.

Remark n = 0, 1

(b) Basic timing 2

[Register setting condition]

- TT0CTL2.TT0ECM1 and TT0CTL2.TT0ECM0 bits = 00
  The 16-bit counter is not cleared even when its count value matches the value of the CCRn buffer register (a = 0, 1).
- TT0CTL2.TT0LDE bit = 0
  The set value of the TT0CCR0 register is not transferred to the 16-bit counter after the counter underflows.
- TT0IOC3.TT0SCE bit = 0, and TT0IOC3.TT0ECS1 and TT0IOC3.TT0ECS0 bits = 00
  Specification of clearing the 16-bit counter when the edge of the encoder clear input signal (TECR0 pin) is detected (no edge specified)



10.4.3 Interrupt culling function

- The interrupts to be culled are INTTAB1CC0 (crest interrupt) and INTTAB1OV (valley interrupt).
- The TAB1OPT1.TAB1ICE bit is used to enable output of the INTTAB1CC0 interrupt and the number of times the interrupt is to be culled.
- The TAB1OPT1.TAB1IOE bit is used to enable output of the INTTAB1OV interrupt and the number of times the interrupt is to be culled.
- The TAB1OPT1.TAB1ID4 to TAB1OPT1.TAB1ID0 bits are used to specify the number of counts by which a specified interrupt is to be culled. The interrupt is masked for the duration of the specified number of counts and is generated at the next interrupt timing.
- The TAB1OPT2.TAB1RDE bit is used to specify whether transfer is to be culled or not.
  If it is specified that transfer is to be culled, transfer is executed at the same timing as the interrupt output after culling.
  If it is specified that transfer is not to be culled, transfer is executed at the transfer timing after the TAB1CCR1 register has been written.
- The TAB1OPT0.TAB1CMS bit is used to specify whether the registers with a transfer function are batch rewritten or anytime rewritten.
  The values of the registers are updated in synchronization with transfer when the TAB1CMS bit is 0. When the TAB1CMS bit is 1, the values of the registers are immediately updated when a new value is written to the registers.
  Transfer is performed from the TAB1CCRm register to the CCRm buffer register in synchronization with the interrupt culling timing.

Cautions 1. When using the interrupt culling function in the batch rewrite mode (transfer mode), execute the function in the intermittent batch rewrite mode (transfer culling mode).

2. The interrupt is generated at the timing after culling.

Remark m = 1 to 3

CSIFn includes the following hardware.

Table 17-1. Configuration of CSIFn

Item	Configuration
Registers	CSIFn receive data register (CFnRX) CSIFn transmit data register (CFnTX) CSIFn control register 0 (CFnCTL0) CSIFn control register 1 (CFnCTL1) CSIFn control register 2 (CFnCTL2) CSIFn status register (CFnSTR)

(1) CSIFn receive data register (CFnRX)

The CFnRX register is a 16-bit buffer register that holds receive data.

This register is read-only, in 16-bit units.

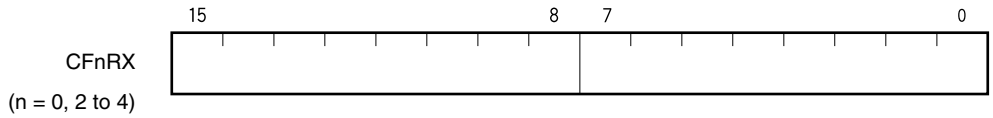
The receive operation is started by reading the CFnRX register in the reception enabled status.

If the transfer data length is 8 bits, the lower 8 bits of this register are read-only in 8-bit units as the CFnRXL register.

Reset sets this register to 0000H.

In addition to reset input, the CFnRX register can be initialized by clearing (to 0) the CFnPWR bit of the CFnCTL0 register.

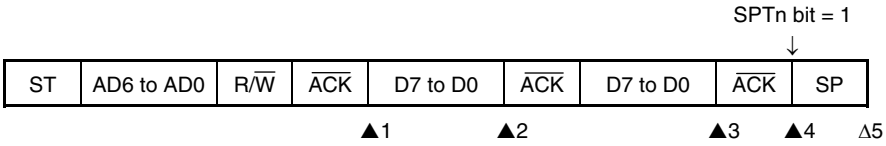
After reset: 0000H R Address: CF0RX FFFFFD04H, CF2RX FFFFFD24H,
CF3RX FFFFFD34H[Note], CF4RX FFFFFD44H



Note V850ES/JC3-H (48 pin), V850ES/JE3-H only

(3) Start ~ Code ~ Data ~ Data ~ Stop (extension code transmission)

<1> When WTIMn bit = 0



▲1: IICSn register = 1010X110B

▲2: IICSn register = 1010X000B

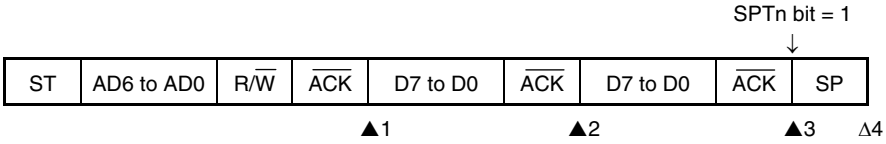
▲3: IICSn register = 1010X000B (WTIMn bit = 1)

▲4: IICSn register = 1010XX00B

Δ 5: IICSn register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIEn bit = 1
X: don't care

<2> When WTIMn bit = 1



▲1: IICSn register = 1010X110B

▲2: IICSn register = 1010X100B

▲3: IICSn register = 1010XX00B

Δ 4: IICSn register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIEn bit = 1
X: don't care

(4) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

<1> When WTIMn bit = 0 (after restart, address mismatch (= not extension code))

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP
			▲1		▲2					▲3		Δ4

▲1: IICSn register = 0010X010B

▲2: IICSn register = 0010X000B

▲3: IICSn register = 00000X10B

Δ 4: IICSn register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIEn bit = 1

X: don't care

<2> When WTIMn bit = 1 (after restart, address mismatch (= not extension code))

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP
			▲1	▲2		▲3				▲4		Δ5

▲1: IICSn register = 0010X010B

▲2: IICSn register = 0010X110B

▲3: IICSn register = 0010XX00B

▲4: IICSn register = 00000X10B

Δ 5: IICSn register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIEn bit = 1

X: don't care

19.9.2 Reading reception data

If it is necessary to consistently read data from the CAN message buffer by software, follow the recommended procedures shown in Figures 19-49 and 19-50.

While receiving a message, the CAN module sets the C0MCTRLm.DN bit two times, at the beginning of the processing to store data in the message buffer and at the end of this storing processing. During this storing processing, the C0MCTRLm.MUC bit of the message buffer is set (1) (refer to **Figure 19-29**).

Before the data is completely stored, the receive history list is written. During this data storing period (MUC bit = 1), the CPU is prohibited from rewriting the C0MCTRLm.RDY bit of the message buffer in which the data is to be stored. Completion of this data storing processing may be delayed by a CPU's access to any message buffer.

Remark m = 0 to 31

Figure 19-29. DN and MUC Bit Setting Period (in Standard ID Format)

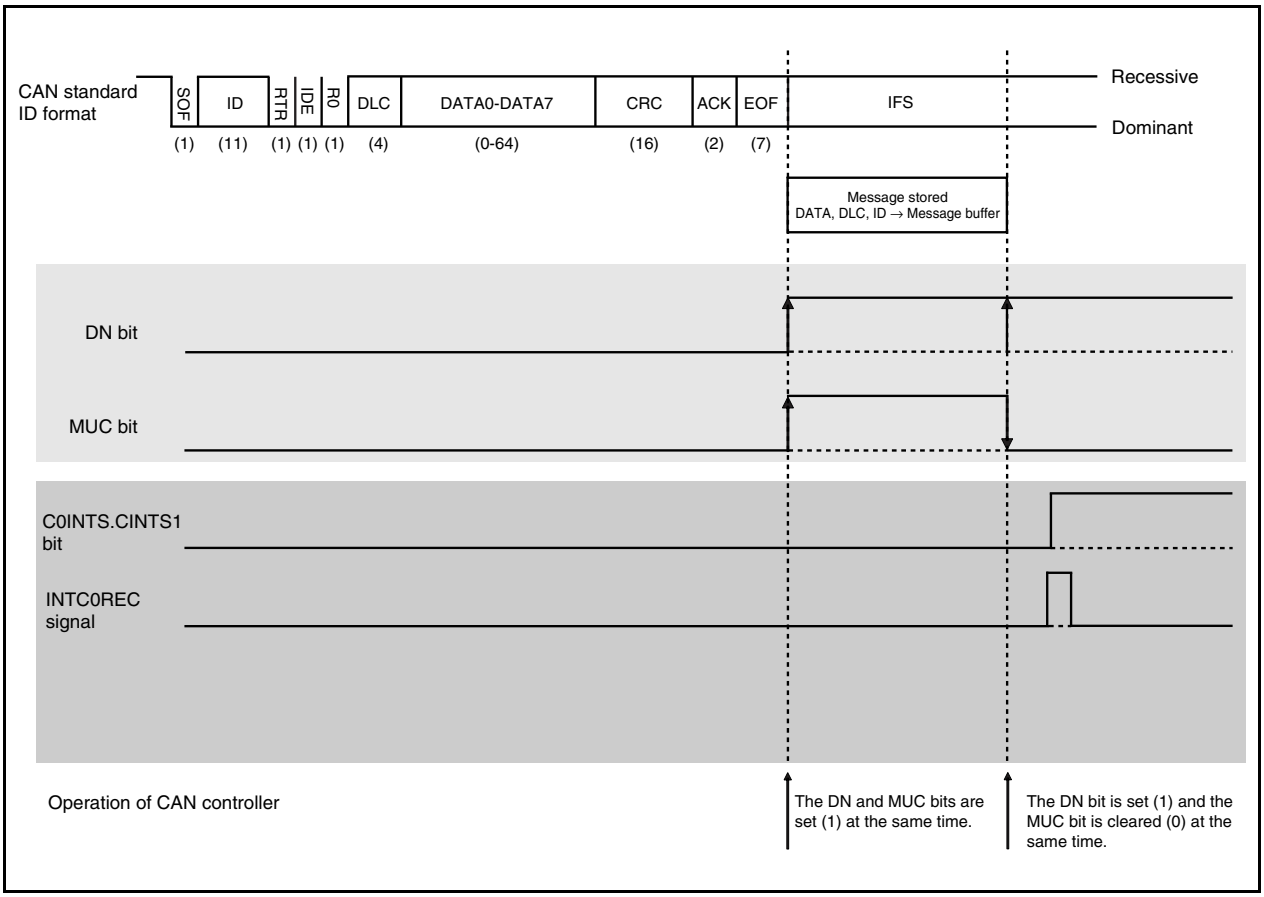


Table 19-22. Settable Bit Rate Combinations (3/3)

Valid Bit Rate Setting					C0BTR Register Setting Value		Sampling Point (Unit: %)
DBT Length	SYNC SEGMENT	PROP SEGMENT	PHASE SEGMENT1	PHASE SEGMENT2	TSEG13 to TSEG10	TSEG22 to TSEG20	
11	1	2	4	4	0101	011	63.6
11	1	4	3	3	0110	010	72.7
11	1	6	2	2	0111	001	81.8
11	1	8	1	1	1000	000	90.9
10	1	1	4	4	0100	011	60.0
10	1	3	3	3	0101	010	70.0
10	1	5	2	2	0110	001	80.0
10	1	7	1	1	0111	000	90.0
9	1	2	3	3	0100	010	66.7
9	1	4	2	2	0101	001	77.8
9	1	6	1	1	0110	000	88.9
8	1	1	3	3	0011	010	62.5
8	1	3	2	2	0100	001	75.0
8	1	5	1	1	0101	000	87.5
7Note	1	2	2	2	0011	001	71.4
7Note	1	4	1	1	0100	000	85.7
6Note	1	1	2	2	0010	001	66.7
6Note	1	3	1	1	0011	000	83.3
5Note	1	2	1	1	0010	000	80.0
4Note	1	1	1	1	0001	000	75.0

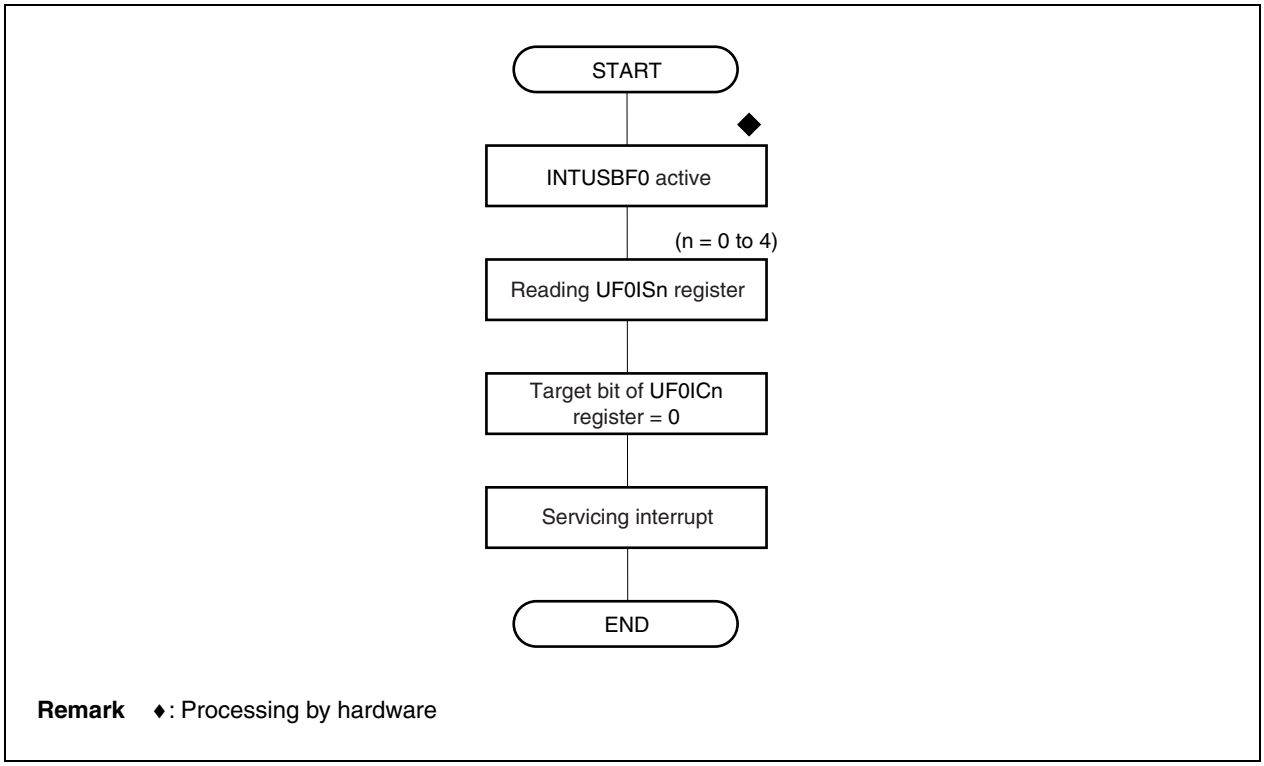
Note Setting with a DBT value of 7 or less is valid only when the value of the C0BRP register is other than 00H.

Caution The values in Table 19-22 do not guarantee the operation of the network system. Thoroughly check the effect on the network system, taking into consideration oscillation errors and delays of the CAN bus and CAN transceiver.

20.9.2 Interrupt servicing

The following flowchart illustrates how an interrupt is serviced.

Figure 20-18. Interrupt Servicing



Remark ♦: Processing by hardware

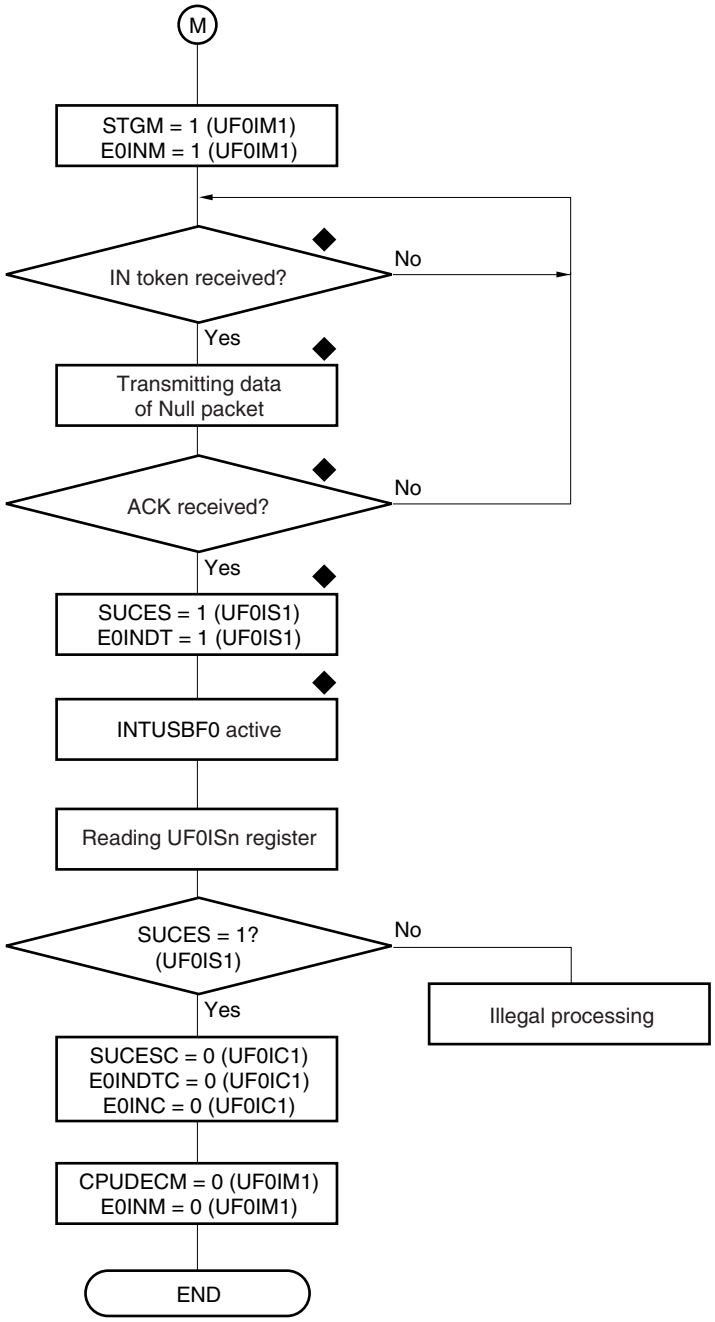
The following bits of the UF0ISn register are automatically cleared by hardware when a given condition is satisfied (n = 0 to 4).

- E0INDT, E0ODT, SUCES, STG, and CPUDEC bits of UF0IS1 register
- BKI2DT, BKI1DT, and IT1DT bits of UF0IS2 register
- BKO2FL, BKO2DT, BKO1FL, and BKO1DT bits of UF0IS3 register

Because clearing an interrupt source by the UF0ICn register is given a lower priority than setting an interrupt source by hardware, the interrupt source may not be cleared depending on the timing (n = 0 to 4).

Figure 20-24. CPUDEC Request for Control Transfer (10/12)

(c) Control transfer (write) (4/4)



Remarks 1. n = 0, 1

2. ♦: Processing by hardware

22.3 Maskable Interrupts

Maskable interrupt request signals can be masked by interrupt control registers. The V850ES/JC3-H and V850ES/JE3-H have 61 to 71 maskable interrupt sources.

If two or more maskable interrupt request signals are generated at the same time, they are acknowledged according to the default priority. In addition to the default priority, eight levels of priorities can be specified by using the interrupt control registers (programmable priority control).

When an interrupt request signal has been acknowledged, the acknowledgment of other maskable interrupt request signals is disabled and the interrupt disabled (DI) status is set.

When the EI instruction is executed in an interrupt service routine, the interrupt enabled (EI) status is set, which enables servicing of interrupts having a higher priority than the interrupt request signal in progress (specified by the interrupt control register). Note that only interrupts with a higher priority will have this capability; interrupts with the same priority level cannot be nested.

To enable multiple interrupts, however, save EIPC and EIPSW to memory or general-purpose registers before executing the EI instruction, and execute the DI instruction before the RETI instruction to restore the original values of EIPC and EIPSW.

22.3.1 Operation

If a maskable interrupt occurs, the CPU performs the following processing, and transfers control to a handler routine.

<1> Saves the restored PC to EIPC.
<2> Saves the current PSW to EIPSW.
<3> Writes an exception code to the lower halfword of ECR (EICC).
<4> Sets the PSW. ID bit to 1 and clears the PSW. EP bit to 0.
<5> Sets the handler address corresponding to each interrupt to the PC, and transfers control.

The maskable interrupt request signal masked by INTC and the maskable interrupt request signal generated while another interrupt is being serviced (while the PSW.NP bit = 1 or the PSW.ID bit = 1) are held pending inside INTC. In this case, servicing a new maskable interrupt is started in accordance with the priority of the pending maskable interrupt request signal if either the maskable interrupt is unmasked or the NP and ID bits are set to 0 by using the RETI or LDSR instruction.

How maskable interrupts are serviced is illustrated below.

22.3.2 Restore

Recovery from maskable interrupt servicing is carried out by the RETI instruction.

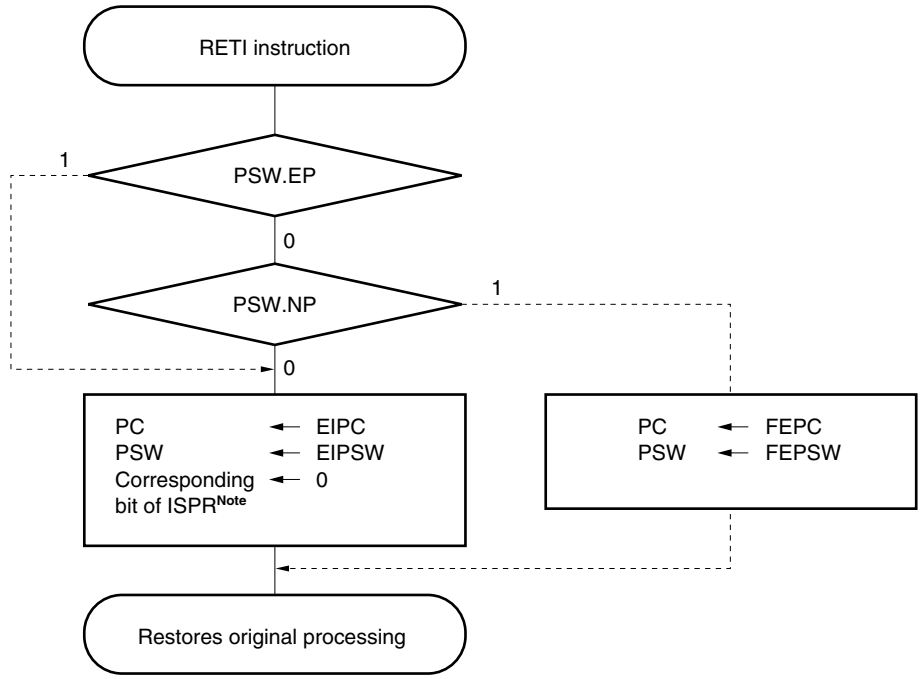
When the RETI instruction is executed, the CPU performs the following processing, and transfers control to the address of the restored PC.

<1> Loads the restored PC and PSW from EIPC and EIPSW because the PSW.EP bit is 0 and the PSW.NP bit is 0.

<2> Transfers control back to the address of the restored PC and PSW.

The processing of the RETI instruction is shown below.

Figure 22-6. RETI Instruction Processing



Note For the ISPR register, see **22.3.6 In-service priority register (ISPR)**.

Caution When the EP and NP bits are changed by the LDSR instruction during maskable interrupt servicing, in order to restore the PC and PSW correctly during recovery by the RETI instruction, it is necessary to set the EP bit back to 0 and the NP bit back to 0 using the LDSR instruction immediately before the RETI instruction.

Remark The solid line shows the CPU processing flow.

CHAPTER 32 ELECTRICAL SPECIFICATIONS

32.1 Absolute Maximum Ratings

(T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	$V_{DD} = EV_{DD} = UV_{DD} = AV_{REF0} = AV_{REF1}$	−0.5 to +4.6	V
	EV_{DD}	$V_{DD} = EV_{DD} = UV_{DD} = AV_{REF0} = AV_{REF1}$	−0.5 to +4.6	V
	UV_{DD}	$V_{DD} = EV_{DD} = UV_{DD} = AV_{REF0} = AV_{REF1}$	−0.5 to +4.6	V
	AV_{REF0}	$V_{DD} = EV_{DD} = UV_{DD} = AV_{REF0} = AV_{REF1}$	−0.5 to +4.6	V
	AV_{REF1}	$V_{DD} = EV_{DD} = UV_{DD} = AV_{REF0} = AV_{REF1}$	−0.5 to +4.6	V
	V_{SS}	$V_{SS} = AV_{SS}$	−0.5 to +0.5	V
	AV_{SS}	$V_{SS} = AV_{SS}$	−0.5 to +0.5	V
Input voltage	V_{I1}	P60 to P65, P92 to P94, P96, P97, P910 to P913, PDL5, $\overline{\text{RESET}}$, FLMD0	−0.5 to EV_{DD} + 0.5 Note 1	V
	V_{I2}	UDMF, UDPF	−0.5 to UV_{DD} + 0.5 Note 1	V
	V_{I3}	P10	−0.5 to AV_{REF1} + 0.5 Note 1	V
	V_{I4}	X1, X2, XT1, XT2	−0.5 to V_{RO} Note 2 + 0.5 Note 1	V
	V_{I5}	P02, P03, P30 to P37, P40 to P42, P52 to P56	−0.5 to +6.0	V
Analog input voltage	V_{IAN}	P70 to P79	−0.5 to AV_{REF0} + 0.5 Note 1	V

Cautions 1. Do not directly connect the output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open-drain pins or open-collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage. Therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

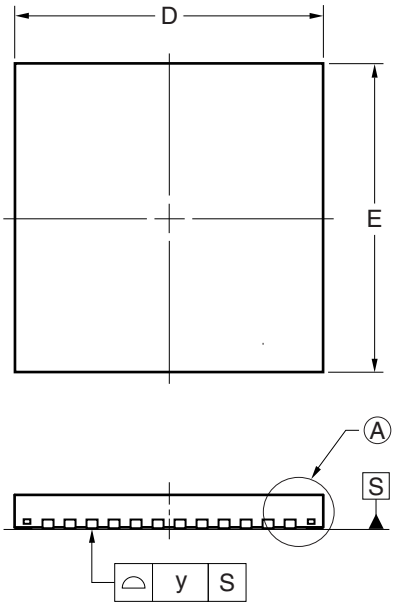
The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

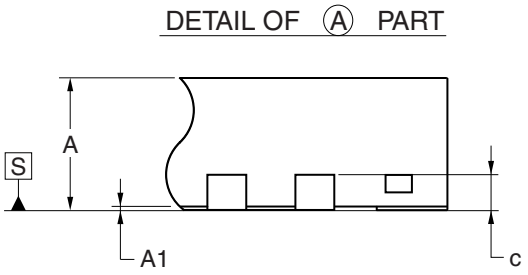
Notes 1. Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

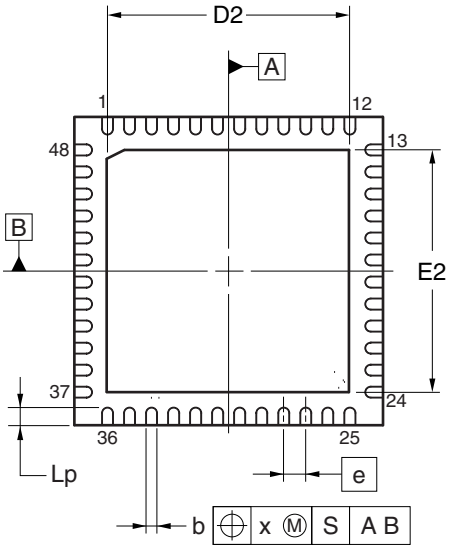
2. On-chip regulator output voltage (2.5 V (TYP.))

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

48-PIN PLASTIC WQFN(7x7)







(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.05
E	7.00±0.05
D2	5.50
E2	5.50
A	0.75±0.05
A1	0.00 to 0.02
b	$0.25^{+0.05}_{-0.07}$
c	0.20±0.05
e	0.50
Lp	0.40±0.10
x	0.05
y	0.05

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Symbol	Name	Unit	Page
RC1WEEK	Day-of-week count register	RTC	600
RC1YEAR	Year count register	RTC	601
RCM	Internal oscillation mode register	CG	160
RECIC0	Interrupt control register	INTC	1222
RESF	Reset source flag register	Reset	1270
RTBH0	Real-time output buffer register 0H	RTO	626
RTBL0	Real-time output buffer register 0L	RTO	626
RTC0IC	Interrupt control register	INTC	1222
RTC1IC	Interrupt control register	INTC	1222
RTC2IC	Interrupt control register	INTC	1222
RTPC0	Real-time output port control register 0	RTO	628
RTPM0	Real-time output port mode register 0	RTO	627
SELCNT0	Selector operation control register 0	Timer	280
SVA0	Slave address register 0	I^2C	787
SVA1	Slave address register 1	I^2C	787
SYS	System status register	CPU	787
TAA0CCIC0	Interrupt control register	INTC	1222
TAA0CCIC1	Interrupt control register	INTC	1222
TAA0CCR0	TAA0 capture/compare register 0	Timer	181
TAA0CCR1	TAA0 capture/compare register 1	Timer	183
TAA0CNT	TAA0 counter read buffer register	Timer	185
TAA0CTL0	TAA0 control register 0	Timer	172
TAA0CTL1	TAA0 control register 1	Timer	173
TAA0IOC0	TAA0 I/O control register 0	Timer	175
TAA0IOC1	TAA0 I/O control register 1	Timer	176
TAA0IOC2	TAA0 I/O control register 2	Timer	177
TAA0IOC4	TAA0 I/O control register 4	Timer	178
TAA0OPT0	TAA0 option register 0	Timer	179
TAA0OPT1	TAA0 option register 1	Timer	180
TAA0OVIC	Interrupt control register	INTC	1222
TAA1CCIC0	Interrupt control register	INTC	1222
TAA1CCIC1	Interrupt control register	INTC	1222
TAA1CCR0	TAA1 capture/compare register 0	Timer	181
TAA1CCR1	TAA1 capture/compare register 1	Timer	183
TAA1CNT	TAA1 counter read buffer register	Timer	185
TAA1CTL0	TAA1 control register 0	Timer	172
TAA1CTL1	TAA1 control register 1	Timer	173
TAA1IOC0	TAA1I/O control register 0	Timer	175
TAA1IOC1	TAA1I/O control register 1	Timer	176
TAA1IOC2	TAA1I/O control register 2	Timer	177
TAA1IOC4	TAA1I/O control register 4	Timer	178
TAA1OPT0	TAA1 option register 0	Timer	179
TAA1OVIC	Interrupt control register	INTC	1222