Renesas Electronics America Inc - UPD70F3823GB-GAH-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, CSI, EBI/EMI, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	45
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 10x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3823gb-gah-ax

(2) Command register (PRCMD)

The PRCMD register is an 8-bit register that protects the registers that may seriously affect the application system from being written, so that the system does not inadvertently stop due to a program hang-up. The first write access to a special register is valid after data has been written in advance to the PRCMD register. In this way, the value of the special register can be rewritten only in a specific sequence, so as to protect the register from an illegal write access.

The PRCMD register is write-only, in 8-bit units (undefined data is read when this register is read).

After reset: Undefined W Address: FFFFF1FCH

	7	6	5	4	3	2	1	0
PRCMD	REG7	REG6	REG5	REG4	REG3	REG2	REG1	REG0

Figure 7-22. Register Setting for Operation in One-Shot Pulse Output Mode (2/3)

(c) TAB1 I/O control register 0 (TAB1IOC0)

	TAB1OL3	TAB1OE3	TAB1OL2	TAB1OE2	TAB1OL1	TAB1OE1	TAB1OL0	TAB1OE0
TAB1IOC0	0/1	0/1	0/1	0/1	0/1	0/1	0/1Note	0/1Note

0: Disable TOAB10 pin output
1: Enable TOAB10 pin output

Setting of output level while operation of TOAB10 pin is disabled
0: Low level
1: High level

0: Disable TOAB11 pin output
1: Enable TOAB11 pin output

Specification of active level of TOAB11 pin output
0: Active-high
1: Active-low

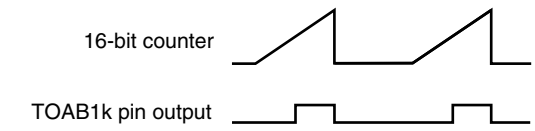
0: Disable TOAB12 pin output
1: Enable TOAB12 pin output

Specification of active level of TOAB12 pin output
0: Active-high
1: Active-low

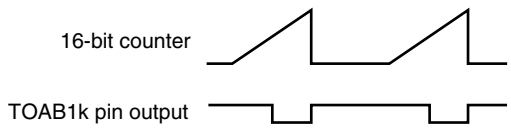
0: Disable TOAB13 pin output
1: Enable TOAB13 pin output

Specification of active level of TOAB13 pin output
0: Active-high
1: Active-low

• When TAB1OLk bit = 0



• When TAB1OLk bit = 1



(d) TAB1 I/O control register 2 (TAB1IOC2)

	TAB1EES1	TAB1EES0	TAB1ETS1	TAB1ETS0				
TAB1IOC2	0	0	0	0	0/1	0/1	0/1	0/1

Select valid edge of external trigger input

Select valid edge of external event count input

(e) TAB1 counter read buffer register (TAB1CNT)

The value of the 16-bit counter can be read by reading the TAB1CNT register.

Note Clear this bit to 0 when the TOAB10 pin is not used in the one-shot pulse output mode.

(4) TMT0 I/O control register 0 (TT0IOC0)

The TT0IOC0 register is an 8-bit register that controls the timer output (TOT00, TOT01 pins).

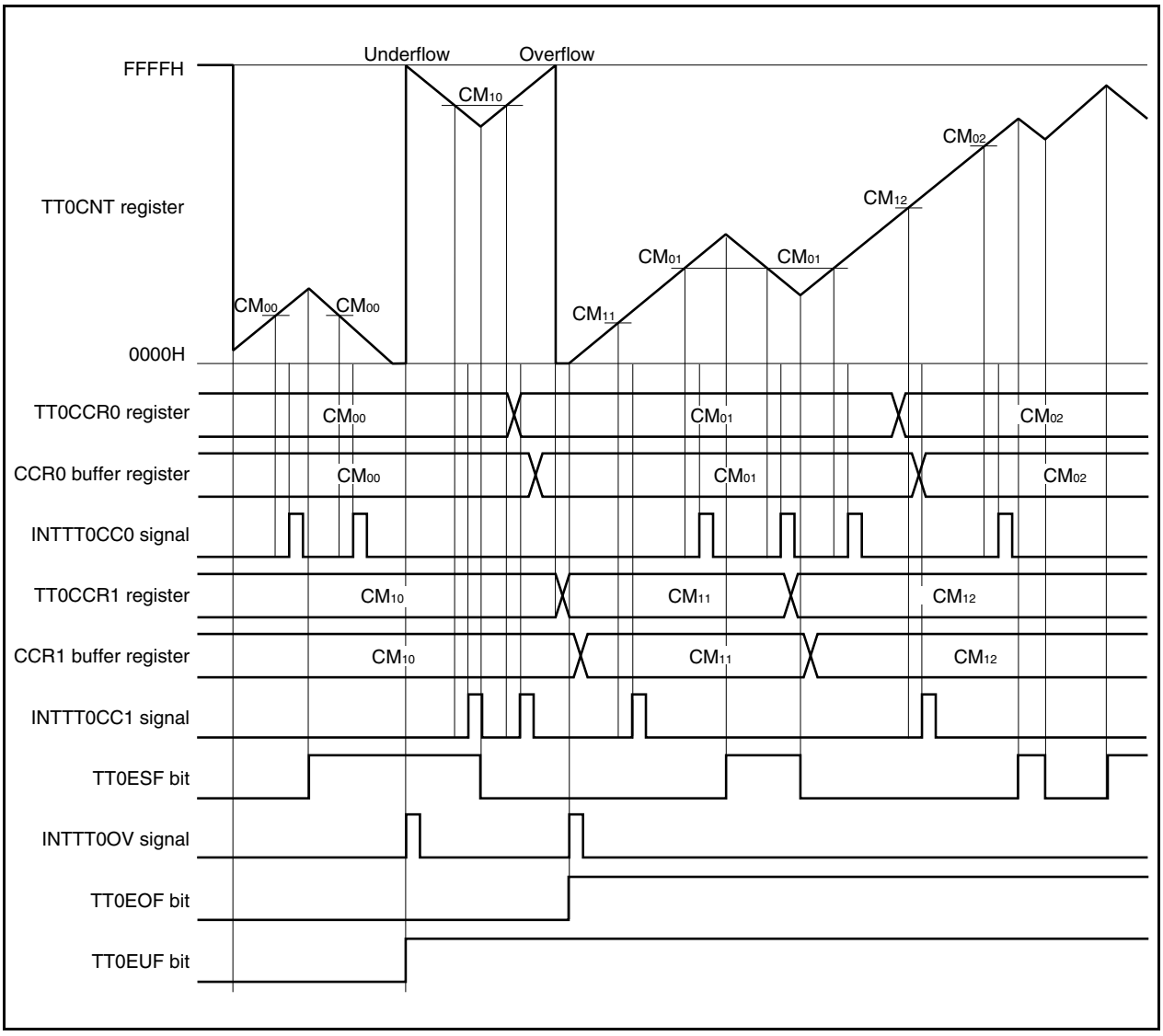
This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

(b) Basic timing 2

[Register setting condition]

- TT0CTL2.TT0ECM1 and TT0CTL2.TT0ECM0 bits = 00
  The 16-bit counter is not cleared even when its count value matches the value of the CCRn buffer register (a = 0, 1).
- TT0CTL2.TT0LDE bit = 0
  The set value of the TT0CCR0 register is not transferred to the 16-bit counter after the counter underflows.
- TT0IOC3.TT0SCE bit = 0, and TT0IOC3.TT0ECS1 and TT0IOC3.TT0ECS0 bits = 00
  Specification of clearing the 16-bit counter when the edge of the encoder clear input signal (TECR0 pin) is detected (no edge specified)



When the 16-bit counter starts operating (TT0CE bit = 0 → 1), the set value of the TT0TCW register is transferred to the 16-bit counter and the counter starts operating.

When the count value of the 16-bit counter matches the value of the CCR0 buffer register, a compare match interrupt request signal (INTTT0CC0) is generated.

When the count value of the 16-bit counter matches the value of the CCR1 buffer register, a compare match interrupt request signal (INTTT0CC1) is generated.

The 16-bit counter is not cleared to 0000H even when its count value matches the value of the CCRn buffer register because the TT0ECM1 and TT0ECM0 bits = 00 (n = 0, 1).

10.4.6 A/D conversion start trigger output function

The V850ES/JC3-H and V850ES/JE3-H have a function to select four trigger sources (INTTAB1OV, INTTAB1CC0, INTTAA4CC0, INTTAA4CC1) to generate the A/D conversion start trigger signal (TABTADT0).

The trigger sources are specified by the TAB1OPT2.TAB1AT0 to TAB1OPT2.TAB1AT3 bits.

- TAB1AT0 bit = 1:
  A/D conversion start trigger signal generated when INTTAB1OV (counter underflow) occurs.
- TAB1AT1 bit = 1:
  A/D conversion start trigger signal generated when INTTAB1CC0 (cycle match) occurs.
- TAB1AT2 bit = 1:
  A/D conversion start trigger signal generated when INTTAA4CC0 (match of TAA4CCR0 register of TAA4 during tuning operation) occurs.
- TAB1AT3 bit = 1:
  A/D conversion start trigger signal generated when INTTAA4CC1 (match of TAA4CCR1 register of TAA4 during tuning operation) occurs.

The A/D conversion start trigger signals selected by the TAB1AT0 to TAB1AT3 bits are ORed and output. Therefore, two or more trigger sources can be specified at the same time.

The INTTAB1OV and INTTAB1CC0 signals selected by the TAB1AT0 and TAB1AT1 bits are culled interrupt signals.

Therefore, these signals are output after the interrupts have been culled and, unless interrupt output is enabled (by the TAB1OPT1.TAB1ICE and TAB1OPT1.TAB1IOE bits), the A/D conversion start trigger signal is not output.

The trigger sources (INTTAA4CC0 and INTTAA4CC1) from TAA4 have a function to mask the A/D conversion start trigger signal depending on the count-up/count-down status of the 16-bit counter, if so set by the TAB1AT2 and TAB1AT3 bits.

- TAB1ATM2 bit: Corresponds to the TAB1AT2 bit and controls INTTAA4CC0 (match interrupt signal) of TAA4.
  - TAB1ATM2 bit = 0: The A/D conversion start trigger signal is output when the 16-bit counter counts up (TAB1OPT0.TAB1CUF bit = 0), and the A/D conversion start trigger signal is not output when the 16-bit counter counts down (TAB1OPT0.TAB1CUF bit = 1).
  - TAB1ATM2 bit = 1: The A/D conversion start trigger signal is output when the 16-bit counter counts up (TAB1OPT0.TAB1CUF bit = 1), and the A/D conversion start trigger signal is not output when the 16-bit counter counts down (TAB1OPT0.TAB1CUF bit = 0).

- TAB1ATM3 bit: Corresponds to the TAB1AT3 bit and controls INTTAA4CC1 (match interrupt signal) of TAA4.
  - TAB1ATM3 bit = 0: The A/D conversion start trigger signal is output when the 16-bit counter counts up (TAB1OPT0.TAB1CUF bit = 0), and the A/D conversion start trigger signal is not output when the 16-bit counter counts down (TAB1OPT0.TAB1CUF bit = 1).
  - TAB1ATM3 bit = 1: The A/D conversion start trigger signal is output when the 16-bit counter counts up (TAB1OPT0.TAB1CUF bit = 1), and the A/D conversion start trigger signal is not output when the 16-bit counter counts down (TAB1OPT0.TAB1CUF bit = 0).

The TAB1ATM3, TAB1ATM2, and TAB1AT3 to TAB1AT0 bits can be rewritten while the timer is operating. If the bit that sets the A/D conversion start trigger signal is rewritten while the timer is operating, the new setting is immediately reflected in the output status of the A/D conversion start trigger signal. These control bits do not have a transfer function and can be used only in the anytime rewrite mode.

(4) Wait cancellation method

The four wait cancellation methods are as follows.

- By setting the IICCn.WRELn bit to 1
- By writing to the IICn register
- By start condition setting (IICCn.STTn bit = 1)[Note]
- By stop condition setting (IICCn.SPTn bit = 1)[Note]

Note Master only

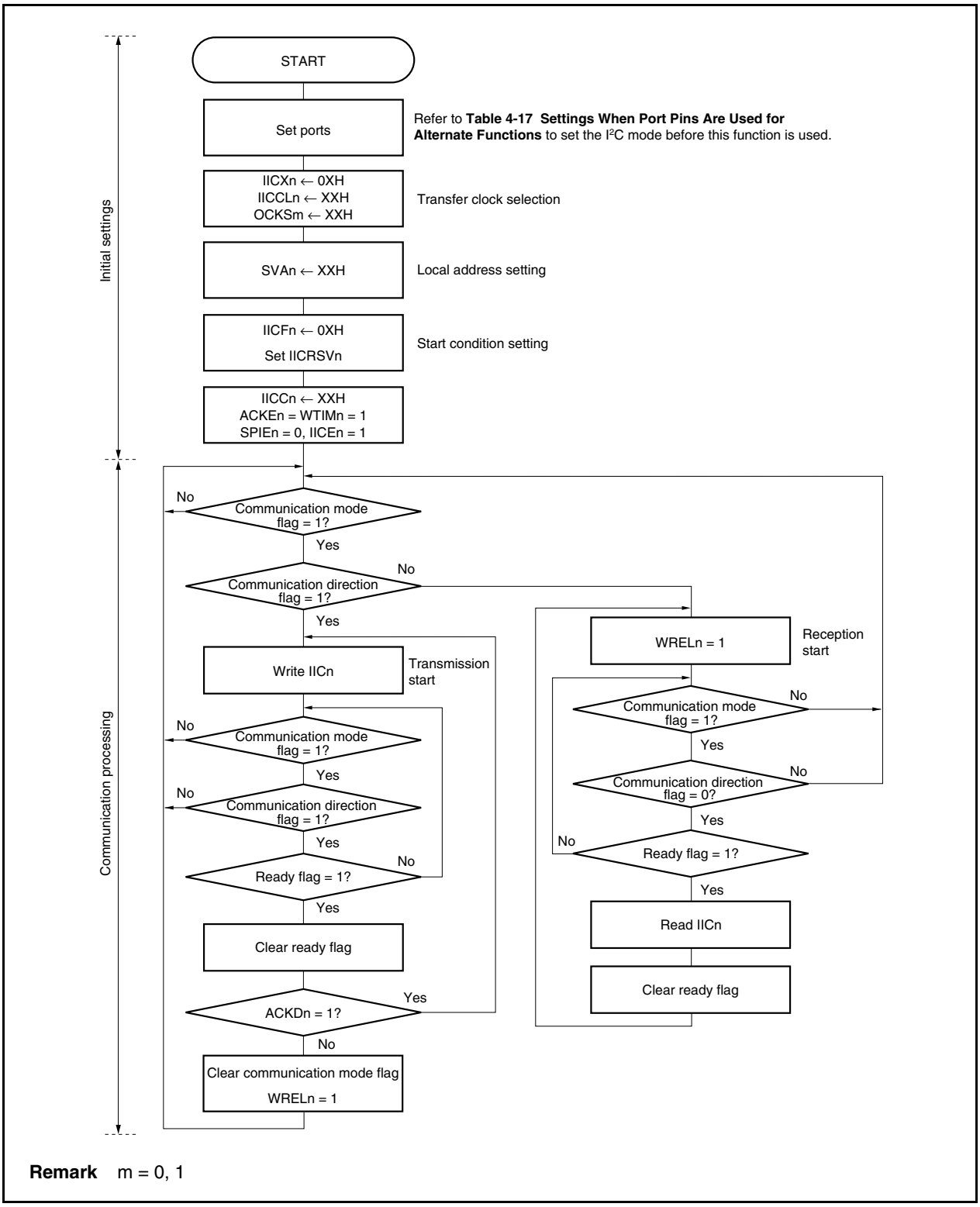
When an 8-clock wait has been selected (WTIMn bit = 0), whether or not $\overline{\text{ACK}}$ has been generated must be determined prior to wait cancellation.

(5) Stop condition detection

The INTIICn signal is generated when a stop condition is detected.

For reception, the required number of data is received and $\overline{ACK}$ is not returned for the next data immediately after transfer is complete. After that, the master device generates the stop condition or restart condition. This causes exit from communications.

Figure 18-21. Slave Operation Flowchart (1)



Remark m = 0, 1

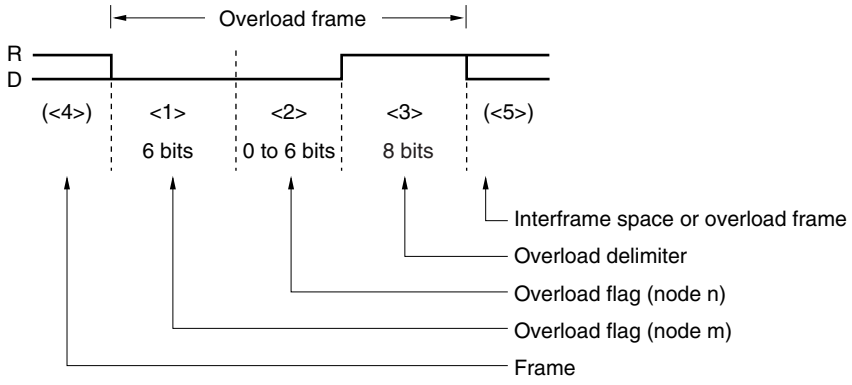
19.2.5 Overload frame

An overload frame is transmitted under the following conditions.

- When the receiving node has not completed the reception operation[Note]
- If a dominant level is detected at the first two bits during intermission
- If a dominant level is detected at the last bit (7th bit) of the end of frame or at the last bit (8th bit) of the error delimiter/overload delimiter

Note In this CAN controller, all reception frames can be loaded without outputting an overload frame because of the enough high-speed internal processing.

Figure 19-16. Overload Frame



Remark D: Dominant = 0
R: Recessive = 1
Node n ≠ node m

Table 19-8. Definition of Overload Frame Fields

No	Name	Bit Count	Definition
<1>	Overload flag	6	Outputs 6 dominant-level bits consecutively.
<2>	Overload flag from other node	0 to 6	The node that received an overload flag in the interframe space outputs an overload flag.
<3>	Overload delimiter	8	Outputs 8 recessive-level bits consecutively. If a dominant level is detected at the 8th bit, an overload frame is transmitted from the next bit.
<4>	Frame	–	Output following an end of frame, error delimiter, or overload delimiter.
<5>	Interframe space/overload frame	–	An interframe space or overload frame starts from here.

Table 19-16. Register Access Types (8/17)

Address	Register Name	Symbol	R/W	Bit Manipulation Units			After Reset
				1 Bit	8 Bits	16 Bits	
03FEC280H	CAN0 message data byte 01 register 12	C0MDATA0112	R/W			√	Undefined
03FEC280H	CAN0 message data byte 0 register 12	C0MDATA012			√		Undefined
03FEC281H	CAN0 message data byte 1 register 12	C0MDATA112			√		Undefined
03FEC282H	CAN0 message data byte 23 register 12	C0MDATA2312				√	Undefined
03FEC282H	CAN0 message data byte 2 register 12	C0MDATA212			√		Undefined
03FEC283H	CAN0 message data byte 3 register 12	C0MDATA312			√		Undefined
03FEC284H	CAN0 message data byte 45 register 12	C0MDATA4512				√	Undefined
03FEC284H	CAN0 message data byte 4 register 12	C0MDATA412			√		Undefined
03FEC285H	CAN0 message data byte 5 register 12	C0MDATA512			√		Undefined
03FEC286H	CAN0 message data byte 67 register 12	C0MDATA6712				√	Undefined
03FEC286H	CAN0 message data byte 6 register 12	C0MDATA612			√		Undefined
03FEC287H	CAN0 message data byte 7 register 12	C0MDATA712			√		Undefined
03FEC288H	CAN0 message data length register 12	C0MDLC12			√		0000xxxxB
03FEC289H	CAN0 message configuration register 12	C0MCONF12			√		Undefined
03FEC28AH	CAN0 message identifier register 12	C0MIDL12				√	Undefined
03FEC28CH		C0MIDH12				√	Undefined
03FEC28EH	CAN0 message control register 12	C0MCTRL12				√	00x00000 000xx000B
03FEC2A0H	CAN0 message data byte 01 register 13	C0MDATA0113				√	Undefined
03FEC2A0H	CAN0 message data byte 0 register 13	C0MDATA013			√		Undefined
03FEC2A1H	CAN0 message data byte 1 register 13	C0MDATA113			√		Undefined
03FEC2A2H	CAN0 message data byte 23 register 13	C0MDATA2313				√	Undefined
03FEC2A2H	CAN0 message data byte 2 register 13	C0MDATA213			√		Undefined
03FEC2A3H	CAN0 message data byte 3 register 13	C0MDATA313			√		Undefined
03FEC2A4H	CAN0 message data byte 45 register 13	C0MDATA4513				√	Undefined
03FEC2A4H	CAN0 message data byte 4 register 13	C0MDATA413			√		Undefined
03FEC2A5H	CAN0 message data byte 5 register 13	C0MDATA513			√		Undefined
03FEC2A6H	CAN0 message data byte 67 register 13	C0MDATA6713				√	Undefined
03FEC2A6H	CAN0 message data byte 6 register 13	C0MDATA613			√		Undefined
03FEC2A7H	CAN0 message data byte 7 register 13	C0MDATA713			√		Undefined
03FEC2A8H	CAN0 message data length register 13	C0MDLC13			√		0000xxxxB
03FEC2A9H	CAN0 message configuration register 13	C0MCONF13			√		Undefined
03FEC2AAH	CAN0 message identifier register 13	C0MIDL13				√	Undefined
03FEC2ACH		C0MIDH13				√	Undefined
03FEC2AEH	CAN0 message control register 13	C0MCTRL13				√	00x00000 000xx000B

(4) UF0 EPNAK mask register (UF0ENM)

This register controls masking a write access to the UF0EN register.

This register can be read or written in 8-bit units.

Be sure to clear bits 7 to 4, 1, and 0 to “0”. If it is set to 1, the operation is not guaranteed.

	7	6	5	4	3	2	1	0	Address	After reset
UF0ENM	0	0	0	0	BKO2NKM	BKO1NKM	0	0	00200006H	00H

Bit position	Bit name	Function
3	BKO2NKM	This bit specifies whether a write access to bit 3 (BKO2NK) of the UF0EN register is masked or not. 1: Do not mask. 0: Mask (default value).
2	BKO1NKM	This bit specifies whether a write access to bit 2 (BKO1NK) of the UF0EN register is masked or not. 1: Do not mask. 0: Mask (default value).

(23) UF0 INT clear 2 register (UF0IC2)

This register controls clearing the interrupt sources indicated by the UF0IS2 register.

This register is write-only, in 8-bit units. If this register is read, the value FFH is read.

FW can clear an interrupt source by writing 0 to the corresponding bit of this register. Even a bit that is automatically cleared to 0 by hardware can be cleared by FW before it is cleared by hardware. Writing 0 to a bit of this register automatically sets the bit to 1. Writing 1 is invalid.

The related bits are invalid if each endpoint is not supported by the setting of the UF0EnIM register (n = 1, 3, 7) and the current setting of the interface.

	7	6	5	4	3	2	1	0	Address	After reset
UF0IC2	BKI2INC	BKI2 DTC	BKI1INC	BKI1 DTC	1	1	1	IT1DTC	00200040H	FFH

Bit position	Bit name	Function
7, 5	BKInINC	These bits clear the BLKInIN interrupt. 0: Clear
6, 4	BKInDTC	These bits clear the BLKInDT interrupt. 0: Clear
0	IT1DTC	These bits clear the INTnDT interrupt. 0: Clear

Remark n = 1, 2

(34) UF0 mode status register (UF0MODS)

This register indicates the configuration status.

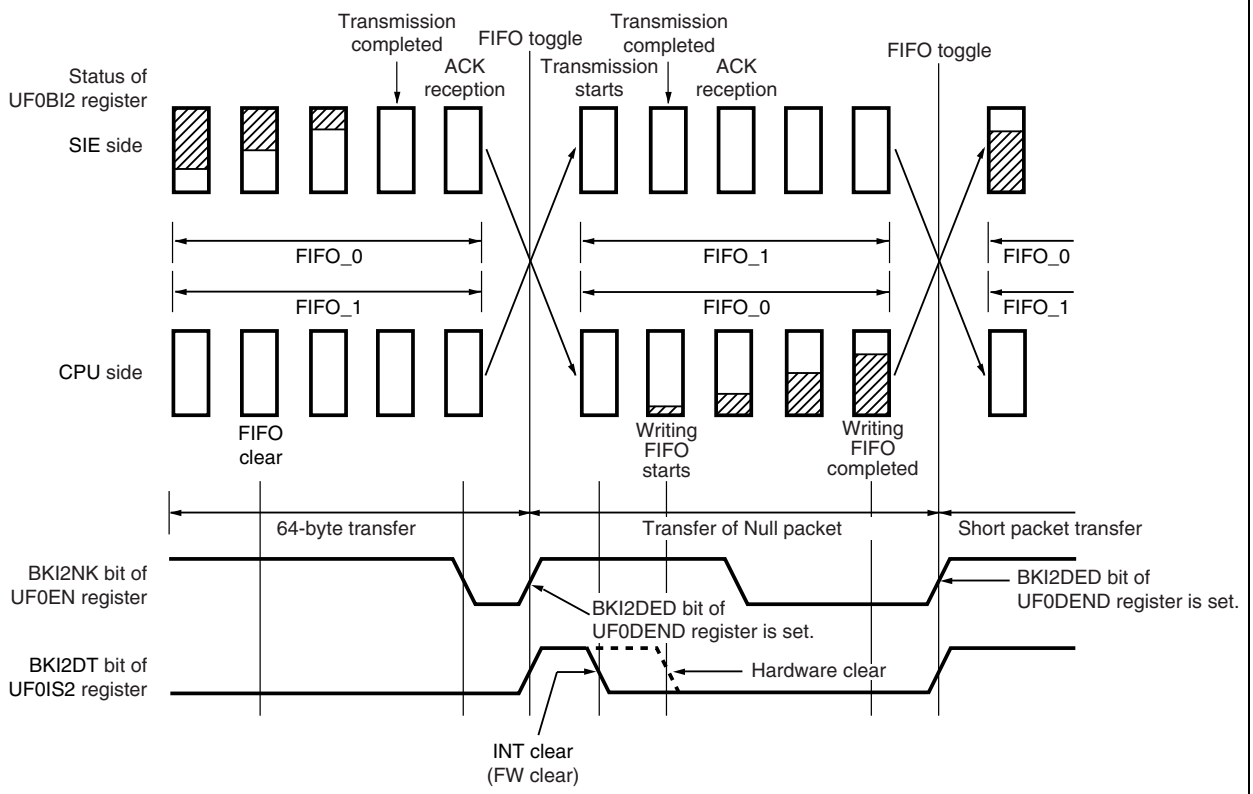
This register is read-only, in 8-bit units.

	7	6	5	4	3	2	1	0	Address	After reset
UF0MODS	0	CDCGD	0	MPACK	DFLT	CONF	0	0	00200078H	00H

Bit position	Bit name	Function
6	CDCGD	This bit specifies whether CPUDEC processing is performed for the GET_DESCRIPTOR Configuration request. 1: Forcibly change the GET_DESCRIPTOR Configuration request to CPUDEC processing. 0: Automatically process the GET_DESCRIPTOR Configuration request (default value).
4	MPACK	This bit indicates the transmit packet size of Endpoint0. 1: Transmit a packet of other than 8 bytes. 0: Transmit a packet of 8 bytes (default value). This bit is automatically set to 1 by hardware after the GET_DESCRIPTOR Device request has been processed (on normal completion of the status stage). It is not cleared to 0 until the USBF has been reset (it is not cleared to 0 by Bus Reset). If this bit is not set to 1, the hardware transfers only the automatically-executed request in 8-byte units. Therefore, even if data of more than 8 bytes is sent by the OUT token to be processed by FW before completion of the GET_DESCRIPTOR Device request, the data is correctly received. This bit is ignored if the size of Endpoint0 is 8 bytes.
3	DFLT	This bit indicates the default status (DFLT bit = 1). 1: Enables response. 0: Disables response (always no response) (default value). This bit is automatically set to 1 by Bus Reset. The transaction for all the endpoints is not responded to until this bit is set to 1.
2	CONF	This bit indicates whether the SET_CONFIGURATION request has been completed. 1: SET_CONFIGURATION request has been completed. 0: SET_CONFIGURATION request has not been completed (default value). This bit is set to 1 when Configuration value = 1 is received by the SET_CONFIGURATION request. Unless this bit is set to 1, access to an endpoint other than Endpoint0 is ignored. This bit is cleared to 0 when Configuration value = 0 is received by the SET_CONFIGURATION request. It is also cleared to 0 when Bus Reset is detected.

Figure 20-10. Operation of UF0BI2 Register (3/3)

(c) Operation example 3



(14) UF0 configuration/interface/endpoint descriptor registers 0 to 255 (UF0CIE0 to UF0CIE255)

These registers store the value to be returned in response to the GET_DESCRIPTOR Configuration request.

These registers can be read or written in 8-bit units. However, data can be written to these registers only when the EP0NKA bit is set to 1.

Descriptor information of up to 256 bytes can be stored in these registers. Store each descriptor in the order of Configuration, Interface, and Endpoint (see **Table 20-6**). If there are two or more Interfaces, repeatedly store the data following the Interface descriptor.

Table 20-6. Mapping of UF0CIEn Register

Address	Descriptor Stored
002001C6H	Configuration descriptor (9 bytes)
002001D8H	Interface descriptor (9 bytes)
002001EAH	Endpoint1 descriptor (7 bytes)
002001F8H	Endpoint2 descriptor (7 bytes)
00200206H	Endpoint3 descriptor (7 bytes)
:	:
002002xxH	Interface descriptor (9 bytes)
002002xxH+9	Endpoint1 descriptor (7 bytes)
002002xxH+16	Endpoint2 descriptor (7 bytes)
002002xxH+23	Endpoint3 descriptor (7 bytes)
:	:

The range of the valid data that can be set to these registers varies according to the setting of the UF0DSCL register. In addition to the descriptors listed in Table 20-7, descriptors peculiar to classes and vendors can also be stored.

If all the values are fixed, they can be stored in ROM.

Cautions 1. To rewrite these registers, set the EP0NKA bit to 1 before reading the register contents, and rewrite the register contents after confirming that the bit has been set, in order to prevent conflict between a read access and a write access.

2. Use the value defined by USB Specification Ver. 2.0 and the latest Class Specification as the set value.

	7	6	5	4	3	2	1	0	Address	After reset
UF0CIEn (n = 0 to 255)									002001C6H to 002003C4H	Undefined

Table 21-1. DMA Start Factors (1/2)

IFCn5	IFCn4	IFCn3	IFCn2	IFCn1	IFCn0	Interrupt Source
0	0	0	0	0	0	DMA request by interrupt disabled
0	0	0	0	0	1	INTP02
0	0	0	0	1	0	INTP05
0	0	0	0	1	1	INTP09
0	0	0	1	0	0	INTP10
0	0	0	1	1	0	INTP16
0	0	1	1	0	0	INTTAB1OV_BASE[Note]
0	0	1	1	0	1	INTTAB1CC0
0	0	1	1	1	0	INTTAB1CC1
0	0	1	1	1	1	INTTAB1CC2
0	1	0	0	0	0	INTTAB1CC3
0	1	0	0	0	1	INTTT0OV
0	1	0	0	1	0	INTTT0CC0
0	1	0	0	1	1	INTTT0CC1
0	1	0	1	0	0	INTTAA0OV
0	1	0	1	0	1	INTTAA0CC0
0	1	0	1	1	0	INTTAA0CC1
0	1	0	1	1	1	INTTAA1OV
0	1	1	0	0	0	INTTAA1CC0
0	1	1	0	0	1	INTTAA1CC1
0	1	1	0	1	0	INTTAA2CC0
0	1	1	0	1	1	INTTAA2CC1
0	1	1	1	1	0	INTTAA4CC0
0	1	1	1	1	1	INTTAA4CC1
1	0	0	0	1	0	INTTM0EQ0
1	0	0	0	1	1	INTTM1EQ0
1	0	0	1	0	0	INTTM2EQ0
1	0	0	1	0	1	INTTM3EQ0
1	0	0	1	1	0	INTCF0R/INTIIC1
1	0	0	1	1	1	INTCF0T

Note INTTAB1OV_BASE is the interrupt signal from before the overflow interrupt of TAB1 (INTTAB1OV) was culled by TMQOP.

21.9 DMA Transfer Start Factors

There are two types of DMA transfer start factors, as shown below.

(1) Request by software

If the STGn bit is set to 1 while the DCHCn.TCn bit = 1 and Enn bit = 1 (DMA transfer enabled), DMA transfer is started.

To request the next DMA transfer cycle immediately after that, confirm, by using the DBCn register, that the preceding DMA transfer cycle has been completed, and set the STGn bit to 1 again (n = 0 to 3).

TCn bit = 0, Enn bit = 1
↓
STGn bit = 1 … Starts the first DMA transfer.
↓
Confirm that the contents of the DBCn register have been updated.
STGn bit = 1 … Starts the second DMA transfer.
↓
:
↓
Generation of terminal count … Enn bit = 0, TCn bit = 1, and INTDMAn signal is generated.

(2) Request by on-chip peripheral I/O

If an interrupt request is generated from the on-chip peripheral I/O set by the DTFRn register when the DCHCn.TCn bit = 0 and Enn bit = 1 (DMA transfer enabled), DMA transfer is started.

Cautions 1. Two start factors (software trigger and hardware trigger) cannot be used for one DMA channel. If two start factors are simultaneously generated for one DMA channel, only one of them is valid. The start factor that is valid cannot be identified.

2. A new transfer request that is generated after the preceding DMA transfer request was generated or in the preceding DMA transfer cycle is ignored (cleared).

3. The transfer request interval of the same DMA channel varies depending on the setting of bus wait in the DMA transfer cycle, the start status of the other channels, or the external bus hold request. In particular, as described in Caution 2, a new transfer request that is generated for the same channel before the DMA transfer cycle or during the DMA transfer cycle is ignored. Therefore, the transfer request intervals for the same DMA channel must be sufficiently separated by the system. When the software trigger is used, completion of the DMA transfer cycle that was generated before can be checked by updating the DBCn register.

22.4.3 EP flag

The EP flag is a status flag used to indicate that exception processing is in progress. It is set when an exception occurs.

After reset: 00000020H

	31	8	7	6	5	4	3	2	1	0
PSW	0		NP	**EP**	ID	SAT	CY	OV	S	Z

EP	Exception processing status
0	Exception processing not in progress.
1	Exception processing in progress.

(2) External interrupt falling, rising edge specification register 3 (INTF3, INTR3)

The INTF3 and INTR3 registers are 8-bit registers that specify detection of the falling and rising edges of the external interrupt pin (INTP07 to INTP09).

These registers can be read or written in 8-bit or 1-bit units.

Reset sets these registers to 00H.

Caution When the function is changed from the external interrupt function (alternate function) to the port function, an edge may be detected. Therefore, set the INTF3n and INTR3n bits to 00, and then set the port mode.

After reset: 00H R/W Address: INTF3 FFFFFC06H, INTR3 FFFFFC26H

	7	6	5	4	3	2	1	0
INTF3	0	0	0	INTF34	0	0	INTF31	INTF30
				INTP09			INTP08	INTP07
INTR3	0	0	0	INTR34	0	0	INTR31	INTR30
				INTP09			INTP08	INTP07

Remark For how to specify a valid edge, see **Table 22-7**.

Table 22-5. Valid Edge Specification

INTF3n	INTR3n	Valid Edge Specification
0	0	No edge detected
0	1	Rising edge
1	0	Falling edge
1	1	Both rising and falling edges

Caution Be sure to set the INTF3n and INTR3n bits to 00 when these registers are not used as the INTP07 to INTP09 pin.

Remark n = 0, 1, 4: Control of INTP07 to INTP09 pins

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Symbol	Name	Unit	Page
PM7H	Port 7 mode register H	Port	134
PM7L	Port 7 mode register L	Port	134
PM9	Port 9 mode register	Port	137
PM9H	Port 9 mode register H	Port	137
PM9L	Port 9 mode register L	Port	137
PMC0	Port 0 mode control register	Port	110
PMC3	Port 3 mode control register	Port	116
PMC4	Port 4 mode control register	Port	122
PMC5	Port 5 mode control register	Port	126
PMC6	Port 6 mode control register	Port	131
PMC9	Port 9 mode control register	Port	137
PMC9H	Port 9 mode control register H	Port	137
PMC9L	Port 9 mode control register L	Port	137
PMDL	Port DL mode register	Port	143
PMDLH	Port DL mode register H	Port	143
PMDLL	Port DL mode register L	Port	143
PRCMD	Command register	CPU	93
PRSCM0	Prescaler compare register 0	BRG	606
PRSCM1	Prescaler compare register 1	BRG	763
PRSCM2	Prescaler compare register 2	BRG	763
PRSCM3	Prescaler compare register 3	BRG	763
PRSM0	Prescaler mode register 0	BRG	605
PRSM1	Prescaler mode register 1	BRG	762
PRSM2	Prescaler mode register 2	BRG	762
PRSM3	Prescaler mode register 3	BRG	762
PSC	Power save control register	CG	1249
PSMR	Power save mode register	CG	1250
PSW	Program status word	CPU	62
r0-r31	General-purpose registers	CPU	58
RAMS	Internal RAM data status register	LVI	1285
RC1ALH	Alarm hour setting register	RTC	603
RC1ALM	Alarm minute setting register	RTC	603
RC1ALW	Alarm day-of week setting register	RTC	604
RC1CC0	Real-time counter control register 0	RTC	592
RC1CC1	Real-time counter control register 1	RTC	592
RC1CC2	Real-time counter control register 2	RTC	594
RC1CC3	Real-time counter control register 3	RTC	595
RC1DAY	Day count register	RTC	599
RC1HOUR	Hour count register	RTC	597
RC1MIN	Minute count register	RTC	597
RC1MONTH	Month count register	RTC	601
RC1SEC	Second count register	RTC	596
RC1SUBC	Sub-count register	RTC	596
RC1SUBU	Watch error correction register	RTC	602