Renesas Electronics America Inc - UPD70F3824GB-GAH-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, CSI, EBI/EMI, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	45
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 10x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3824gb-gah-ax

2.3 Pin I/O Circuit Types, I/O Buffer Power Supplies and Connection of Unused Pins

Table 2-3. Pin I/O Circuit Types, I/O Buffer Power Supplies and Connection of Unused Pins (1/3)

Pin Name	Alternate Function	I/O Circuit Type	Recommended Connection	Pin No.		
				JC3-H		JE3-H
				40 pin	48 pin	
P02	NMI	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	–	–	√
P03	INTP02/ADTRG/UCLK	10-D		√	√	√
P10	ANO0	12-D	Input: Independently connect to AV_{REF1} or AV_{SS} via a resistor. Output: Leave open.	–	√	√
P30	TXDC0/SOF4/INTP07	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	√	√	√
P31	RXDC0/SIF4/INTP08			√	√	√
P32	ASCKC0/$\overline{\text{SCKF4}}$/TIAA00/TOAA00			√	√	√
P33	TIAA01/TOAA01/RTCDIV/RTCCL			–	–	√
P34	TIAA10/TOAA10/TOAA1OFF/INTP09			–	–	√
	TIAA10/TOAA10/ INTP09			√	√	–
P35	TIAA11/TOAA11/RTC1HZ			–	–	√
P36	TXDC3/SCL00/CTXD0[Note]			–	√	√
P37	RXDC3/SDA00/CRXD0[Note]			–	√	√
P40	SIF0/TXDC4/SDA01	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	√	√	√
P41	SOF0/RXDC4/SCL01			√	√	√
P42	$\overline{\text{SCKF0}}$/INTP10			√	√	√
P52	KR2/RTP02/DDI	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	√	√	√
P53	SIF2/KR3/RTP03/DDO			√	√	√
P54	SOF2/KR4/RTP04/DCK			√	√	√
P55	$\overline{\text{SCKF2}}$/KR5/RTP05/DMS			√	√	√
P56	INTP05/$\overline{\text{DRST}}$			√	√	√
P60	TOAB1T1/TIAB11/TOAB11	5	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	–	–	√
P61	TOAB1B1/TIAB10/TOAB10			–	–	√
P62	TOAB1T2/TIAB12/TOAB12			–	–	√
P63	TOAB1B2/TRGAB1			–	–	√
P64	TOAB1T3/TIAB13/TOAB13			–	–	√
P70 to P74	ANI0 to ANI4	11-G	Input: Independently connect to AV_{REF1} or AV_{SS} via a resistor. Output: Leave open.	√	√	√
P75	ANI5			–	√	√
P76 to P79	ANI6 to ANI9			–	–	√

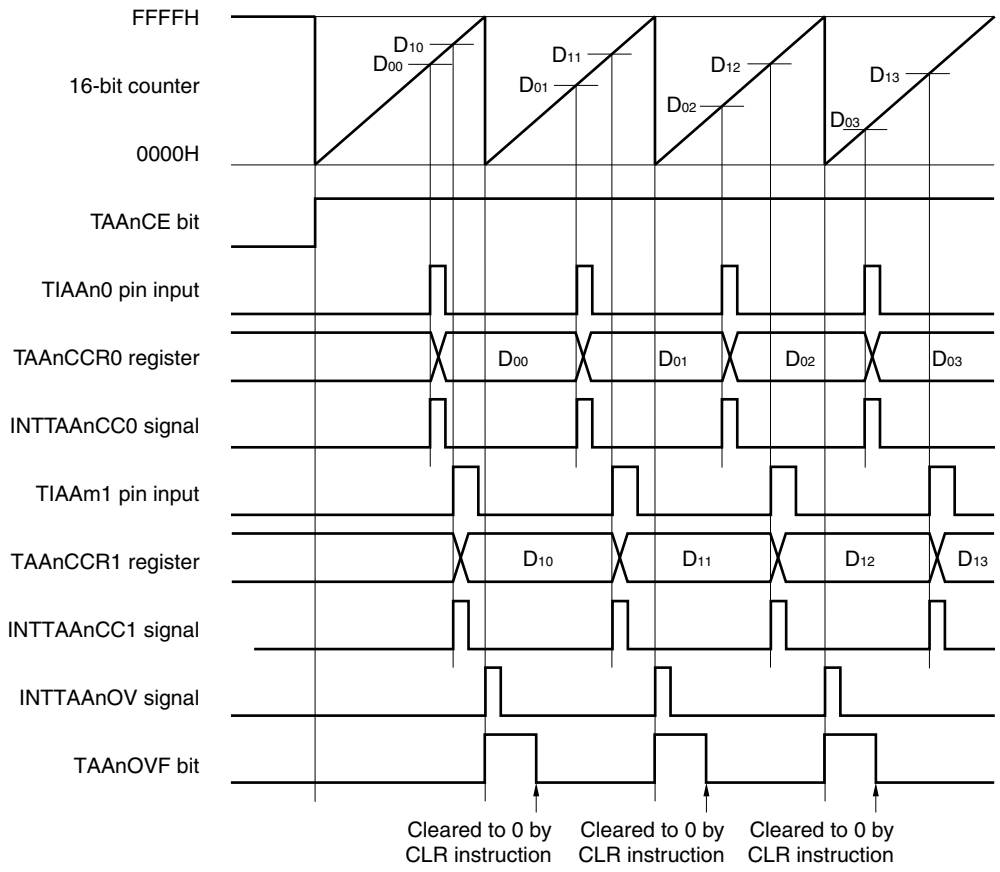
Note μPD70F3819, 70F3825 only

Remark JC3-H: V850ES/JC3-H, JE3-H: V850ES/JE3-H

When the TAAnCE bit is set to 1, the 16-bit counter starts counting. When the valid edge input to the TIAAnm pin is detected, the count value of the 16-bit counter is stored in the TAAnCCRm register, and a capture interrupt request signal (INTTAAnCCm) is generated.

The 16-bit counter continues counting in synchronization with the count clock. When it counts up to FFFFH, it generates an overflow interrupt request signal (INTTAAnOV) at the next clock, is cleared to 0000H, and continues counting. At this time, the overflow flag (TAAnOPT0.TAAnOVF bit) is also set to 1. Clear the overflow flag to 0 by executing the CLR instruction by software.

Figure 6-35. Basic Timing in Free-Running Timer Mode (Capture Function)



Remark n = 0 to 2
m = 2 (V850ES/JC3-H)
m = 0 to 2 (V850ES/JE3-H)

Figure 6-51. Operation Flow in Cascade Connection of TAA1 and TAA0 (2/2)

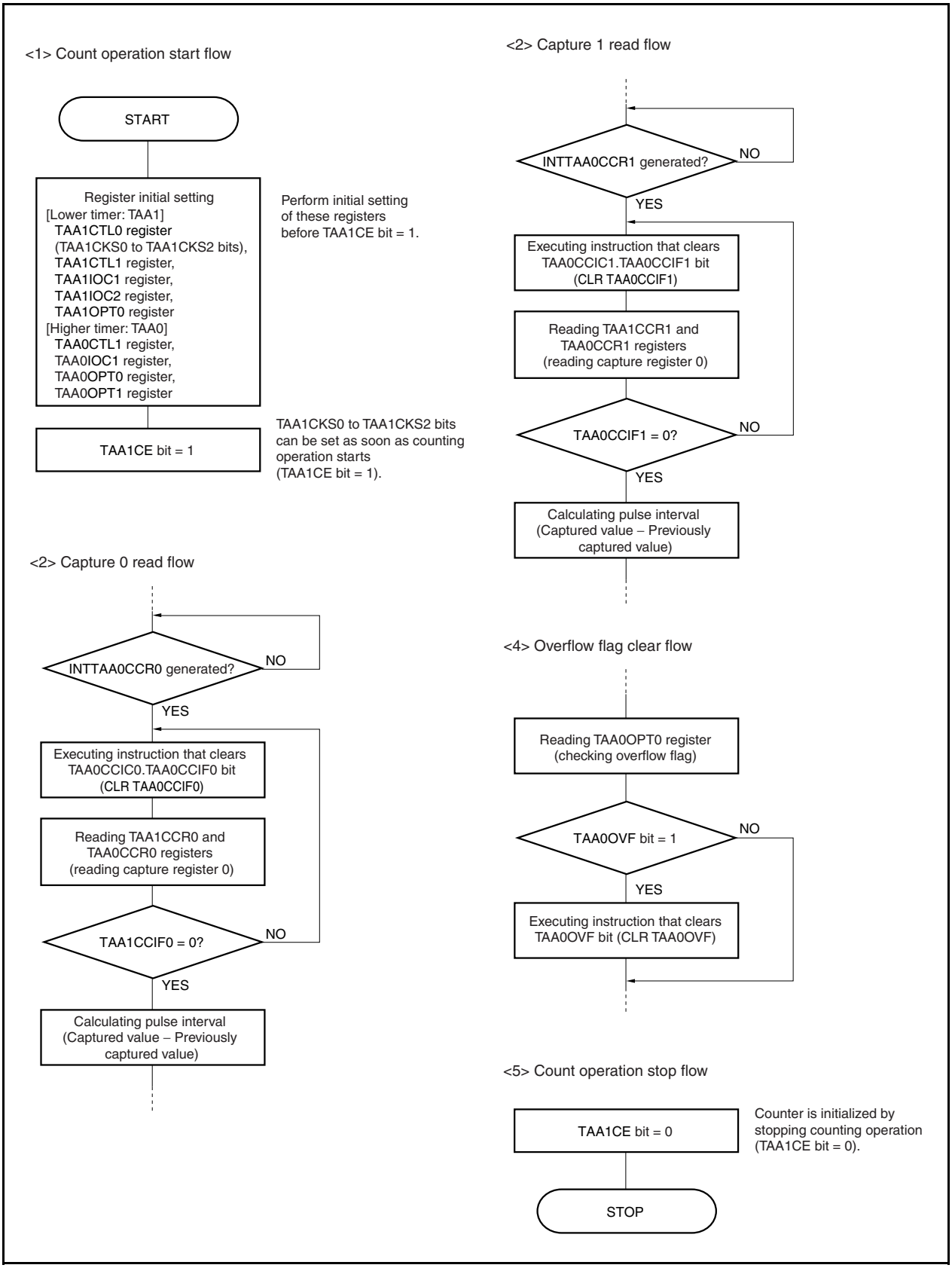
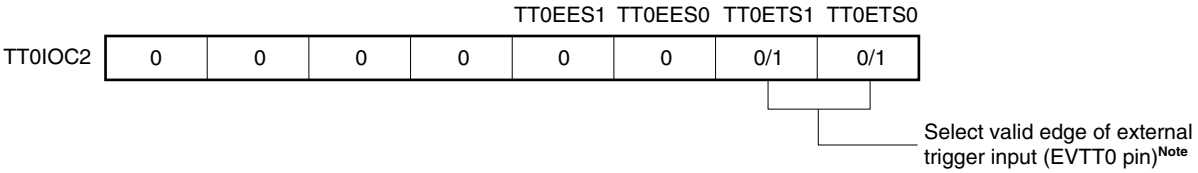


Figure 8-27. Setting of Registers in One-Shot Pulse Output Mode (2/2)

(d) TMT0 I/O control register 2 (TT0IOC2)



Note Set the valid edge selection of the unused alternate external input signals to “No edge detection”.

(e) TMT0 counter read buffer register (TT0CNT)

The value of the 16-bit counter can be read by reading the TT0CNT register.

(f) TMT0 capture/compare registers 0 and 1 (TT0CCR0 and TT0CCR1)

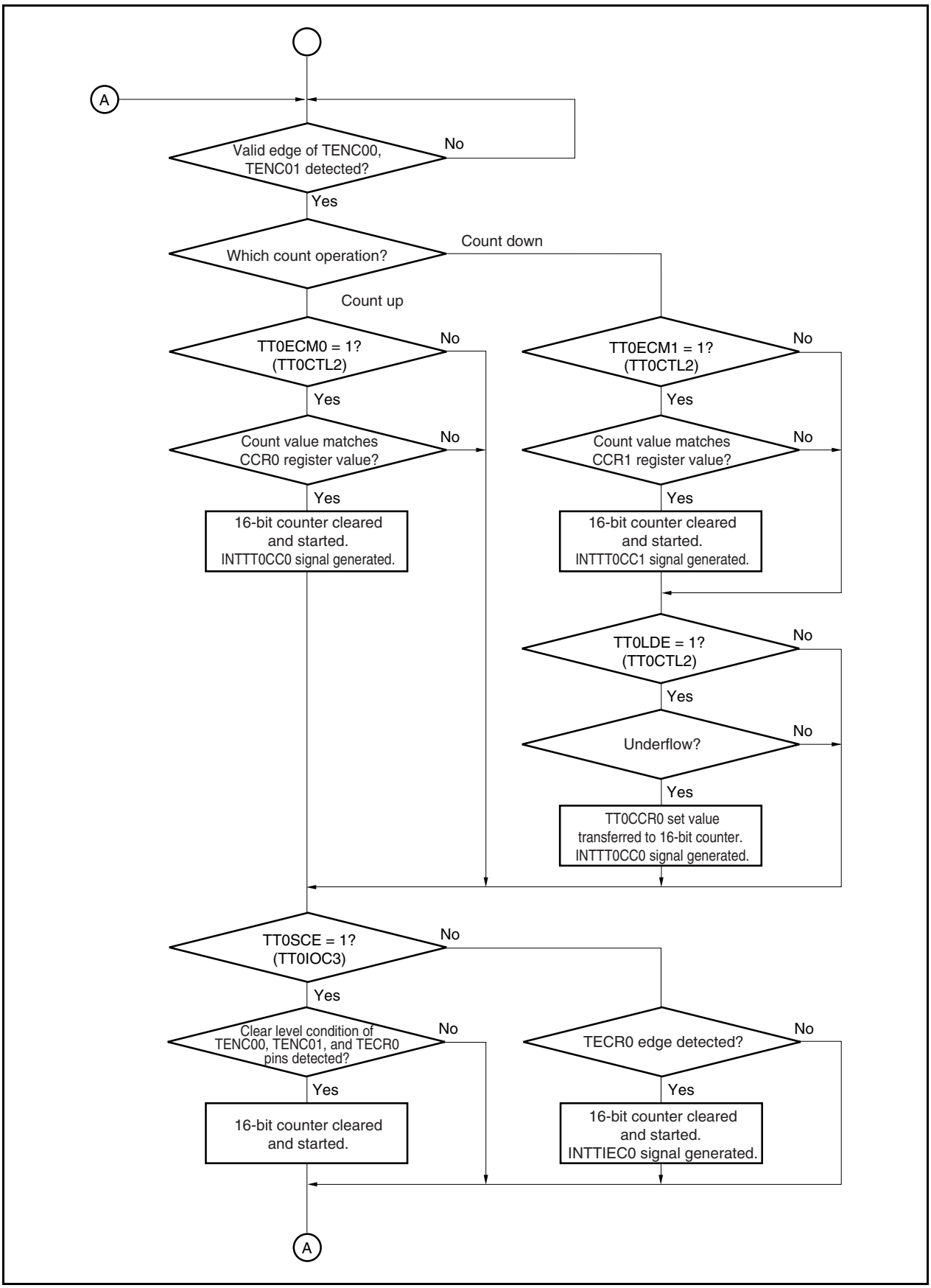
If D_0 is set to the TT0CCR0 register and D_1 to the TT0CCR1 register, the active level width and output delay period of the one-shot pulse are as follows.

Active level width = $(D_0 - D_1 + 1) \times$ Count clock cycle

Output delay period = $D_1 \times$ Count clock cycle

Remark TMT0 control register 2 (TT0CTL2), TMT0 I/O control register 1 (TT0IOC1), TMT0 I/O control register 3 (TT0IOC3), TMT0 option register 0 (TT0OPT0), TMT0 option register 1 (TT0OPT1), and TMT0 counter write register (TT0TCW) are not used in the one-shot pulse output mode.

Figure 8-56. Encoder Compare Mode Operation Processing



CHAPTER 16 ASYNCHRONOUS SERIAL INTERFACE C (UARTC)

The V850ES/JC3-H (40 pin) have a 3 channels UARTC.
The V850ES/JC3-H (48 pin) and V850ES/JE3-H have a 4channels UARTC.

16.1 Features

- Transfer rate: 300 bps to 3 Mbps (using internal system clock of 24 MHz and dedicated baud rate generator)
- Full-duplex communication: Internal UARTCn receive data register (UCnRX)
  Internal UARTCn transmit data register (UCnTX)
- 2-pin configuration: TXDCn: Transmit data output pin
  RXDCn: Receive data input pin
- Reception error detection function
  - Parity error
  - Framing error
  - Overrun error
  - LIN communication data consistency error detect function
  - SBF reception success detect function
- Interrupt sources: 2 types
  - Reception completion interrupt (INTUCnR): This interrupt occurs upon transfer of receive data from the receive shift register to the receive data register after serial transfer is complete, in the reception enabled status.
  - Transmission enable interrupt (INTUCnT): This interrupt occurs upon transfer of transmit data from the transmit data register to the transmit shift register in the transmission enabled status.
- Character length: 7 to 9 bits
- Parity function: Odd, even, 0, none
- Transmission stop bit: 1, 2 bits
- On-chip dedicated baud rate generator
- MSB-/LSB-first transfer selectable
- Transmit/receive data inverted input/output possible
- SBF (Sync Break Field) transmission in the LIN (Local Interconnect Network) communication format
  - 13 to 20 bits selectable for the SBF transmission
  - Recognition of 11 bits or more possible for SBF reception
  - SBF reception flag provided

Remark n = 0, 2, 4 (V850ES/JC3-H (40 pin))
n = 0, 2 to 4 (V850ES/JC3-H (48 pin), V850ES/JE3-H)

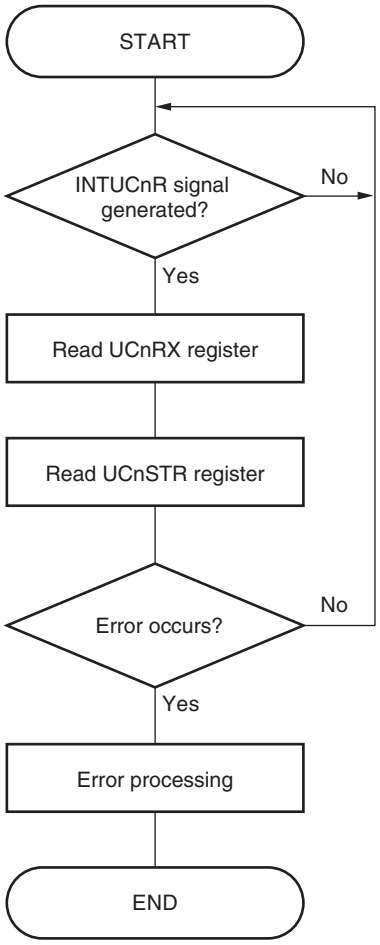
16.6.8 Reception errors

Errors during a receive operation are of three types: parity errors, framing errors, and overrun errors. Data reception result error flags are set in the UCnSTR register and a reception completion interrupt request signal (INTUCnR) is output when an error occurs.

It is possible to ascertain which error occurred during reception by reading the contents of the UCnSTR register.

Clear the reception error flag by writing 0 to it after reading it.

Figure 16-15. Receive Data Read Flow



Caution When an INTUCnR signal is generated, the UCnSTR register must be read to check for errors.

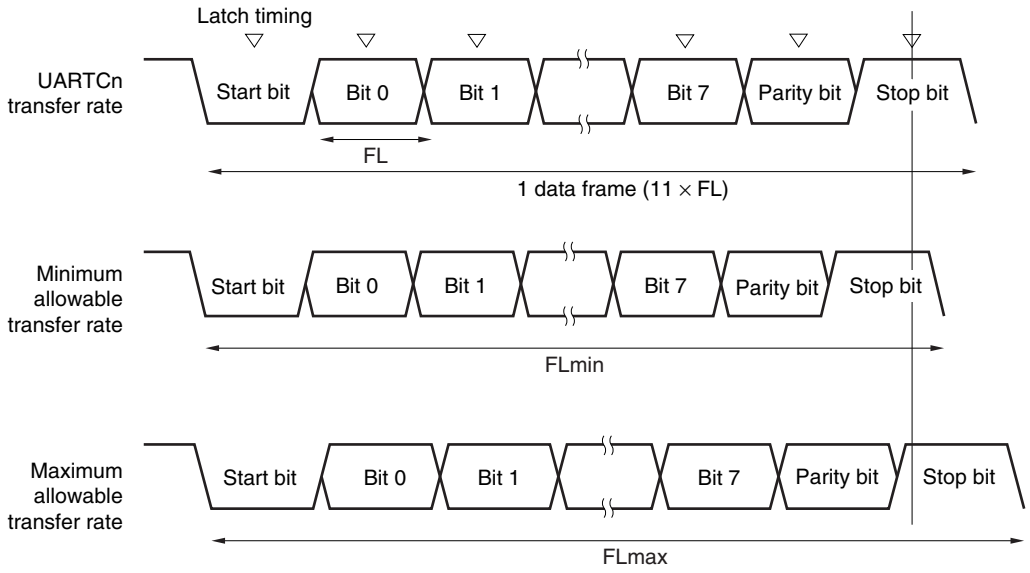
Remark fxx: Main clock frequency
ERR: Baud rate error (%)

(5) Allowable baud rate range during reception

The baud rate error range at the destination that is allowable during reception is shown below.

Caution The baud rate error during reception must be set within the allowable error range using the following equation.

Figure 16-19. Allowable Baud Rate Range During Reception



Remark n = 0, 2 to 4 (V850ES/JC3-H (48 pin) (Except the μPD70F3819),
V850ES/JE3-H (64 pin) (Except the μPD70F3825))
n = 0, 2, 4 (V850ES/JC3-H (40 pin))

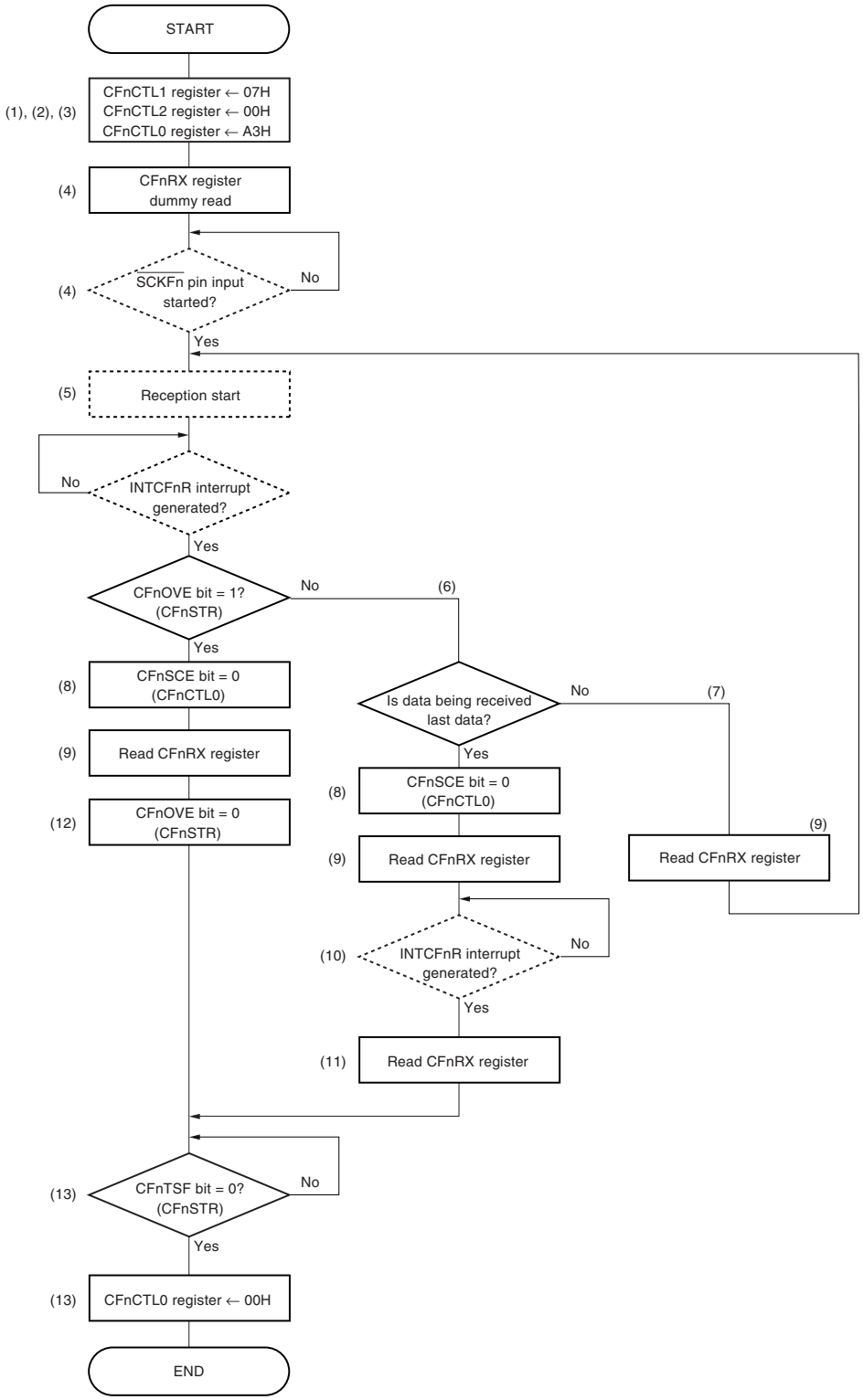
As shown in Figure 16-20, the receive data latch timing is determined by the counter set using the UCnCTL2 register following start bit detection. The transmit data can be normally received if up to the last data (stop bit) can be received in time for this latch timing.
When this is applied to 11-bit reception, the following is the theoretical result.

$FL = (Brate)^{-1}$

Brate: UARTCn baud rate (n = 0 to 2, 4)
k: Set value of UCnCTL2.UCnBRS7 to UCnCTL2.UCnBRS0 bits (n = 0 to 2, 4)
FL: 1-bit data length
Latch timing margin: 2 clocks

Minimum allowable transfer rate: $FLmin = 11 \times FL - \frac{k-2}{2k} \times FL = \frac{21k+2}{2k} FL$

(1) Operation flow

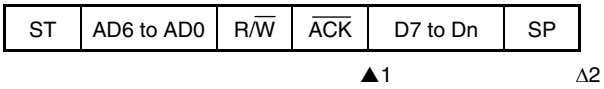


Remarks 1. The broken lines indicate the hardware processing.

2. The numbers in this figure correspond to the processing numbers in **(2) Operation timing**.

3. n = 0, 2 to 4

(5) When arbitration loss occurs due to stop condition during data transfer



▲1 Δ2

▲1: IICSn register = 1000X110B

Δ 2: IICSn register = 01000001B

Remarks 1. ▲: Always generated

Δ: Generated only when SPIEn bit = 1

X: don't care

2. Dn = D6 to D0

Table 19-16. Register Access Types (17/17)

Address	Register Name	Symbol	R/W	Bit Manipulation Units			After Reset
				1 Bit	8 Bits	16 Bits	
03FEC4C0H	CAN0 message data byte 01 register 30	C0MDATA0130	R/W			√	Undefined
03FEC4C0H	CAN0 message data byte 0 register 30	C0MDATA030			√		Undefined
03FEC4C1H	CAN0 message data byte 1 register 30	C0MDATA130			√		Undefined
03FEC4C2H	CAN0 message data byte 23 register 30	C0MDATA2330				√	Undefined
03FEC4C2H	CAN0 message data byte 2 register 30	C0MDATA230			√		Undefined
03FEC4C3H	CAN0 message data byte 3 register 30	C0MDATA330			√		Undefined
03FEC4C4H	CAN0 message data byte 45 register 30	C0MDATA4530				√	Undefined
03FEC4C4H	CAN0 message data byte 4 register 30	C0MDATA430			√		Undefined
03FEC4C5H	CAN0 message data byte 5 register 30	C0MDATA530			√		Undefined
03FEC4C6H	CAN0 message data byte 67 register 30	C0MDATA6730				√	Undefined
03FEC4C6H	CAN0 message data byte 6 register 30	C0MDATA630			√		Undefined
03FEC4C7H	CAN0 message data byte 7 register 30	C0MDATA730			√		Undefined
03FEC4C8H	CAN0 message data length register 30	C0MDLC30			√		0000xxxxB
03FEC4C9H	CAN0 message configuration register 30	C0MCONF30			√		Undefined
03FEC4CAH	CAN0 message identifier register 30	C0MIDL30				√	Undefined
03FEC4CCH		C0MIDH30				√	Undefined
03FEC4CEH	CAN0 message control register 30	C0MCTRL30				√	00x00000 000xx000B
03FEC4E0H	CAN0 message data byte 01 register 31	C0MDATA0131				√	Undefined
03FEC4E0H	CAN0 message data byte 0 register 31	C0MDATA031			√		Undefined
03FEC4E1H	CAN0 message data byte 1 register 31	C0MDATA131			√		Undefined
03FEC4E2H	CAN0 message data byte 23 register 31	C0MDATA2331				√	Undefined
03FEC4E2H	CAN0 message data byte 2 register 31	C0MDATA231			√		Undefined
03FEC4E3H	CAN0 message data byte 3 register 31	C0MDATA331			√		Undefined
03FEC4E4H	CAN0 message data byte 45 register 31	C0MDATA4531				√	Undefined
03FEC4E4H	CAN0 message data byte 4 register 31	C0MDATA431			√		Undefined
03FEC4E5H	CAN0 message data byte 5 register 31	C0MDATA531			√		Undefined
03FEC4E6H	CAN0 message data byte 67 register 31	C0MDATA6731				√	Undefined
03FEC4E6H	CAN0 message data byte 6 register 31	C0MDATA631			√		Undefined
03FEC4E7H	CAN0 message data byte 7 register 31	C0MDATA731			√		Undefined
03FEC4E8H	CAN0 message data length register 31	C0MDLC31			√		0000xxxxB
03FEC4E9H	CAN0 message configuration register 31	C0MCONF31			√		Undefined
03FEC4EAH	CAN0 message identifier register 31	C0MIDL31				√	Undefined
03FEC4ECH		C0MIDH31				√	Undefined
03FEC4EEH	CAN0 message control register 31	C0MCTRL31				√	00x00000 000xx000B

(7) CAN0 module last error information register (C0LEC)

The C0LEC register provides the error information of the CAN protocol.

After reset: 00H R/W Address: 03FEC052H

	7	6	5	4	3	2	1	0
C0LEC	0	0	0	0	0	LEC2	LEC1	LEC0

LEC2	LEC1	LEC0	Last CAN protocol error information
0	0	0	No error
0	0	1	Stuff error
0	1	0	Form error
0	1	1	ACK error
1	0	0	Bit error. (The CAN module tried to transmit a recessive-level bit as part of a transmit message (except the arbitration field), but the value on the CAN bus is a dominant-level bit.)
1	0	1	Bit error. (The CAN module tried to transmit a dominant-level bit as part of a transmit message, ACK bit, error frame, or overload frame, but the value on the CAN bus is a recessive-level bit.)
1	1	0	CRC error
1	1	1	Undefined

Caution Be sure to set bits 3 to 7 to “0”.

Remarks 1. The contents of the C0LEC register are not cleared when the CAN module changes from an operation mode to the initialization mode.

2. If an attempt is made to write a value other than 00H to the C0LEC register by software, the access is ignored.

Figure 19-32. Transmit History List

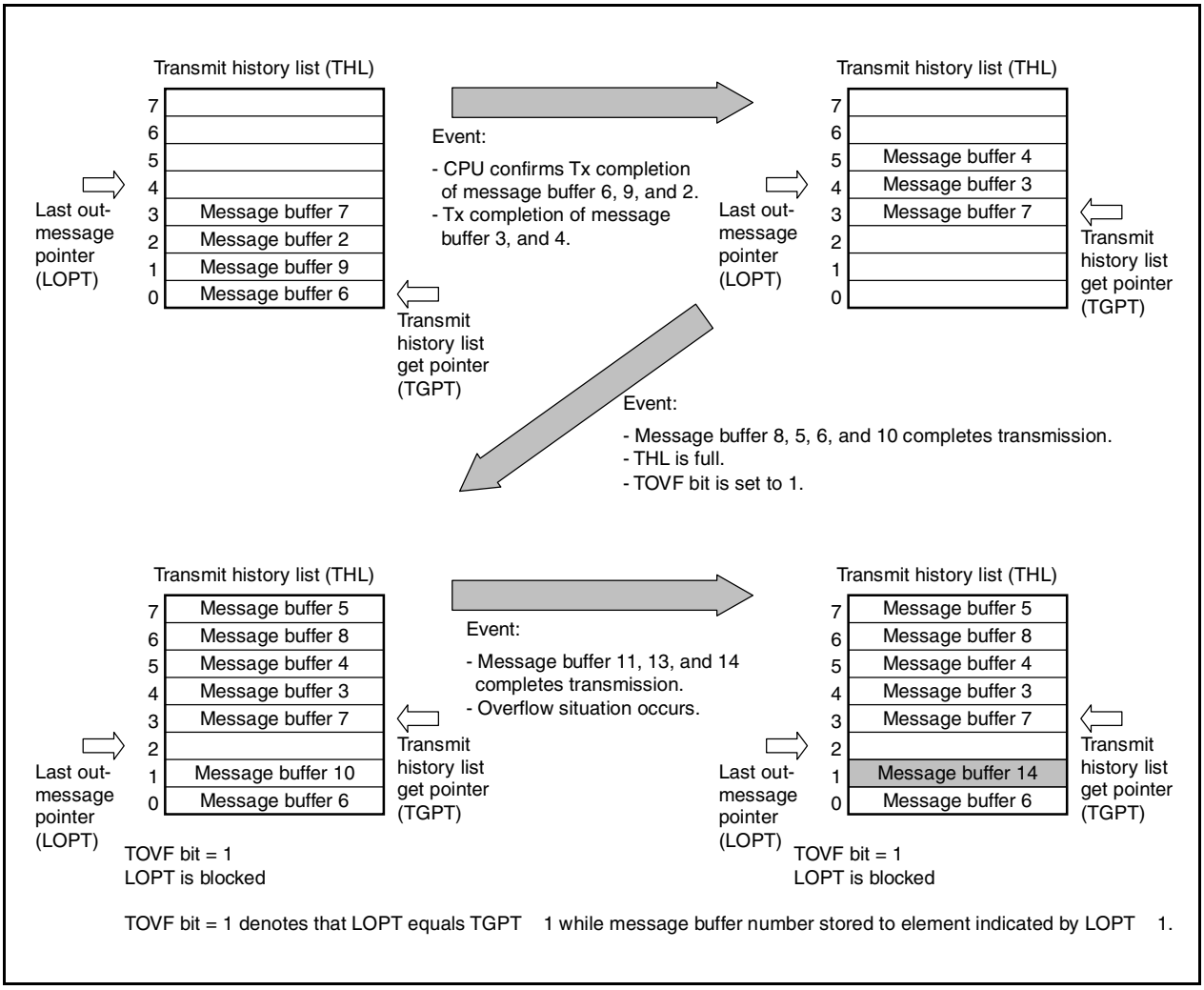


Figure 20-8. Operation of UF0BO2 Register (1/2)

(a) Operation example 1

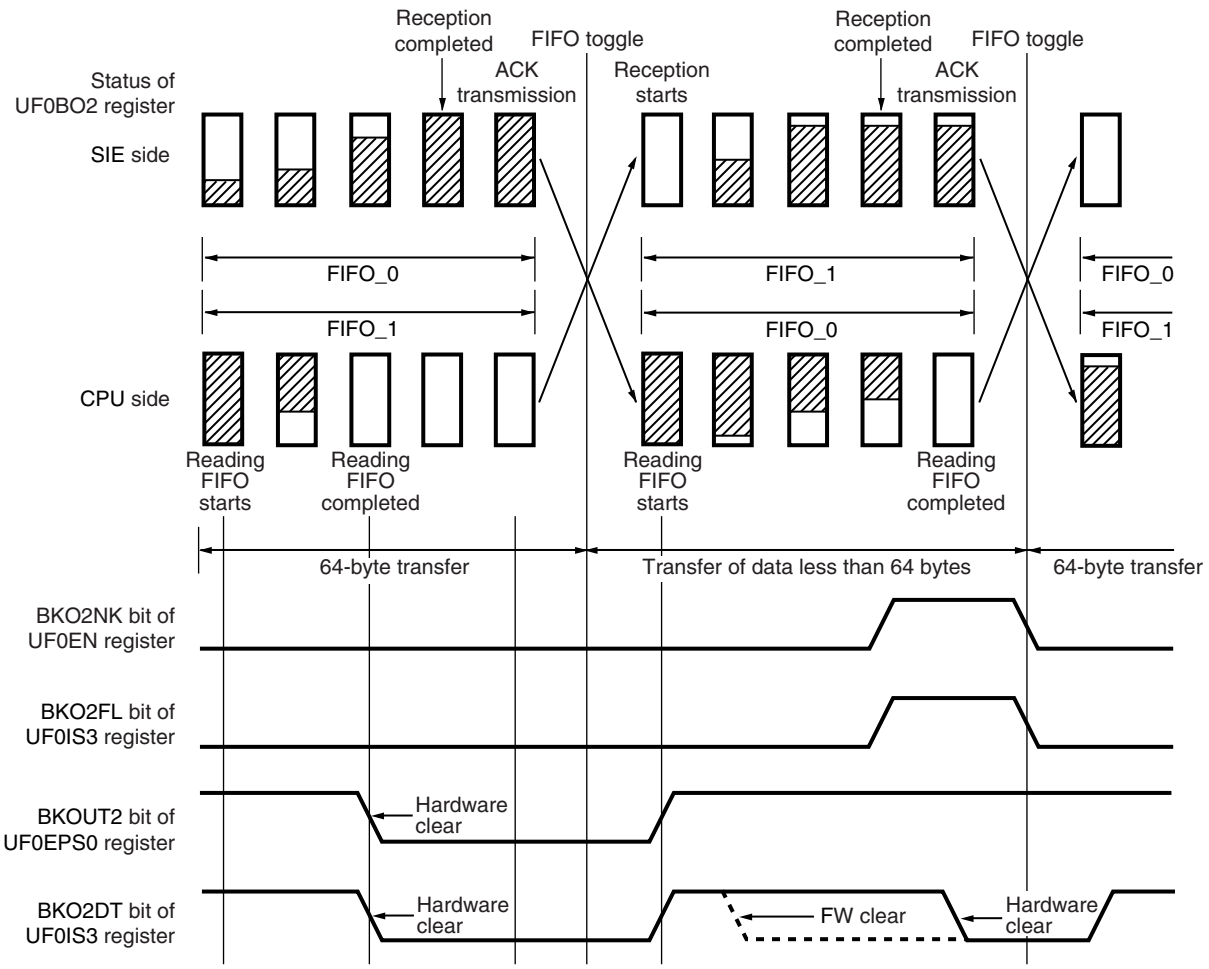
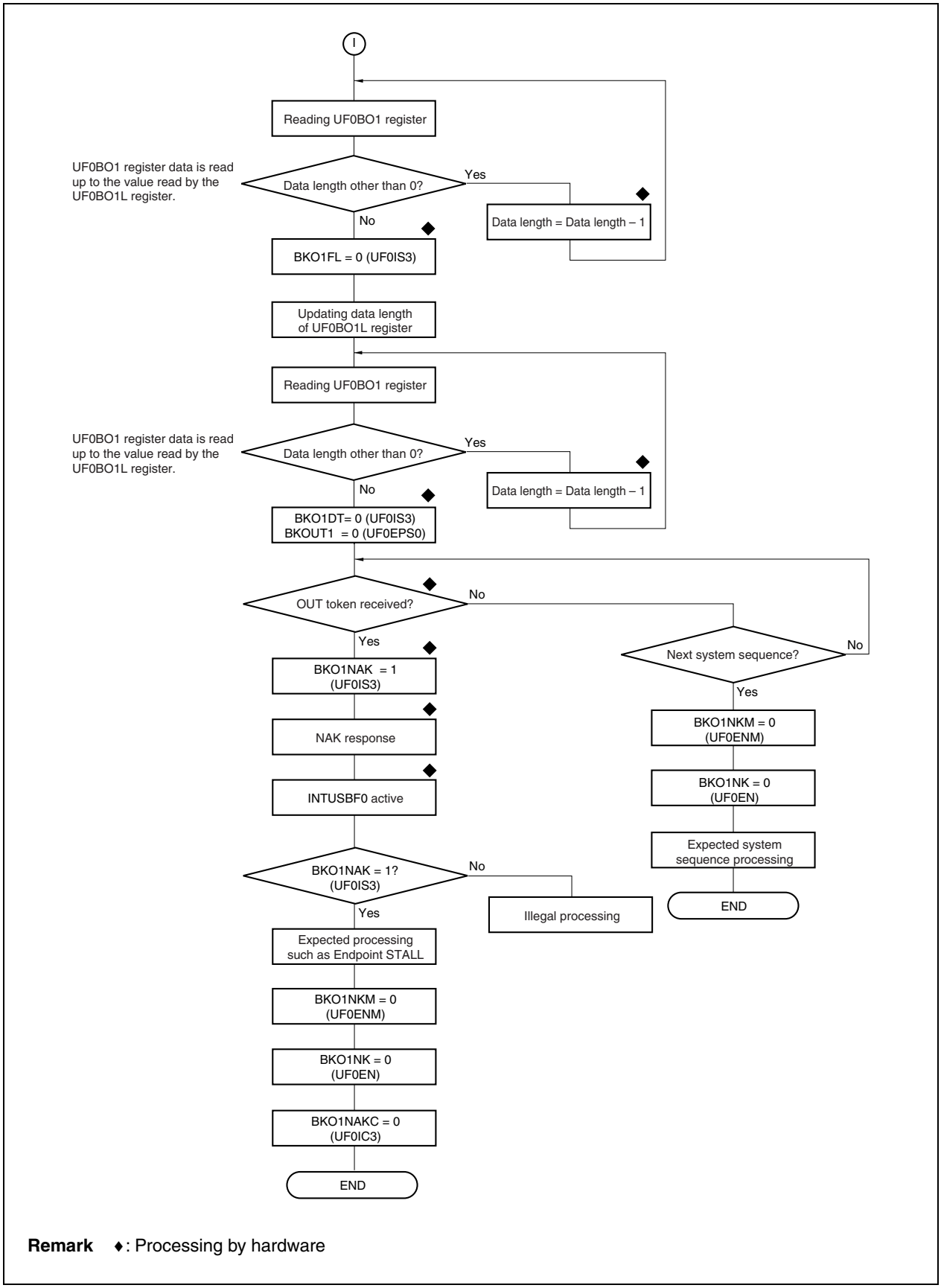


Table 20-9. FW-Supported Standard Requests

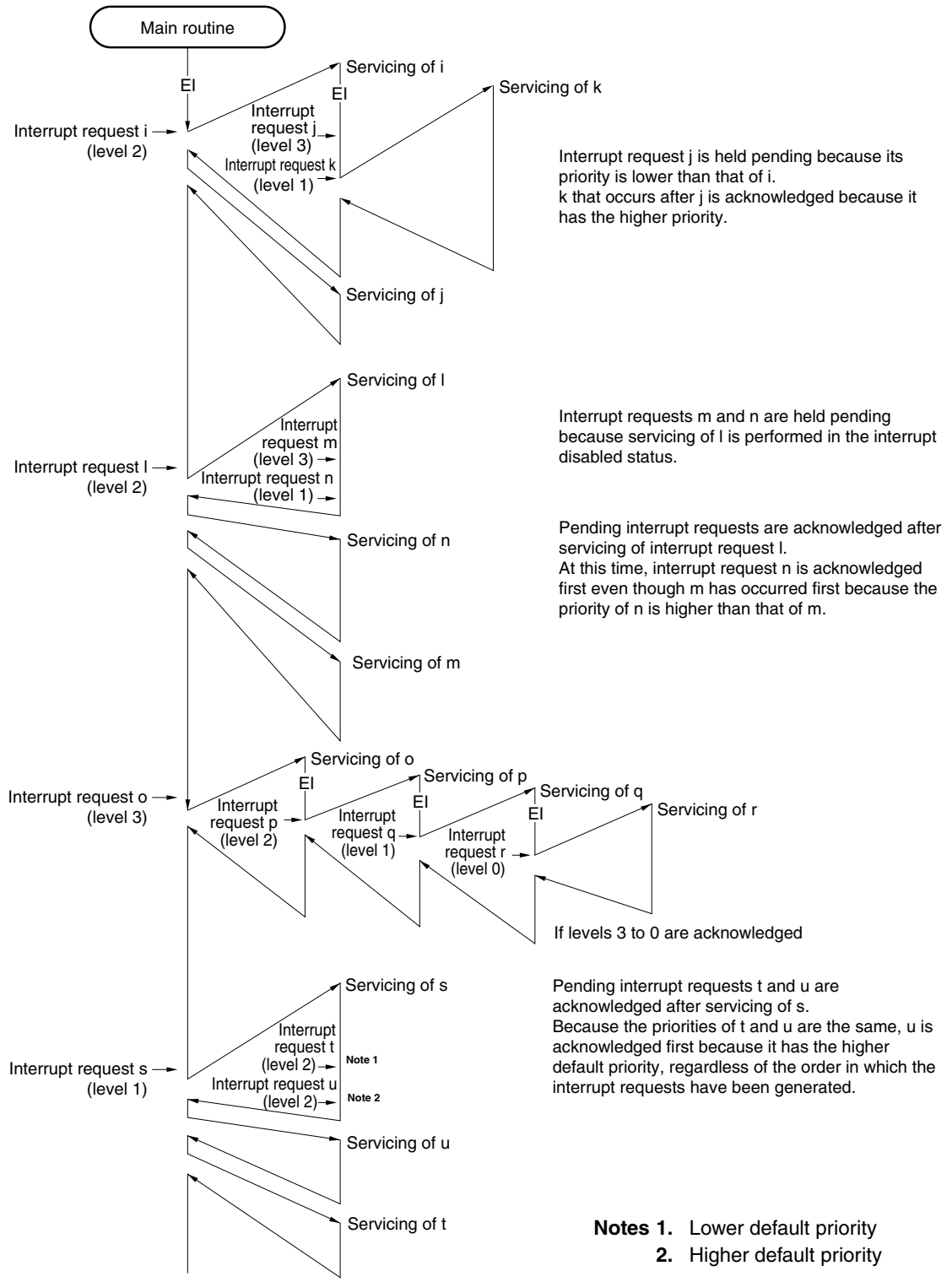
Request	Reception Side	Processing/ Frequency	Explanation
CLEAR_FEATURE	Interface	Automatic STALL response	It is considered that this request does not come to Interface because there is no function selector value, though it is reserved for bmRequestType. When this request is received, the hardware makes an automatic STALL response.
SET_FEATURE	Interface	Automatic STALL response	It is considered that this request does not come to Interface because there is no function selector value, though it is reserved for bmRequestType. When this request is received, the hardware makes an automatic STALL response.
GET_DESCRIPTOR	String	FW	Returns the string descriptor. When this request is received by the SETUP token, the hardware generates the CPUDEC interrupt request for FW. FW decodes the contents of the request from the CPUDEC interrupt request, and writes the data to be returned to the host, to the UF0E0W register.
SET_DESCRIPTOR	Device	FW	Rewrites the device descriptor. When this request is received by the SETUP token, the hardware generates the CPUDEC interrupt request for FW. FW decodes the contents of the request from the CPUDEC interrupt request, and the writes the data for the next control transfer (OUT) to the UF0DDn register (n = 0 to 17).
SET_DESCRIPTOR	Configuration	FW	Rewrites the configuration descriptor. When this request is received by the SETUP token, the hardware generates the CPUDEC interrupt request for FW. FW decodes the contents of the request from the CPUDEC interrupt request, and the writes the data for the next control transfer (OUT) to the UF0CIEn register (n = 0 to 255).
SET_DESCRIPTOR	String	FW	Rewrites the string descriptor. When this request is received by the SETUP token, the hardware generates the CPUDEC interrupt request for FW. FW decodes the contents of the request from the CPUDEC interrupt request, and loads the data for the next control transfer (OUT).
Other	NA	FW	When this request is received by the SETUP token, the hardware generates the CPUDEC interrupt request for FW. FW decodes the contents of the request from the CPUDEC interrupt request, and performs the necessary processing.

Figure 20-28. Processing If More Data Than Expected by System Is Transmitted (Endpoint2) (2/2)



Remark ♦: Processing by hardware

Figure 22-7. Example of Processing in Which Another Interrupt Request Signal Is Issued While an Interrupt Is Being Serviced (2/2)



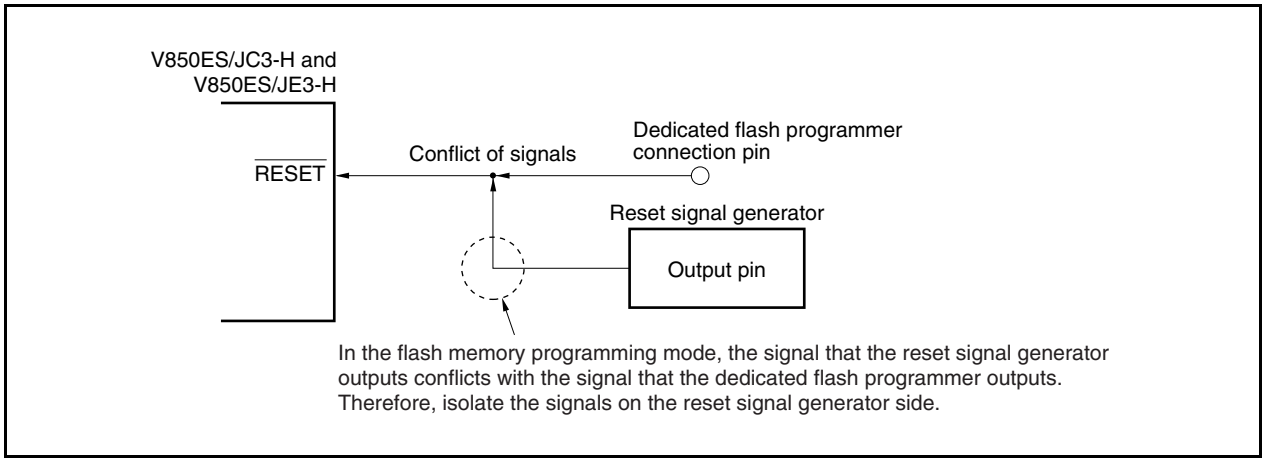
Caution To perform multiple interrupt servicing, the values of the EIPC and EIPSW registers must be saved before executing the EI instruction. When returning from multiple interrupt servicing, restore the values of EIPC and EIPSW after executing the DI instruction.

(4) $\overline{\text{RESET}}$ pin

When the reset signals of the dedicated flash programmer are connected to the $\overline{\text{RESET}}$ pin that is connected to the reset signal generator on-board, a conflict of signals occurs. To avoid the conflict of signals, isolate the connection to the reset signal generator.

When a reset signal is input from the user system in the flash memory programming mode, the programming operation will not be performed correctly. Therefore, do not input signals other than the reset signals from the dedicated flash programmer.

Figure 30-16. Conflict of Signals ($\overline{\text{RESET}}$ Pin)



(5) Port pins (including NMI)

When the system shifts to the flash memory programming mode, all the pins that are not used for flash memory programming are in the same status as that immediately after reset. If the external device connected to each port does not recognize the status of the port immediately after reset, pins require appropriate processing, such as connecting to V_{DD} via a resistor or connecting to V_{SS} via a resistor.

(6) Other signal pins

Connect X1, X2, XT1, XT2, and REGC in the same status as that in the normal operation mode.

During flash memory programming, input a low level to the $\overline{\text{DRST}}$ pin or leave it open. Do not input a high level.

(7) Power supply

Supply the same power (V_{DD}, V_{SS}, EV_{DD}, UV_{DD}, AV_{REF0}, AV_{REF1}, AV_{SS}) as in normal operation mode.

(24/34)

Symbol	Name	Unit	Page
TM0CMP0	TMM0 compare register 0	Timer	520
TM0CTL0	TMM0 control register 0	Timer	521
TM0EQIC0	Interrupt control register	INTC	1222
TM1CMP0	TMM1 compare register 0	Timer	520
TM1CTL0	TMM1 control register 0	Timer	521
TM1EQIC0	Interrupt control register	INTC	1222
TM2CMP0	TMM2 compare register 0	Timer	520
TM2CTL0	TMM2 control register 0	Timer	521
TM2EQIC0	Interrupt control register	INTC	1222
TM3CMP0	TMM3 compare register 0	Timer	520
TM3CTL0	TMM3 control register 0	Timer	521
TM3EQIC0	Interrupt control register	INTC	1222
TTNFC	Noise elimination control register	Timer	410
TRXIC0	Interrupt control register	INTC	1222
TT0CCIC0	Interrupt control register	INTC	1222
TT0CCIC1	Interrupt control register	INTC	1222
TT0CCR0	TMT0 capture/compare register 0	Timer	405
TT0CCR1	TMT0 capture/compare register 1	Timer	407
TT0CNT	TMT0 counter read buffer register	Timer	409
TT0CTL0	TMT0 control register 0	Timer	391
TT0CTL1	TMT0 control register 1	Timer	392
TT0CTL2	TMT0 control register 2	Timer	394
TT0IECIC	Interrupt control register	INTC	1222
TT0IOC0	TMT0 I/O control register 0	Timer	396
TT0IOC1	TMT0 I/O control register 1	Timer	398
TT0IOC2	TMT0 I/O control register 2	Timer	399
TT0IOC3	TMT0 I/O control register 3	Timer	400
TT0OPT0	TMT0 option register 0	Timer	402
TT0OPT1	TMT0 option register 1	Timer	403
TT0OVIC	Interrupt control register	INTC	1222
TT0TCW	TMT0 count write register	Timer	409
UC0CTL0	UARTC0 control register 0	UARTC	679
UC0CTL1	UARTC0 control register 1	UARTC	707
UC0CTL2	UARTC0 control register 2	UARTC	708
UC0OPT0	UARTC0 option control register 0	UARTC	681
UC0OPT1	UARTC0 option control register 1	UARTC	683
UC0RIC	Interrupt control register	INTC	1222
UC0RX	UARTC0 receive data register	UARTC	687
UC0RXL	UARTC0 receive data register L	UARTC	687
UC0STR	UARTC0 status register	UARTC	685
UC0TIC	Interrupt control register	INTC	1222
UC0TX	UARTC0 transmit data register	UARTC	688
UC0TX	UARTC0 transmit data register L	UARTC	688

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