Renesas Electronics America Inc - UPD70F3825GB-GAH-AX Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, CSI, EBI/EMI, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	45
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 10x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3825gb-gah-ax

(1) TAAn control register 0 (TAAnCTL0)

The TAAnCTL0 register is an 8-bit register that controls the operation of TAAn.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

The same value can always be written to the TAAnCTL0 register by software.

After reset: 00H R/W Address: TAA0CTL0 FFFFF630H, TAA1CTL0 FFFFF640H, TAA2CTL0 FFFFF650H, TAA4CTL0 FFFFF670H

TAAnCTL0 (n = 0 to 2, 4)

7	6	5	4	3	2	1	0
TAAnCE	0	0	0	0	TAAnCKS2	TAAnCKS1	TAAnCKS0

TAAnCE	TAAn operation control
0	TAAn operation disabled (TAAn reset asynchronously[Note]).
1	TAAn operation enabled. TAAn operation started.

TAAnCKS2	TAAnCKS1	TAAnCKS0	Internal count clock selection	
			n = 0, 1, 4	n = 2
0	0	0	fxx (20.8 ns)	fxx/2 (41.7 ns)
0	0	1	fxx/2 (41.7 ns)	fxx/4 (83.3 ns)
0	1	0	fxx/4 (83.3 ns)	fxx/8 (166.7 ns)
0	1	1	fxx/8 (166.7 ns)	fxx/16 (333.3 ns)
1	0	0	fxx/16 (333.3 ns)	fxx/64 (1.3333 μs)
1	0	1	fxx/32 (666.7 ns)	fxx/256 (5.3333 μs)
1	1	0	fxx/64 (1.3333 μs)	fxx/512 (10.6667 μs)
1	1	1	fxx/128 (2.6667 μs)	fxx/1024 (21.3333 μs)

Note TAAnOPT0.TAAnOVF bit, 16-bit counter, timer output (TOAAn0, TOAAn1 pins)

Cautions 1. Set the TAAnCKS2 to TAAnCKS0 bits when the TAAnCE bit = 0. When the value of the TAAnCE bit is changed from 0 to 1, the TAAnCKS2 to TAAnCKS0 bits can be set simultaneously.

2. Be sure to set bits 3 to 6 to "0".

Remark fxx: Main clock frequency

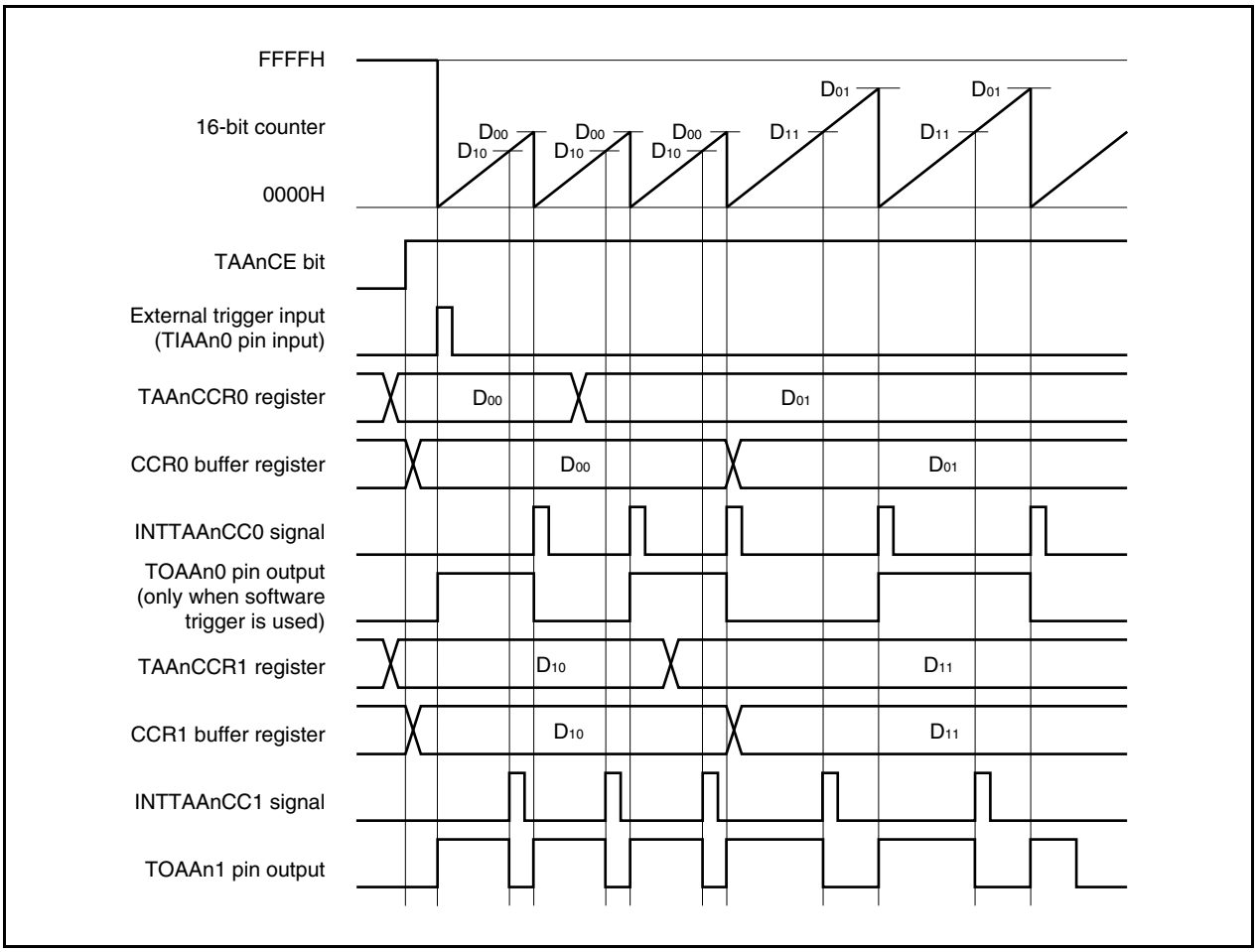
The values in parentheses indicate the cycles when fxx = 48 MHz.

(2) External trigger pulse output mode operation timing

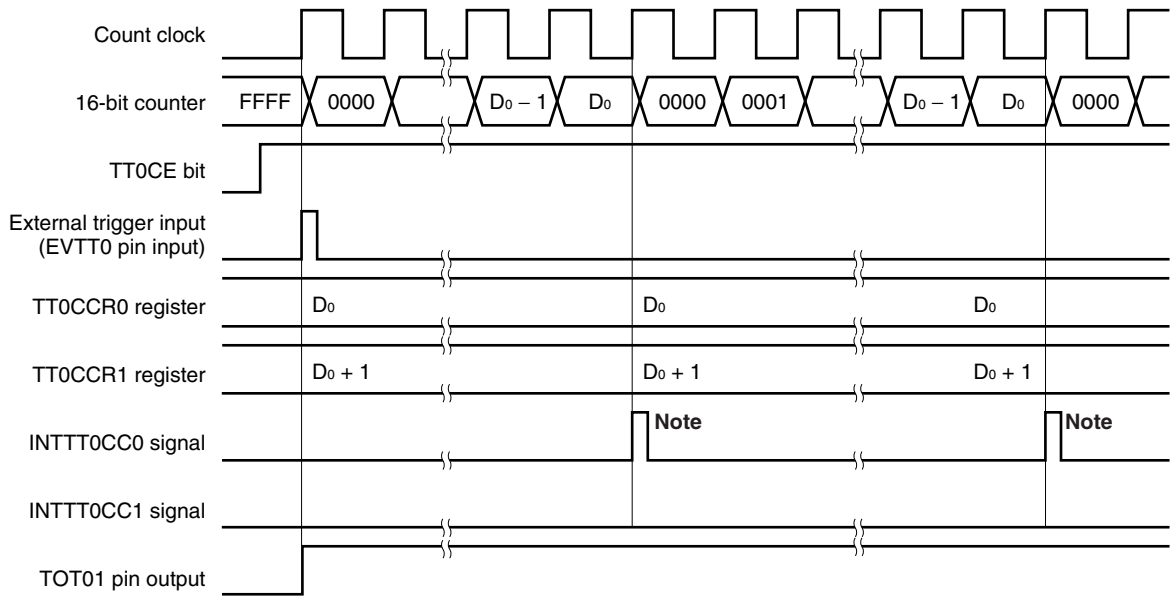
(a) Note on changing pulse width during operation

To change the PWM waveform while the counter is operating, write the TAAnCCR1 register last.

Rewrite the TAAnCCRm register after writing the TAAnCCR1 register after the INTTAAnCC0 signal is detected.



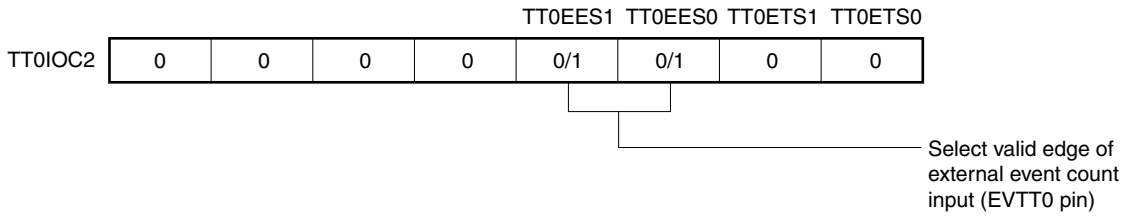
To output a 100% waveform, set a value of (set value of TT0CCR0 register + 1) to the TT0CCR1 register. If the set value of the TT0CCR0 register is FFFFH, 100% output cannot be produced.



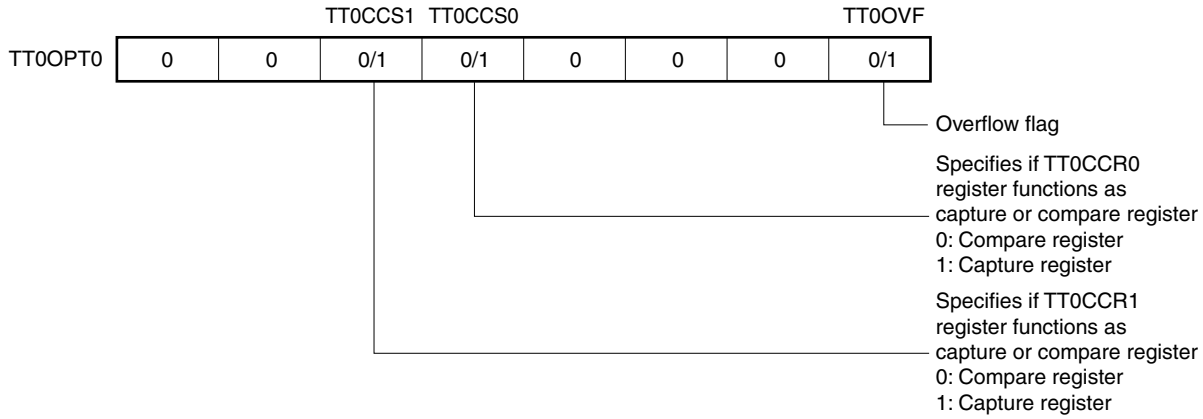
Note The timing is actually delayed by one operating clock (fxx).

Figure 8-36. Register Setting in Free-Running Timer Mode (2/2)

(e) TMT0 I/O control register 2 (TT0IOC2)



(f) TMT0 option register 0 (TT0OPT0)



(g) TMT0 counter read buffer register (TT0CNT)

The value of the 16-bit counter can be read by reading the TT0CNT register.

(h) TMT0 capture/compare registers 0 and 1 (TT0CCR0 and TT0CCR1)

These registers function as capture registers or compare registers depending on the setting of the TT0OPT0.TT0CCSn bit.

When the registers function as capture registers, they store the count value of the 16-bit counter when the valid edge input to the TIT0n pin is detected.

When the registers function as compare registers and when D_a is set to the TT0CCRn register, the INTTT0CCn signal is generated when the counter reaches (D_a + 1), and the output signals of the TOT00 and TOT01 pins are inverted.

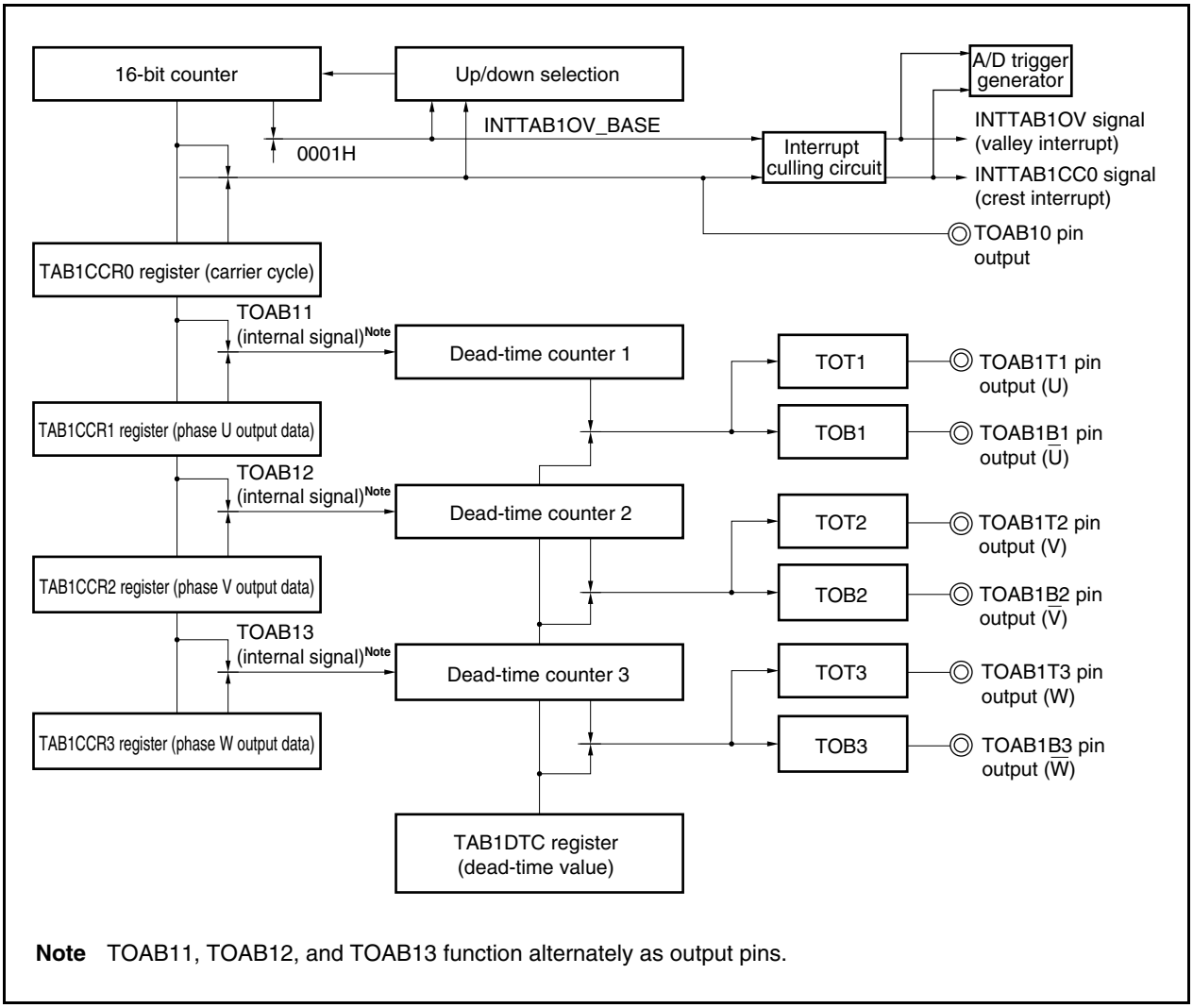
Remark n = 0, 1

(2) Operation timing in pulse width measurement mode

(a) Clearing overflow flag

The overflow flag can be cleared to 0 by clearing the TT0OVF bit to 0 with the CLR instruction after reading the TT0OVF bit when it is 1 and by writing 8-bit data (bit 0 is 0) to the TT0OPT0 register after reading the TT0OVF bit when it is 1.

Figure 10-5. Outline of 6-Phase PWM Output Mode



Note TOAB11, TOAB12, and TOAB13 function alternately as output pins.

Cautions 1. The A/D conversion start trigger signal output that is set by the TAB1AT2 and TAB1AT3 bits can be used only when TAA4 is performing a tuning operation as the slave timer of TAB1. If TAB1 and TAA4 are not performing a tuning operation, or if a mode other than the 6-phase PWM output mode is used, the output cannot be guaranteed.

2. The TAB1 signal output is internally used to identify whether the 16-bit counter is counting up or down. Therefore, enable TOAB10 pin output by clearing the TAB1IOC0.TAB1OL0 bit to 0 and setting the TAB1IOC0.TAB1OE0 bit to 1.

14.5 Operation

14.5.1 Basic operation

<1> Set the operation mode, trigger mode, and conversion time for executing A/D conversion by using the ADA0M0, ADA0M1, ADA0M2, and ADA0S registers. When the ADA0CE bit of the ADA0M0 register is set, conversion is started in the software trigger mode and the A/D converter waits for a trigger in the external or timer trigger mode.

<2> When A/D conversion is started, the voltage input to the selected analog input channel is sampled by the sample & hold circuit.

<3> When the sample & hold circuit samples the input channel for a specific time, it enters the hold status, and holds the input analog voltage until A/D conversion is complete.

<4> Set bit 9 of the successive approximation register (SAR), and set the compare voltage generation DAC to (1/2) AV_{REF0}.

<5> The voltage difference between the voltage of the compare voltage generation DAC and the analog input voltage is compared by the voltage comparator. If the analog input voltage is higher than (1/2) AV_{REF0}, the MSB of the SAR remains set. If it is lower than (1/2) AV_{REF0}, the MSB is reset.

<6> Next, bit 8 of the SAR is automatically set and the next comparison is started. Depending on the value of bit 9, to which a result has been already set, the compare voltage generation DAC is selected as follows.

- Bit 9 = 1: (3/4) AV_{REF0}
- Bit 9 = 0: (1/4) AV_{REF0}

This compare voltage and the analog input voltage are compared and, depending on the result, bit 8 is manipulated as follows.

Analog input voltage ≥ Compare voltage: Bit 8 = 1

Analog input voltage ≤ Compare voltage: Bit 8 = 0

<7> This comparison is continued to bit 0 of the SAR.

<8> When comparison of the 10 bits is complete, the valid digital result remains in the SAR, and is then transferred to and stored in the ADA0CRn register. After that, an A/D conversion end interrupt request signal (INTAD) is generated.

<9> In one-shot select mode, conversion is stopped[Note]. In one-shot scan mode, conversion is stopped after scanning once[Note]. In continuous select mode, repeat steps <2> to <8> until the ADA0M0.ADA0CE bit is cleared to 0. In continuous scan mode, repeat steps <2> to <8> for each channel.

Note In the external trigger mode, timer trigger mode 0, or timer trigger mode 1, the trigger standby status is entered.

Remark The trigger standby status means the status after the stabilization time has elapsed.

(4/4)

SPTn	Stop condition trigger
0	Stop condition is not generated.
1	Stop condition is generated (termination of master device's transfer). After the SDA0n line goes to low level, either set the SCL0n line to high level or wait until the SCL0n pin goes to high level. Next, after the rated amount of time has elapsed, the SDA0n line is changed from low level to high level and a stop condition is generated.

Cautions concerning set timing

For master reception: Cannot be set to 1 during transfer.
Can be set to 1 only when the ACKEn bit has been set to 0 and during the wait period after the slave has been notified of final reception.

For master transmission: A stop condition may not be generated normally during the $\overline{\text{ACK}}$ reception period. Set to 1 during the wait period that follows output of the ninth clock.

- Cannot be set to 1 at the same time as the STTn bit.
- The SPTn bit can be set to 1 only when in master mode[Note].
- When the WTIMn bit has been set to 0, if the SPTn bit is set to 1 during the wait period that follows output of eight clocks, note that a stop condition will be generated during the high-level period of the ninth clock.
  The WTIMn bit should be changed from 0 to 1 during the wait period following output of eight clocks, and the SPTn bit should be set to 1 during the wait period that follows output of the ninth clock.
- When the SPTn bit is set to 1, setting the SPTn bit to 1 again is disabled until the setting is cleared to 0.

Condition for clearing (SPTn bit = 0)	Condition for setting (SPTn bit = 1)
• Cleared by loss in arbitration • Automatically cleared after stop condition is detected • Cleared when the LRELn bit = 1 (communication save) • When the IICEn bit = 0 (operation stop) • After reset	• Set by instruction

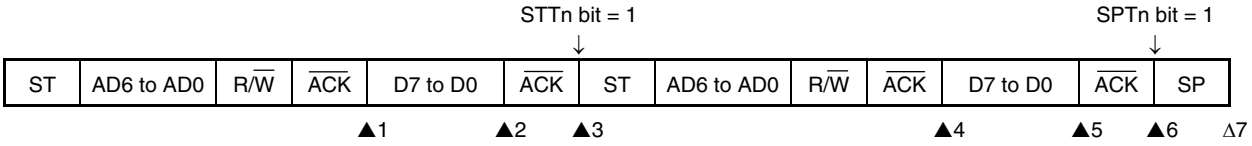
Note Set the SPTn bit to 1 only in master mode. However, to perform a master operation before detecting the first stop condition after operation has been enabled when the IICRSVn bit is 0, the SPTn bit must be set to 1 and a stop condition must be set. For details, see **18.15 Cautions**.

Caution If the WRELn bit is set to 1 during the ninth clock and the wait state is canceled when the TRCn bit is 1, the TRCn bit is cleared to 0 and the SDA0n line is set to high impedance.

Remark The SPTn bit is 0 if it is read immediately after data setting.

(2) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop (restart)

<1> When WTIMn bit = 0



▲1: IICSn register = 1000X110B

▲2: IICSn register = 1000X000B (WTIMn bit = 1)

▲3: IICSn register = 1000XX00B (WTIMn bit = 0)

▲4: IICSn register = 1000X110B (WTIMn bit = 0)

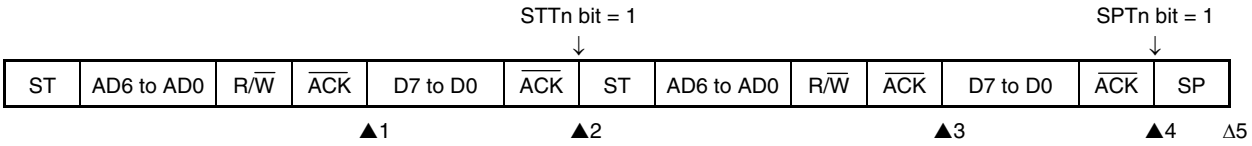
▲5: IICSn register = 1000X000B (WTIMn bit = 1)

▲6: IICSn register = 1000XX00B

Δ 7: IICSn register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIEn bit = 1
X: don't care

<2> When WTIMn bit = 1



▲1: IICSn register = 1000X110B

▲2: IICSn register = 1000XX00B

▲3: IICSn register = 1000X110B

▲4: IICSn register = 1000XX00B

Δ 5: IICSn register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIEn bit = 1
X: don't care

18.7.4 Operation without communication

(1) Start ~ Code ~ Data ~ Data ~ Stop

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

Δ1

Δ 1: IICSn register = 00000001B

Remarks Δ: Generated only when SPIEn bit = 1

18.7.5 Arbitration loss operation (operation as slave after arbitration loss)

(1) When arbitration loss occurs during transmission of slave address data

<1> When IICCn.WTIMn bit = 0

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 ▲3 Δ4

▲1: IICSn register = 0101X110B (Example: When IICSn.ALDn bit is read during interrupt servicing)

▲2: IICSn register = 0001X000B

▲3: IICSn register = 0001X000B

Δ 4: IICSn register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIEn bit = 1
X: don't care

<2> When WTIMn bit = 1

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 ▲3 Δ4

▲1: IICSn register = 0101X110B (Example: When ALDn bit is read during interrupt servicing)

▲2: IICSn register = 0001X100B

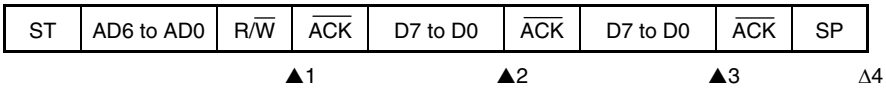
▲3: IICSn register = 0001XX00B

Δ 4: IICSn register = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIEn bit = 1
X: don't care

(2) When arbitration loss occurs during transmission of extension code

<1> When WTIMn bit = 0



▲1: IICSn register = 0110X010B (Example: When ALDn bit is read during interrupt servicing)

▲2: IICSn register = 0010X000B

▲3: IICSn register = 0010X000B

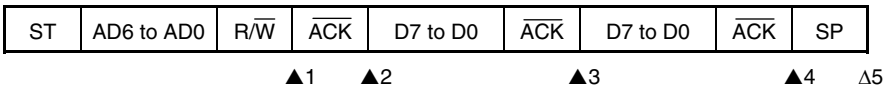
Δ 4: IICSn register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIEn bit = 1

X: don't care

<2> When WTIMn bit = 1



▲1: IICSn register = 0110X010B (Example: When ALDn bit is read during interrupt servicing)

▲2: IICSn register = 0010X110B

▲3: IICSn register = 0010X100B

▲4: IICSn register = 0010XX00B

Δ 5: IICSn register = 00000001B

Remark ▲: Always generated

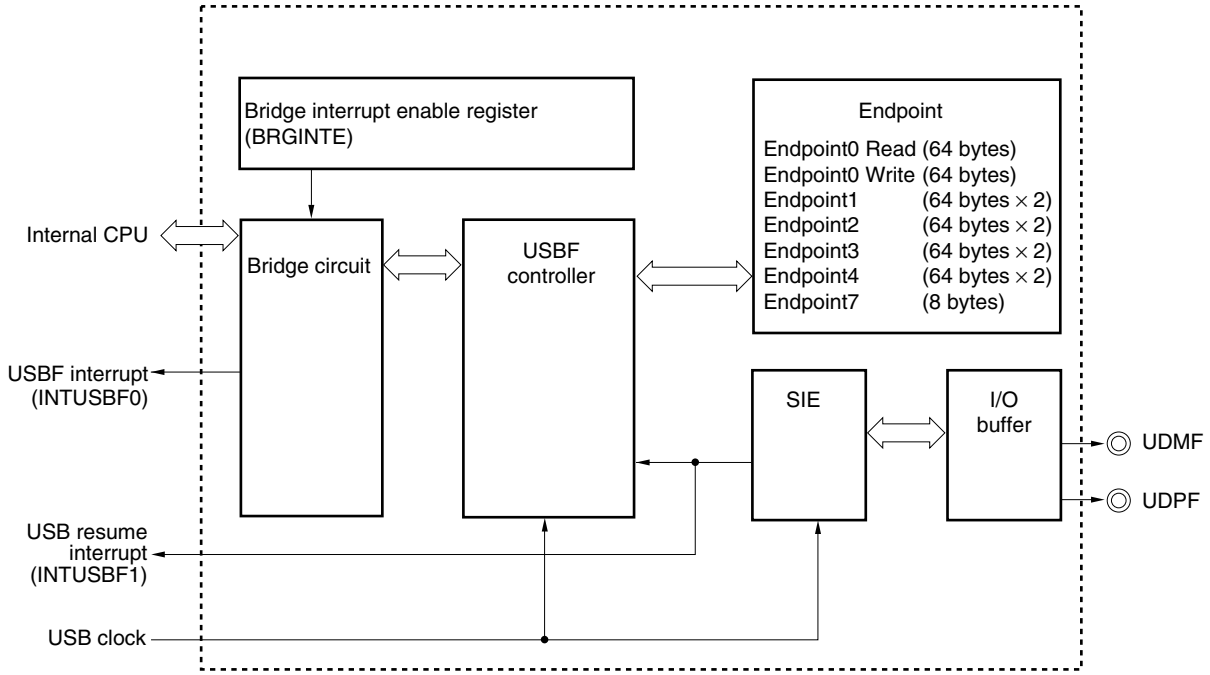
Δ: Generated only when SPIEn bit = 1

X: don't care

20.2 Configuration

20.2.1 Block diagram

Figure 20-1. Block Diagram of USB Function Controller



Remark Area enclosed with dashed line: These functions are included in the USB function controller.

(38) UF0 endpoint 1 interface mapping register (UF0E1IM)

This register specifies for which Interface and Alternative Setting Endpoint1 is valid.

This register can be read or written in 8-bit units.

The setting of this register and the Alternative Setting selected by the SET_INTERFACE request indicate whether Endpoint1 is currently valid, and the hardware determines how the GET_STATUS/CLEAR_FEATURE/SET_FEATURE Endpoint1 request and the IN transaction to Endpoint1 are responded to, and whether the related bits are valid or invalid.

	7	6	5	4	3	2	1	0	Address	After reset
UF0E1IM	E1EN2	E1EN1	E1EN0	E12AL1	E15AL4	E15AL3	E15AL2	E15AL1	00200086H	00H

Bit position	Bit name	Function
7 to 5	E1EN2 to E1EN0	These bits set a link between the Interface of Endpoint1 and the two-/five-series Alternative Setting. The endpoint is linked with Alternative Setting 0. The endpoint linked with Alternative Setting 0 cannot be excluded from Alternative Setting 1 to 4.

E1EN2	E1EN1	E1EN0	Link status
1	1	1	Not linked with Interface
1	1	0	
1	0	1	Linked with Interface 4 and Alternative Setting 0
1	0	0	Linked with Interface 3 and Alternative Setting 0
0	1	1	Linked with Interface 2 and Alternative Setting 0
0	1	0	Linked with Interface 1 and Alternative Setting 0
0	0	1	Linked with Interface 0 and Alternative Setting 0
0	0	0	Not linked with Interface (default value)

When these bits are set to 110 or 111, they are invalid even if the E12AL1 bit is cleared to 0.

If the endpoint is linked, setting of the CONF bit of the UF0MODS register to 1 indicates that Endpoint1 is valid.

4	E12AL1	This bit validates Endpoint1 when the two-series Alternative Setting and the Alternative Setting of the linked Interface are set to 1. 1: Validate the endpoint when Alternative Setting 1 is set with CONF bit = 1. 0: Do not validate the endpoint even when Alternative Setting 1 is set with CONF bit = 1 (default value). This bit is valid when the E15AL4 to E15AL1 bits are 0000.
3 to 0	E15ALn	These bits validate Endpoint1 when the five-series Alternative Setting and the Alternative Setting of the linked Interface are set to n. 1: Validate the endpoint when Alternative Setting n is set with CONF bit = 1. 0: Do not validate the endpoint even when Alternative Setting n is set with CONF bit = 1 (default value).

Remark n = 1 to 4

(6) UF0 EP4 status register L (UF0E4SL)

This register stores the value that is to be returned in response to the GET_STATUS Endpoint4 request.

This register can be read or written in 8-bit units. Note, however, that data can be written to this register only when the EP0NKA bit is set to 1.

If an error occurs in Endpoint4, the E4HALT bit is set to 1. A write access to this register is ignored while a USB-side access to Endpoint4 is being received.

The hardware automatically transmits the contents of this register to the host when it has received the GET_STATUS Endpoint4 request. If Endpoint4 has stalled, the UF0BO2 register is cleared and the BKO2NK bit is cleared to 0.

Because writing this register is always masked when transfer to Endpoint4, rather than control transfer, is executed, be sure to check this register to see if data has been correctly written to it.

Caution To rewrite this register, set the EP0NKA bit to 1 before reading the register contents, and rewrite the register contents after confirming that the bit has been set, in order to prevent conflict between a read access and a write access.

	7	6	5	4	3	2	1	0	Address	After reset
UF0E4SL	0	0	0	0	0	0	0	E4HALT	0020015CH	00H

Bit position	Bit name	Function
0	E4HALT	This bit indicates the status of Endpoint4. 1: Stalled 0: Not stalled This bit is set to 1 by hardware when the SET_FEATURE Endpoint4 request has been received. It is cleared to 0 by hardware when the CLEAR_FEATURE Endpoint4 request, SET_CONFIGURATION request, or the SET_INTERFACE request for the Interface to which Endpoint4 is linked has correctly been received. DATA PID is initialized to DATA0.

21.6 Transfer Types

As a transfer type, the 2-cycle transfer is supported.

In two-cycle transfer, data transfer is performed in two cycles, a read cycle and a write cycle.

In the read cycle, the transfer source address is output and reading is performed from the source to the DMAC. In the write cycle, the transfer destination address is output and writing is performed from the DMAC to the destination.

An idle cycle of one clock is always inserted between a read cycle and a write cycle. If the data bus width differs between the transfer source and destination for DMA transfer of two cycles, the operation is performed as follows.

<16-bit data transfer>

<1> Transfer from 32-bit bus → 16-bit bus
A read cycle (the higher 16 bits are in a high-impedance state) is generated, followed by generation of a write cycle (16 bits).

<2> Transfer from 16-/32-bit bus to 8-bit bus
A 16-bit read cycle is generated once, and then an 8-bit write cycle is generated twice.

<3> Transfer from 8-bit bus to 16-/32-bit bus
An 8-bit read cycle is generated twice, and then a 16-bit write cycle is generated once.

<4> Transfer between 16-bit bus and 32-bit bus
A 16-bit read cycle is generated once, and then a 16-bit write cycle is generated once.

For DMA transfer executed to an on-chip peripheral I/O register (transfer source/destination), be sure to specify the same transfer size as the register size. For example, for DMA transfer to an 8-bit register, be sure to specify byte (8-bit) transfer.

Remark The bus width of each transfer target (transfer source/destination) is as follows.

- On-chip peripheral I/O: 16-bit bus width
- Internal RAM: 32-bit bus width

27.3 Registers

The low-voltage detector is controlled by the following registers.

- Low-voltage detection register (LVIM)
- Internal RAM data status register (RAMS)

(1) Low-voltage detection register (LVIM)

The LVIM register is a special register. This can be written only in the special combination of the sequences (see **3.4.8 Special registers**).

The LVIM register is used to enable or disable low-voltage detection, and to set the operation mode of the low-voltage detector.

This register can be read or written in 8-bit or 1-bit units. However, the LVIF bit is read-only.

After reset: 00H[Note 1] R/W Address: FFFFF890H

	<7>	6	5	4	3	2	<1>	<0>
LVIM	LVION	0	0	0	0	0	LVIMD	LVIF

LVION	Low-voltage detection operation enable or disable
0	Disable operation.
1	Enable operation.

LVIMD	Selection of operation mode of low-voltage detection
0	Generates interrupt signal INTLVI when the supply voltage drops or rises across the detection voltage value.
1	Generates internal reset signal LVIRES when the supply voltage drops across the detected voltage value.

LVIF[Note 2]	Low-voltage detection flag
0	When supply voltage > detected voltage, or when operation is disabled
1	Supply voltage of connected power supply < detected voltage

Notes 1. Reset by low-voltage detection: 82H
Reset due to other source: 00H

2. After the LVI operation has started (LVION bit = 1) or when INTLVI has occurred, confirm the supply voltage state using the LVIF bit.

Cautions 1. When the LVION and LVIMD bits to 1, the low-voltage detector cannot be stopped until the reset request due to other than the low-voltage detection is generated.

2. When the LVION bit is set to 1, the comparator in the LVI circuit starts operating. Wait 0.2 ms or longer by software before checking the voltage at the LVIF bit after the LVION bit is set.

3. Be sure to set bits 6 to 2 to "0".

(32/34)

Symbol	Name	Unit	Page
UF0CIE253	UF0 configuration/interface/endpoint descriptor register 253	USBF	1118
UF0CIE254	UF0 configuration/interface/endpoint descriptor register 254	USBF	1118
UF0CIE255	UF0 configuration/interface/endpoint descriptor register 255	USBF	1118
UF0CLR	UF0 CLR request register	USBF	1039
UF0CNF	UF0 configuration register	USBF	1113
UF0DD0	UF0 device descriptor register 0	USBF	1117
UF0DD1	UF0 device descriptor register 1	USBF	1117
UF0DD2	UF0 device descriptor register 2	USBF	1117
UF0DD3	UF0 device descriptor register 3	USBF	1117
UF0DD4	UF0 device descriptor register 4	USBF	1117
UF0DD5	UF0 device descriptor register 5	USBF	1117
UF0DD6	UF0 device descriptor register 6	USBF	1117
UF0DD7	UF0 device descriptor register 7	USBF	1117
UF0DD8	UF0 device descriptor register 8	USBF	1117
UF0DD9	UF0 device descriptor register 9	USBF	1117
UF0DD10	UF0 device descriptor register 10	USBF	1117
UF0DD11	UF0 device descriptor register 11	USBF	1117
UF0DD12	UF0 device descriptor register 12	USBF	1117
UF0DD13	UF0 device descriptor register 13	USBF	1117
UF0DD14	UF0 device descriptor register 14	USBF	1117
UF0DD15	UF0 device descriptor register 15	USBF	1117
UF0DD16	UF0 device descriptor register 16	USBF	1117
UF0DD17	UF0 device descriptor register 17	USBF	1117
UF0DEND	UF0 data end register	USBF	1069
UF0DMS0	UF0 DMA status 0 register	USBF	1065
UF0DMS1	UF0 DMA status 1 register	USBF	1066
UF0DSCL	UF0 descriptor length register	USBF	1116
UF0DSTL	UF0 device status register L	USBF	1105
UF0E0L	UF0 EP0 length register	USBF	1083
UF0E0N	UF0 EP0NAK register	USBF	1030
UF0E0NA	UF0 EP0NAKALL register	USBF	1032
UF0E0R	UF0 EP0 read register	USBF	1082
UF0E0SL	UF0 EP0 status register L	USBF	1106
UF0E0ST	UF0 EP0 setup register	USBF	1084
UF0E0W	UF0 EP0 write register	USBF	1096
UF0E1DC1	EP1 DMA control register 1	USBF	1124
UF0E1DC2	EP1 DMA control register 2	USBF	1126
UF0E1IM	UF0 endpoint 1 interface mapping register	USBF	1078
UF0E1SL	UF0 EP1 status register L	USBF	1108
UF0E2DC1	EP2 DMA control register 1	USBF	1124
UF0E2DC2	EP2 DMA control register 2	USBF	1126

(34/34)

Symbol	Name	Unit	Page
UF0INT1	UF0 interrupt 1 register	USBF	1103
UF0IS0	UF0 INT status 0 register	USBF	1045
UF0IS1	UF0 INT status 1 register	USBF	1047
UF0IS2	UF0 INT status 2 register	USBF	1049
UF0IS3	UF0 INT status 3 register	USBF	1050
UF0IS4	UF0 INT status 4 register	USBF	1052
UF0MODC	UF0 mode control register	USBF	1072
UF0MODS	UF0 mode status register	USBF	1073
UF0SDS	UF0 SNDSIE register	USBF	1038
UF0SET	UF0 SET request register	USBF	1040
UFCKMSK	USB function control register	USBF	1009
UFDRQEN	USBF DMA request enable register	USBF	1131
UFIC0	Interrupt control register	INTC	1222
UFIC1	Interrupt control register	INTC	1222
VSWC	System wait control register	CPU	95
WDTE	Watchdog timer enable register	WDT	623
WDTM2	Watchdog timer mode register 2	WDT	1233
WUPIC0	Interrupt control register	INTC	1222

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Ku, Seoul, 135-920, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 3.0