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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at80c51ra2-3csul

Mnemonic	Pin Number			Type	Name And Function
	DIL	LCC	VQFP 1.4		
	12	14	8	I	$\overline{\text{INT0}}$ (P3.2): External interrupt 0
	13	15	9	I	$\overline{\text{INT1}}$ (P3.3): External interrupt 1
	14	16	10	I	T0 (P3.4): Timer 0 external input
	15	17	11	I	T1 (P3.5): Timer 1 external input
	16	18	12	O	$\overline{\text{WR}}$ (P3.6): External data memory write strobe
	17	19	13	O	$\overline{\text{RD}}$ (P3.7): External data memory read strobe
Reset	9	10	4	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC} . If the hardware watchdog reaches its time-out, the reset pin becomes an output during the time the internal reset is activated.
$\overline{\text{ALE/PROG}}$	30	33	27	O (I)	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during EPROM programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
PSEN	29	32	26	O	Program Store Enable: The read strobe to external program memory. When executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
$\overline{\text{EA}}/V_{PP}$	31	35	29	I	External Access Enable/Programming Supply Voltage: $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH (RB) or 7FFFH (RC), or FFFFH (RD). If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (RB) or 7FFFH (RC). $\overline{\text{EA}}$ must be held low for ROMless devices. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming. If security level 1 is programmed, $\overline{\text{EA}}$ will be internally latched on Reset.
XTAL1	19	21	15	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	Crystal 2: Output from the inverting oscillator amplifier

5.1 Pin Description for 64/68 pin Packages

Port 4 and Port 5 are 8-bit bidirectional I/O ports with internal pull-ups. Pins that have 1s written to them are pulled high by the internal pull ups and can be used as inputs.

As inputs, pins that are externally pulled low will source current because of the internal pull-ups.

Refer to the previous pin description for other pins.

Table 5-1. 64/68 Pin Packages Configuration

Pin	PLCC68	SQUARE VQFP64 1.4
VSS	51	9/40
VCC	17	8

Bit Number	Bit Mnemonic	Description
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	X2	CPU and peripheral clock bit Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$).

Reset Value = XXXX XXX0b

Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (<http://www.atmel.com>)

6.3 Programmable Counter Array PCA

The PCA provides more timing capabilities with less CPU intervention than the standard timer/counters. Its advantages include reduced software overhead and improved accuracy. The PCA consists of a dedicated timer/counter which serves as the time base for an array of five compare/capture modules. Its clock input can be programmed to count any one of the following signals:

- Oscillator frequency $\div 12$ ($\div 6$ in X2 mode)
- Oscillator frequency $\div 4$ ($\div 2$ in X2 mode)
- Timer 0 overflow
- External input on ECI (P1.2)

Each compare/capture modules can be programmed in any one of the following modes:

- rising and/or falling edge capture,
- software timer,
- high-speed output, or
- pulse width modulator.

Module 4 can also be programmed as a watchdog timer (See Section "PCA Watchdog Timer", page 33).

When the compare/capture modules are programmed in the capture mode, software timer, or high speed output mode, an interrupt can be generated when the module executes its function. All five modules plus the PCA timer overflow share one interrupt vector.

The PCA timer/counter and compare/capture modules share Port 1 for external I/O. These pins are listed below. If the port is not used for the PCA, it can still be used for standard I/O.

PCA component	External I/O Pin
16-bit Counter	P1.2 / ECI
16-bit Module 0	P1.3 / CEX0
16-bit Module 1	P1.4 / CEX1
16-bit Module 2	P1.5 / CEX2
16-bit Module 3	P1.6 / CEX3
16-bit Module 4	P1.7 / CEX4

The PCA timer is a common time base for all five modules (See Figure 6-4). The timer count source is determined from the CPS1 and CPS0 bits in the **CMOD SFR** (See Table 6-4) and can be programmed to run at:

- 1/12 the oscillator frequency. (Or 1/6 in X2 Mode)
- 1/4 the oscillator frequency. (Or 1/2 in X2 Mode)
- The Timer 0 overflow
- The input on the ECI pin (P1.2)

Figure 6-4. PCA Timer/Counter

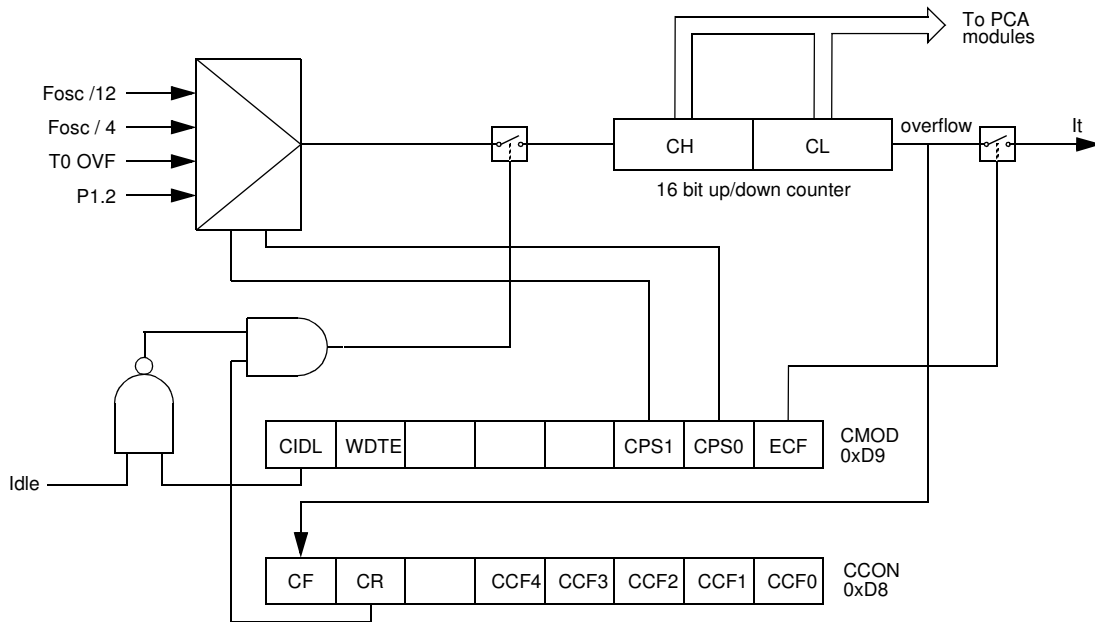


Table 6-4. CMOD: PCA Counter Mode Register

CMOD									
Address 0D9H		CIDL	WDTE	-	-	-	CPS1	CPS0	ECF
Reset value		0	0	X	X	X	0	0	0

Symbol	Function															
CIDL	Counter Idle control: CIDL = 0 programs the PCA Counter to continue functioning during idle Mode. CIDL = 1 programs it to be gated off during idle.															
WDTE	Watchdog Timer Enable: WDTE = 0 disables Watchdog Timer function on PCA Module 4. WDTE = 1 enables it.															
-	Not implemented, reserved for future use. ⁽¹⁾															
CPS1	PCA Count Pulse Select bit 1.															
CPS0	PCA Count Pulse Select bit 0.															
	<table border="1"> <thead> <tr> <th>CPS1</th> <th>CPS0</th> <th>Selected PCA input. ⁽²⁾</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Internal clock $f_{osc}/12$ (Or $f_{osc}/6$ in X2 Mode).</td> </tr> <tr> <td>0</td> <td>1</td> <td>Internal clock $f_{osc}/4$ (Or $f_{osc}/2$ in X2 Mode).</td> </tr> <tr> <td>1</td> <td>0</td> <td>Timer 0 Overflow</td> </tr> <tr> <td>1</td> <td>1</td> <td>External clock at ECI/P1.2 pin (max rate = $f_{osc}/8$)</td> </tr> </tbody> </table>	CPS1	CPS0	Selected PCA input. ⁽²⁾	0	0	Internal clock $f_{osc}/12$ (Or $f_{osc}/6$ in X2 Mode).	0	1	Internal clock $f_{osc}/4$ (Or $f_{osc}/2$ in X2 Mode).	1	0	Timer 0 Overflow	1	1	External clock at ECI/P1.2 pin (max rate = $f_{osc}/8$)
CPS1	CPS0	Selected PCA input. ⁽²⁾														
0	0	Internal clock $f_{osc}/12$ (Or $f_{osc}/6$ in X2 Mode).														
0	1	Internal clock $f_{osc}/4$ (Or $f_{osc}/2$ in X2 Mode).														
1	0	Timer 0 Overflow														
1	1	External clock at ECI/P1.2 pin (max rate = $f_{osc}/8$)														
ECF	PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function of CF.															

1. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.
2. f_{osc} = oscillator frequency

The **CMOD SFR** includes three additional bits associated with the PCA (See Figure 6-4 and Table 6-4).

- The CIDL bit which allows the PCA to stop during idle mode.
- The WDTE bit which enables or disables the watchdog function on module 4.
- The ECF bit which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows.

The **CCON SFR** contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (Refer to Table 6-5).

- Bit CR (CCON.6) must be set by software to run the PCA. The PCA is shut off by clearing this bit.
- Bit CF: The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software.
- Bits 0 through 4 are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software.

Table 6-5. CCON: PCA Counter Control Register

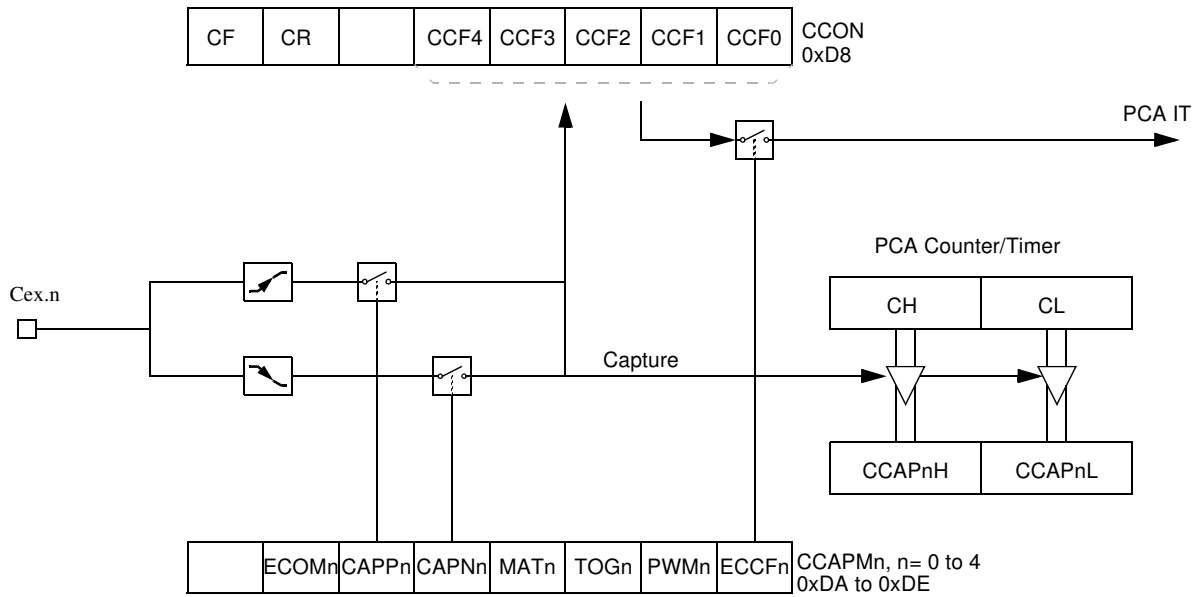
CCON		CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0
Address 0D8H									
Reset value		0	0	X	0	0	0	0	0
Symbol	Function								
CF	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.								
CR	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.								
-	Not implemented, reserved for future use. ⁽¹⁾								
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								

1. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

The **watchdog timer** function is implemented in module 4 (See Figure 6-7).

The **PCA interrupt** system is shown in Figure 6-5.

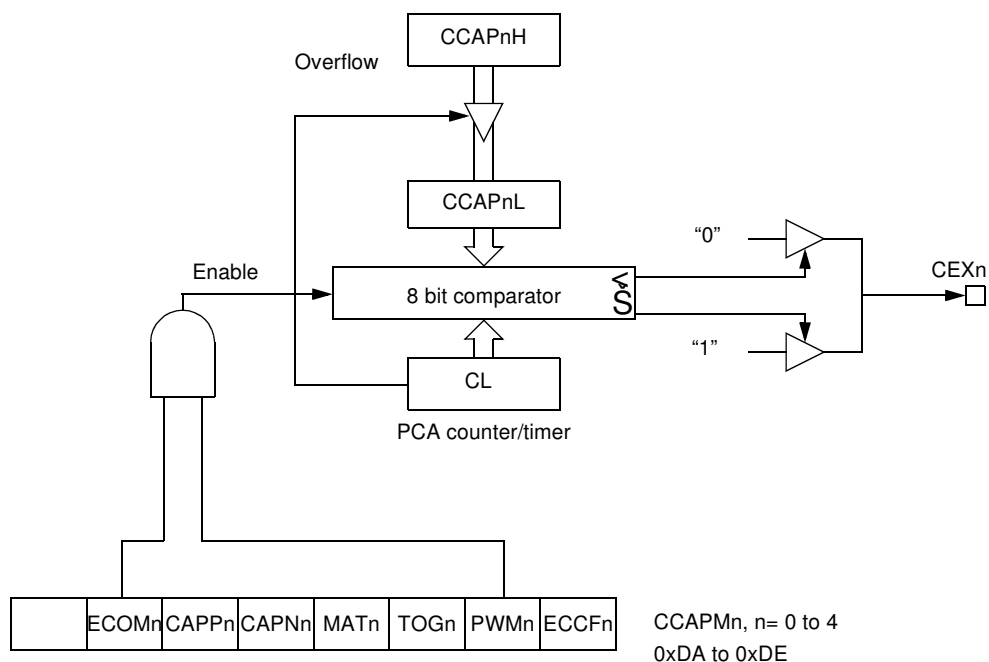
Figure 6-6. PCA Capture Mode



6.3.2 16-bit Software Timer/ Compare Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set (See Figure 6-7).

Figure 6-9. PCA PWM Mode



6.3.5 PCA Watchdog Timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed. Figure 6-7 shows a diagram of how the watchdog works. The user preloads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

- 1. Periodically change the compare value so it will never match the PCA timer,
- 2. periodically change the PCA timer value so it will never match the compare values, or
- 3. Disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for all modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

This watchdog timer won't generate a reset out on the reset pin.

Bit Number	Bit Mnemonic	Description																
7	FE	Framing Error bit (SMOD0=1) Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit																
	SM0	Serial port Mode bit 0 Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit																
6	SM1	Serial port Mode bit 1 <u>SM0 SM1 Mode Description Baud Rate</u> <table border="0"> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Shift Register $F_{XTAL}/12$ (/6 in X2 mode)</td> </tr> <tr> <td>0</td> <td>1</td> <td>18-bit UART</td> <td>Variable</td> </tr> <tr> <td>1</td> <td>0</td> <td>29-bit UART</td> <td>$F_{XTAL}/64$ or $F_{XTAL}/32$ (/32, /16 in X2 mode)</td> </tr> <tr> <td>1</td> <td>1</td> <td>39-bit UART</td> <td>Variable</td> </tr> </table>	0	0	0	Shift Register $F_{XTAL}/12$ (/6 in X2 mode)	0	1	18-bit UART	Variable	1	0	29-bit UART	$F_{XTAL}/64$ or $F_{XTAL}/32$ (/32, /16 in X2 mode)	1	1	39-bit UART	Variable
0	0	0	Shift Register $F_{XTAL}/12$ (/6 in X2 mode)															
0	1	18-bit UART	Variable															
1	0	29-bit UART	$F_{XTAL}/64$ or $F_{XTAL}/32$ (/32, /16 in X2 mode)															
1	1	39-bit UART	Variable															
5	SM2	Serial port Mode 2 bit / Multiprocessor Communication Enable bit Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.																
4	REN	Reception Enable bit Clear to disable serial reception. Set to enable serial reception.																
3	TB8	Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3 Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.																
2	RB8	Receiver Bit 8 / Ninth bit received in modes 2 and 3 Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.																
1	TI	Transmit Interrupt flag Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.																
0	RI	Receive Interrupt flag Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 6-11. and Figure 6-12. in the other modes.																

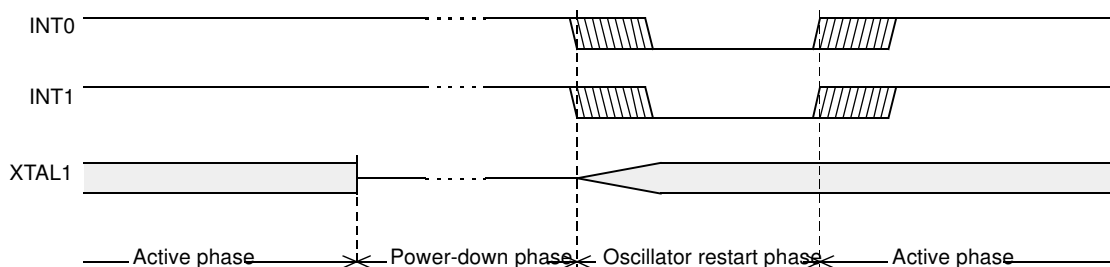
Reset Value = 0000 0000b

Bit addressable

Table 6-15. PCON Register
PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

Figure 6-14. Power-Down Exit Waveform



Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does not affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

Note: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

Table 6-20. The state of ports during idle and power-down mode

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data*	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power-down	Internal	0	0	Port Data*	Port Data	Port Data	Port Data
Power-down	External	0	0	Floating	Port Data	Port Data	Port Data

* Port 0 can force a "zero" level. A "one" will leave port floating.

6.8 Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST-pin.

6.8.1 Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is $96 \times T_{OSC}$, where $T_{OSC} = 1/F_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

To have a more powerful WDT, a 2^7 counter has been added to extend the Time-out capability, ranking from 16ms to 2s @ $F_{OSC} = 12\text{MHz}$. To manage this feature, refer to WDTPRG register description, [Table 6-22](#) (SFR0A7h).

Table 6-21. WDTRST Register
WDTRST Address (0A6h)

	7	6	5	4	3	2	1
Reset value	X	X	X	X	X	X	X

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.

Table 6-22. WDTPRG Register
WDTPRG Address (0A7h)

7	6	5	4	3	2	1	0
T4	T3	T2	T1	T0	S2	S1	S0

7. Power-Off Flag

The power-off flag allows the user to distinguish between a “cold start” reset and a “warm start” reset.

A cold start reset is the one induced by V_{CC} switch-on. A warm start reset occurs while V_{CC} is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See [Table 7-1](#)). POF is set by hardware when V_{CC} rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a V_{cc} range from 4.5V to 5.5V. For lower V_{cc} value, reading POF bit will return indeterminate value.

Table 7-1. PCON Register
PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
Bit Number	Bit Mnemonic	Description					
7	SMOD1	Serial port Mode bit 1 Set to select double baud rate in mode 1, 2 or 3.					
6	SMOD0	Serial port Mode bit 0 Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.					
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
4	POF	Power-Off Flag Clear to recognize next reset type. Set by hardware when V_{CC} rises from 0 to its nominal voltage. Can also be set by software.					
3	GF1	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.					
2	GF0	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.					
1	PD	Power-Down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.					
0	IDL	Idle mode bit Clear by hardware when interrupt or reset occurs. Set to enter idle mode.					

Reset Value = 00X1 0000b

Not bit addressable

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Ambient Temperature Under Bias: C = commercial.....0°C to 70°C I = industrial-40°C to 85°C Storage Temperature -65°C to + 150°C Voltage on V _{CC} to V _{SS}-0.5 V to + 7 V Voltage on Any Pin to V _{SS}-0.5 V to V _{CC} + 0.5 V Power Dissipation 1 W	*NOTICE: Stresses at or above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability. Power dissipation is based on the maximum allowable die temperature and the thermal resistance of the package.
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11.2 Power Consumption Measurement

Since the introduction of the first C51 devices, every manufacturer made operating I_{CC} measurements under reset, which made sense for the designs where the CPU was running under reset. In Atmel new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That's why, while keeping measurements under Reset, Atmel presents a new way to measure the operating I_{CC}:

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = V_{CC}, RST = V_{SS}, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating I_{CC}.

11.3 DC Parameters for Standard Voltage

T_A = 0°C to +70°C; V_{SS} = 0 V; V_{CC} = 5 V ± 10%; F = 0 to 40 MHz.

T_A = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 5 V ± 10%; F = 0 to 40 MHz.

Table 11-1. DC Parameters in Standard Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Input Low Voltage	-0.5		0.2 V _{CC} - 0.1	V	
V _{IH}	Input High Voltage except XTAL1, RST	0.2 V _{CC} + 0.9		V _{CC} + 0.5	V	
V _{IH1}	Input High Voltage, XTAL1, RST	0.7 V _{CC}		V _{CC} + 0.5	V	
V _{OL}	Output Low Voltage, ports 1, 2, 3, 4, 5 ⁽⁶⁾			0.3	V	I _{OL} = 100 μA ⁽⁴⁾
				0.45	V	I _{OL} = 1.6 mA ⁽⁴⁾
				1.0	V	I _{OL} = 3.5 mA ⁽⁴⁾
V _{OL1}	Output Low Voltage, port 0 ⁽⁶⁾			0.3	V	I _{OL} = 200 μA ⁽⁴⁾
				0.45	V	I _{OL} = 3.2 mA ⁽⁴⁾
				1.0	V	I _{OL} = 7.0 mA ⁽⁴⁾
V _{OL2}	Output Low Voltage, ALE, $\overline{\text{PSEN}}$			0.3	V	I _{OL} = 100 μA ⁽⁴⁾
				0.45	V	I _{OL} = 1.6 mA ⁽⁴⁾
				1.0	V	I _{OL} = 3.5 mA ⁽⁴⁾

11.4 DC Parameters for Low Voltage

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{SS} = 0\text{ V}$; $V_{CC} = 2.7\text{ V}$ to $5.5\text{ V} \pm 10\%$; $F = 0$ to 30 MHz .

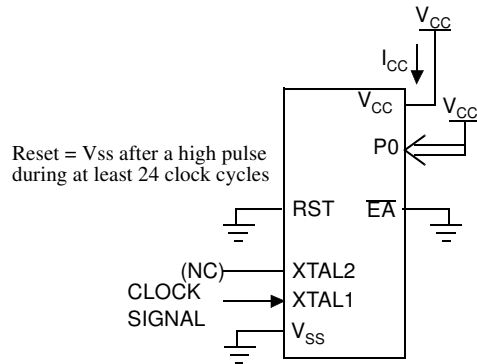
$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; $V_{SS} = 0\text{ V}$; $V_{CC} = 2.7\text{ V}$ to $5.5\text{ V} \pm 10\%$; $F = 0$ to 30 MHz .

Table 11-2. DC Parameters for Low Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		$0.2 V_{CC} - 0.1$	V	
V_{IH}	Input High Voltage except XTAL1, RST	$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage, XTAL1, RST	$0.7 V_{CC}$		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage, ports 1, 2, 3, 4, 5 ⁽⁶⁾			0.45	V	$I_{OL} = 0.8\text{ mA}$ ⁽⁴⁾
V_{OL1}	Output Low Voltage, port 0, ALE, $\overline{\text{PSEN}}$ ⁽⁶⁾			0.45	V	$I_{OL} = 1.6\text{ mA}$ ⁽⁴⁾
V_{OH}	Output High Voltage, ports 1, 2, 3, 4, 5	$0.9 V_{CC}$			V	$I_{OH} = -10\ \mu\text{A}$
V_{OH1}	Output High Voltage, port 0, ALE, $\overline{\text{PSEN}}$	$0.9 V_{CC}$			V	$I_{OH} = -40\ \mu\text{A}$
I_{IL}	Logical 0 Input Current ports 1, 2, 3, 4, 5			-50	μA	$V_{in} = 0.45\text{ V}$
I_{LI}	Input Leakage Current			± 10	μA	$0.45\text{ V} < V_{in} < V_{CC}$
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3, 4, 5			-650	μA	$V_{in} = 2.0\text{ V}$
R_{RST}	RST Pulldown Resistor	50	90 ⁽⁵⁾	200	k Ω	
CIO	Capacitance of I/O Buffer			10	pF	$F_c = 1\text{ MHz}$ $T_A = 25^\circ\text{C}$
I_{PD}	Power-down Current		20 ⁽⁵⁾ 10 ⁽⁵⁾	50 30	μA	$V_{CC} = 2.0\text{ V}$ to 5.5 V ⁽³⁾ $V_{CC} = 2.0\text{ V}$ to 3.3 V ⁽³⁾
I_{PD}	Power-down Current (Only for TS87C51RD2 S287-xxx Very Low power)		2 ⁽⁵⁾	15	μA	$2.0\text{ V} < V_{CC} < 3.6\text{ V}$ ⁽³⁾
I_{CC} under RESET	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			1 + 0.2 Freq (MHz) @12MHz 3.4 @16MHz 4.2	mA	$V_{CC} = 3.3\text{ V}$ ⁽¹⁾
I_{CC} operating	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			1 + 0.3 Freq (MHz) @12MHz 4.6 @16MHz 5.8	mA	$V_{CC} = 3.3\text{ V}$ ⁽⁸⁾
I_{CC} idle	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			0.15 Freq (MHz) + 0.2 @12MHz 2 @16MHz 2.6	mA	$V_{CC} = 3.3\text{ V}$ ⁽²⁾

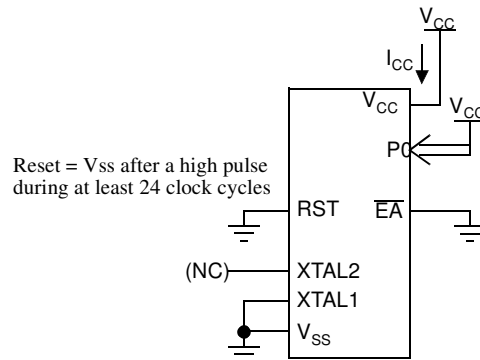
- Notes: 1. I_{CC} under reset is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5\text{ ns}$ (see Figure 11-5.), $V_{IL} = V_{SS} + 0.5\text{ V}$, $V_{IH} = V_{CC} - 0.5\text{ V}$; XTAL2 N.C.; $\overline{\text{EA}} = \text{RST} = \text{Port 0} = V_{CC}$. I_{CC} would be slightly higher if a crystal oscillator used..
2. Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5\text{ ns}$, $V_{IL} = V_{SS} + 0.5\text{ V}$, $V_{IH} = V_{CC} - 0.5\text{ V}$; XTAL2 N.C.; Port 0 = V_{CC} ; EA = RST = V_{SS} (see Figure 11-3.).
3. Power-down I_{CC} is measured with all output pins disconnected; $\overline{\text{EA}} = V_{SS}$, PORT 0 = V_{CC} ; XTAL2 NC.; RST = V_{SS} (see Figure 11-4.).

Figure 11-3. I_{CC} Test Condition, Idle Mode



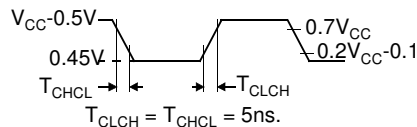
All other pins are disconnected.

Figure 11-4. I_{CC} Test Condition, Power-Down Mode



All other pins are disconnected.

Figure 11-5. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes



11.5 AC Parameters

11.5.1 Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example: T_{AVLL} = Time for Address Valid to ALE Low.

T_{LLPL} = Time for ALE Low to \overline{PSEN} Low.

T_A = 0 to +70°C (commercial temperature range); V_{SS} = 0 V; V_{CC} = 5 V \pm 10%; -M and -V ranges.
 T_A = -40°C to +85°C (industrial temperature range); V_{SS} = 0 V; V_{CC} = 5 V \pm 10%; -M and -V ranges.

$T_A = 0$ to $+70^\circ\text{C}$ (commercial temperature range); $V_{SS} = 0$ V; 2.7 V $< V_{CC} < 5.5$ V; -L range.
 $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (industrial temperature range); $V_{SS} = 0$ V; 2.7 V $< V_{CC} < 5.5$ V; -L range.

Table 11-3. gives the maximum applicable load capacitance for Port 0, Port 1, 2 and 3, and ALE and $\overline{\text{PSEN}}$ signals. Timings will be guaranteed if these capacitances are respected. Higher capacitance values can be used, but timings will then be degraded.

Table 11-3. Load Capacitance versus speed range, in pF

	-M	-V	-L
Port 0	100	50	100
Port 1, 2, 3	80	50	80
ALE / $\overline{\text{PSEN}}$	100	30	100

Table 11-5., Table 39. and Table 42. give the description of each AC symbols.

Table 11-6., Table 11-8. and Table 11-10. give for each range the AC parameter.

Table 11-7., Table 11-9. and Table 11-11. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

Table 11-4. Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20	40	30	30	20
T (ns)	25	50	25	33.3	33.3	50

Example:

T_{LLIV} in X2 mode for a -V part at 20 MHz ($T = 1/20^{\text{E}6} = 50$ ns):

$$x = 22 \text{ (Table 11-7.)}$$

$$T = 50\text{ns}$$

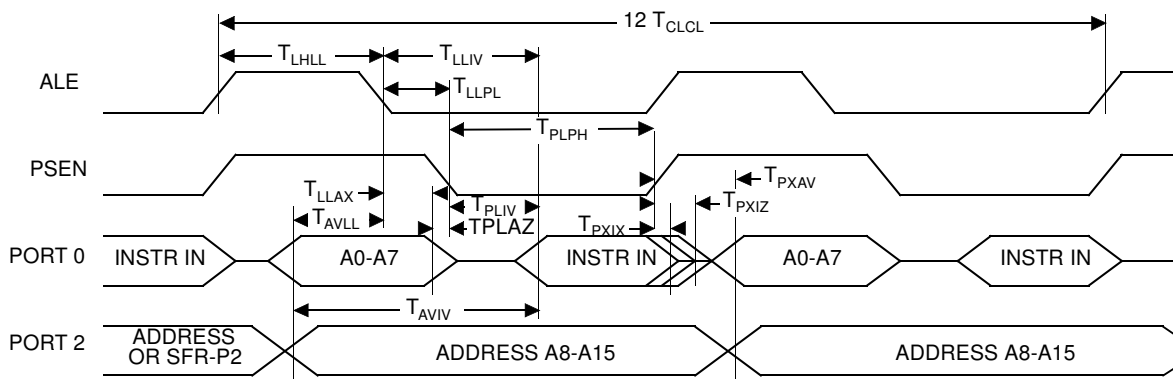
$$T_{LLIV} = 2T - x = 2 \times 50 - 22 = 78\text{ns}$$

Table 11-7. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{LHLL}	Min	$2 T - x$	$T - x$	10	8	15	ns
T_{AVLL}	Min	$T - x$	$0.5 T - x$	15	13	20	ns
T_{LLAX}	Min	$T - x$	$0.5 T - x$	15	13	20	ns
T_{LLIV}	Max	$4 T - x$	$2 T - x$	30	22	35	ns
T_{LLPL}	Min	$T - x$	$0.5 T - x$	10	8	15	ns
T_{PLPH}	Min	$3 T - x$	$1.5 T - x$	20	15	25	ns
T_{PLIV}	Max	$3 T - x$	$1.5 T - x$	40	25	45	ns
T_{PXIX}	Min	x	x	0	0	0	ns
T_{PXIZ}	Max	$T - x$	$0.5 T - x$	7	5	15	ns
T_{AVIV}	Max	$5 T - x$	$2.5 T - x$	40	30	45	ns
T_{PLAZ}	Max	x	x	10	10	10	ns

11.5.3 External Program Memory Read Cycle

Figure 11-6. External Program Memory Read Cycle



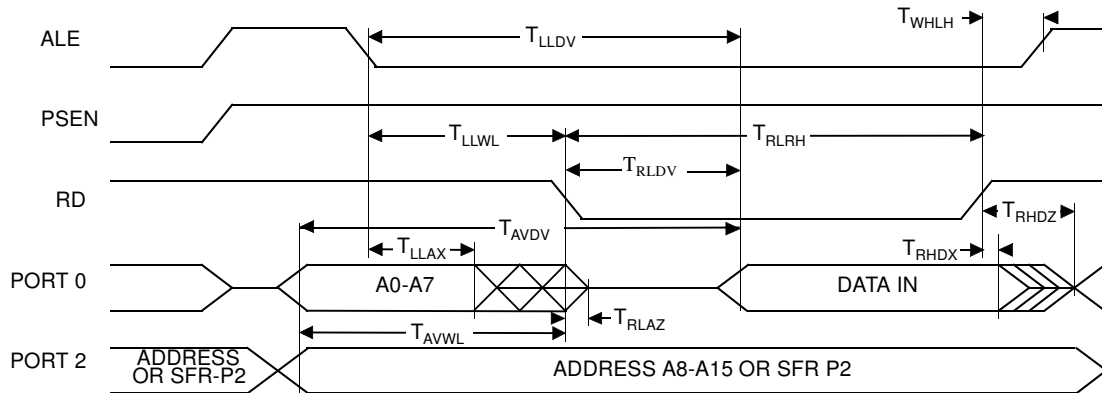
11.5.4 External Data Memory Characteristics

Symbol	Parameter
T_{RLRH}	\overline{RD} Pulse Width
T_{WLWH}	\overline{WR} Pulse Width
T_{RLDV}	\overline{RD} to Valid Data In
T_{RHDX}	Data Hold After \overline{RD}
T_{RHDZ}	Data Float After \overline{RD}
T_{LLDV}	ALE to Valid Data In
T_{AVDV}	Address to Valid Data In
T_{LLWL}	ALE to \overline{WR} or \overline{RD}
T_{AVWL}	Address to \overline{WR} or \overline{RD}
T_{QVWX}	Data Valid to \overline{WR} Transition
T_{QVWH}	Data set-up to \overline{WR} High
T_{WHQX}	Data Hold After \overline{WR}
T_{RLAZ}	\overline{RD} Low to Address Float
T_{WHLH}	\overline{RD} or \overline{WR} High to ALE high

Table 11-8. AC Parameters for a Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T_{RLRH}	130		85		135		125		175		ns
T_{WLWH}	130		85		135		125		175		ns
T_{RLDV}		100		60		102		95		137	ns
T_{RHDX}	0		0		0		0		0		ns
T_{RHDZ}		30		18		35		25		42	ns
T_{LLDV}		160		98		165		155		222	ns
T_{AVDV}		165		100		175		160		235	ns
T_{LLWL}	50	100	30	70	55	95	45	105	70	130	ns
T_{AVWL}	75		47		80		70		103		ns
T_{QVWX}	10		7		15		5		13		ns
T_{QVWH}	160		107		165		155		213		ns
T_{WHQX}	15		9		17		10		18		ns
T_{RLAZ}		0		0		0		0		0	ns
T_{WHLH}	10	40	7	27	15	35	5	45	13	53	ns

Figure 11-8. External Data Memory Read Cycle



11.5.7 Serial Port Timing - Shift Register Mode

Symbol	Parameter
T_{XLXL}	Serial port clock cycle time
T_{QVHX}	Output data set-up to clock rising edge
T_{XHQX}	Output data hold after clock rising edge
T_{XHDX}	Input data hold after clock rising edge
T_{XHDV}	Clock rising edge to input data valid

Table 11-10. AC Parameters for a Fix Clock

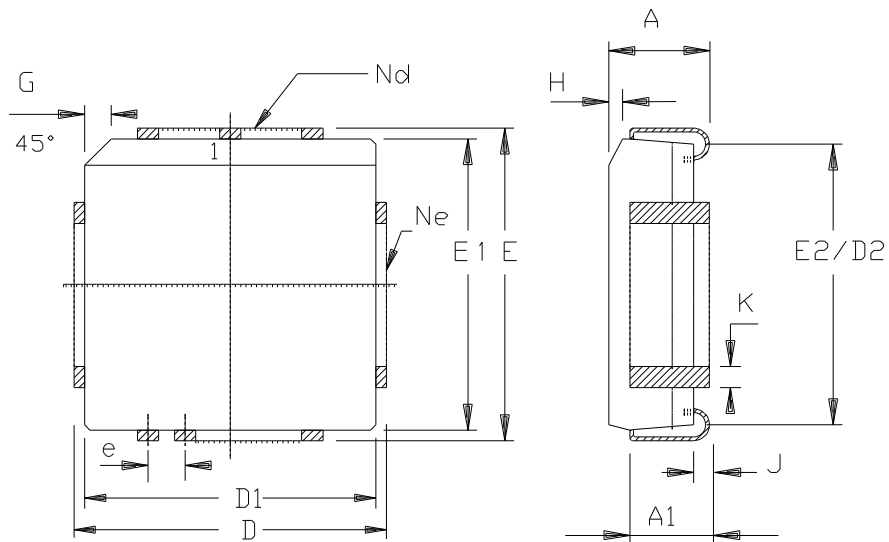
Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T_{XLXL}	300		200		300		300		400		ns
T_{QVHX}	200		117		200		200		283		ns
T_{XHQX}	30		13		30		30		47		ns
T_{XHDX}	0		0		0		0		0		ns
T_{XHDV}		117		34		117		117		200	ns

Part Number	Memory size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS83C51RC2-MCA						
TS83C51RC2-MCB						
TS83C51RC2-MCE						
TS83C51RC2-MIA						
TS83C51RC2-MIB						
TS83C51RC2-MIE						
TS83C51RC2-LCA						
TS83C51RC2-LCB						
TS83C51RC2-LCE						
TS83C51RC2-LIA						
TS83C51RC2-LIB						
TS83C51RC2-LIE						
TS83C51RC2-VCA						
TS83C51RC2-VCB						
TS83C51RC2-VCE						
TS83C51RC2-VIA						
TS83C51RC2-VIB						
TS83C51RC2-VIE						
OBSOLETE						
AT83C51RC2-3CSUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PDIL40	Stick
AT83C51RC2-SLSUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PLCC44	Stick
AT83C51RC2-RLTUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	VQFP44	Tray
AT83C51RC2-3CSUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PDIL40	Stick
AT83C51RC2-SLSUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PLCC44	Stick
AT83C51RC2-RLTUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	VQFP44	Tray



13. Package Drawings

13.1 PLCC44



	MM		INCH	
A	4.20	4.57	.165	.180
A1	2.29	3.04	.090	.120
D	17.40	17.65	.685	.695
D1	16.44	16.66	.647	.656
D2	14.99	16.00	.590	.630
E	17.40	17.65	.685	.695
E1	16.44	16.66	.647	.656
E2	14.99	16.00	.590	.630
e	1.27	BSC	.050	BSC
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	-	.020	-
K	0.33	0.53	.013	.021
Nd	11		11	
Ne	11		11	
PKG STD	00			