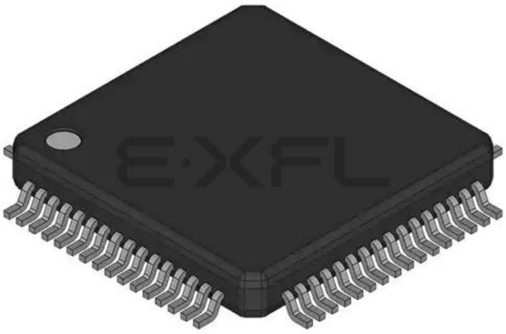
Atmel - AT80C51RA2-RLRUL Datasheet



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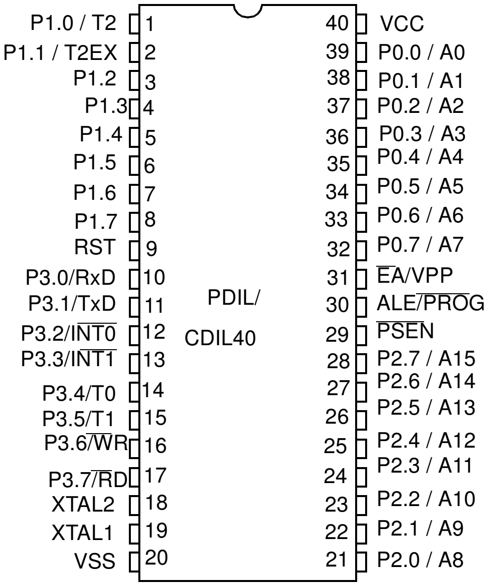
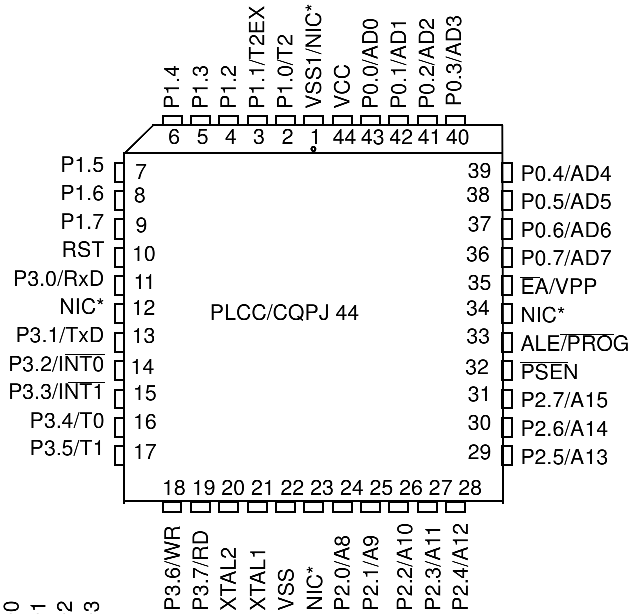
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

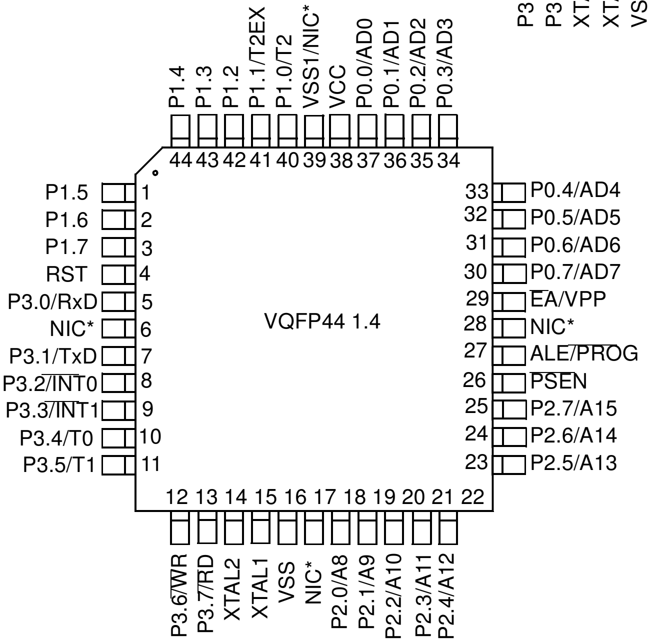
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-VQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at80c51ra2-rlrul

5. Pin Configuration







*NIC: No Internal Connection

P0.0	15	6
P0.1	14	5
P0.2	12	3
P0.3	11	2
P0.4	9	64
P0.5	6	61
P0.6	5	60
P0.7	3	59
P1.0	19	10
P1.1	21	12
P1.2	22	13
P1.3	23	14
P1.4	25	16
P1.5	27	18
P1.6	28	19
P1.7	29	20
P2.0	54	43
P2.1	55	44
P2.2	56	45
P2.3	58	47
P2.4	59	48
P2.5	61	50
P2.6	64	53
P2.7	65	54
P3.0	34	25
P3.1	39	28

Pin	PLCC68	SQUARE VQFP64 1.4
P3.2	40	29
P3.3	41	30
P3.4	42	31
P3.5	43	32
P3.6	45	34
P3.7	47	36
RESET	30	21
ALE/$\overline{\text{PROG}}$	68	56

Bit Number	Bit Mnemonic	Description
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	X2	**CPU and peripheral clock bit** Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$).

Reset Value = XXXX XXX0b

Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (http://www.atmel.com)

6.1 Expanded RAM (XRAM)

The TS80C51Rx2 provide additional Bytes of ramdom access memory (RAM) space for increased data parameter handling and high level language usage.

RA2, RB2 and RC2 devices have 256 bytes of expanded RAM, from 00H to FFH in external data space; RD2 devices have 768 bytes of expanded RAM, from 00H to 2FFH in external data space.

The TS80C51Rx2 has internal data memory that is mapped into four separate segments.

The four segments are:

- 1. The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
- 2. The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
- 3. The Special Function Registers, SFRs, (addresses 80H to FFH) are directly addressable only.
- 4. The expanded RAM bytes are indirectly accessed by MOVX instructions, and with the EXTRAM bit cleared in the AUXR register. (See Table 6-1.)

The Lower 128 bytes can be accessed by either direct or indirect addressing. The Upper 128 bytes can be accessed by indirect addressing only. The Upper 128 bytes occupy the same address space as the SFR. That means they have the same address, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of data RAM or to SFR space by the addressing mode used in the instruction.

- Instructions that use direct addressing access SFR space. **For example: MOV 0A0H, # data**, accesses the SFR at location 0A0H (which is P2).
- Instructions that use indirect addressing access the Upper 128 bytes of data RAM. **For example: MOV @R0, # data** where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).
- The 256 or 768 XRAM bytes can be accessed by indirect addressing, with EXTRAM bit cleared and MOVX instructions. This part of memory which is physically located on-chip, logically occupies the first 256 or 768 bytes of external data memory.
- With EXTRAM = 0, the XRAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. **An access to XRAM will not affect ports P0, P2, P3.6 ($\overline{\text{WR}}$) and P3.7 ($\overline{\text{RD}}$). For example, with EXTRAM = 0, MOVX @R0, # data** where R0 contains 0A0H, accesses the XRAM at address 0A0H rather than external memory. An access to external data memory locations higher than FFH (i.e. 0100H to FFFFH) (higher than 2FFH (i.e. 0300H to FFFFH for RD devices) will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51, so with P0 and P2 as data/address busses, and P3.6 and P3.7 as write and read timing signals. Refer to Figure 6-1. For RD devices, accesses to expanded RAM from 100H to 2FFH can only be done thanks to the use of DPTR.
- With EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 80C51. MOVX @ Ri will provide an eight-bit address multiplexed with data on Port0 and any output port pins can be used to output higher order address bits. This is to provide the external paging capability. MOVX @DPTR will generate a sixteen-bit address. Port2 outputs the high-order eight address bits (the contents of DPH) while Port0 multiplexes the low-order eight

address bits (DPL) with data. MOVX @ Ri and MOVX @DPTR will generate either read or write signals on P3.6 ($\overline{WR}$) and P3.7 ($\overline{RD}$).

The stack pointer (SP) may be located anywhere in the 256 bytes RAM (lower and upper RAM) internal data memory. The stack may not be located in the XRAM.

Figure 6-1. Internal and External Data Memory Address

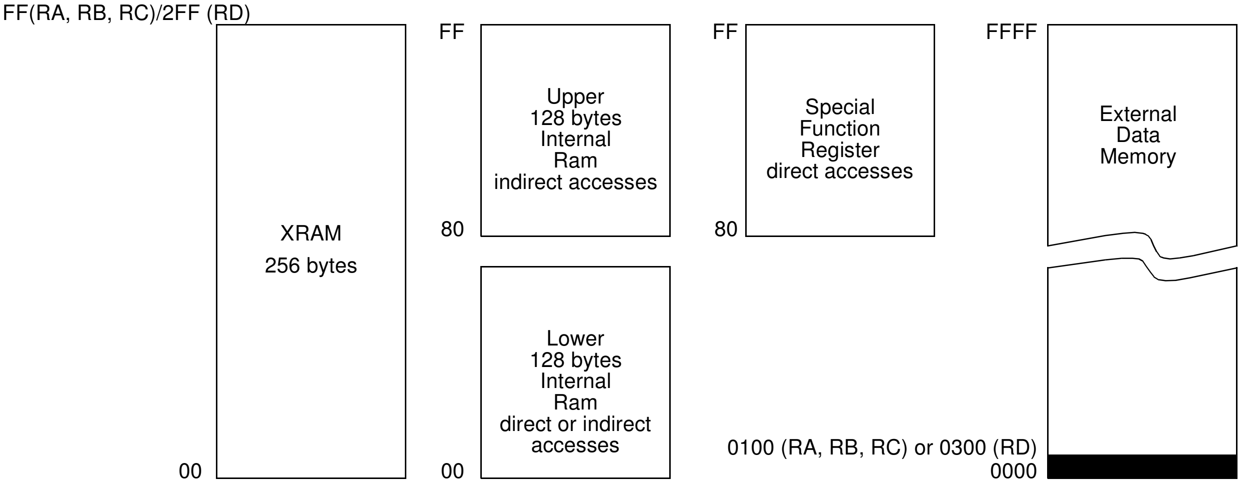


Table 6-1. Auxiliary Register AUXR

AUXR Address 08EH	-	-	-	-	-	-	EXTRAM	AO
Reset value	X	X	X	X	X	X	0	0

<table>
<tr><th>Symbol</th><th colspan="2">Function</th></tr>
<tr><td>-</td><td colspan="2">Not implemented, reserved for future use. (1)</td></tr>
<tr><td rowspan="4">AO</td><td colspan="2">Disable/Enable ALE</td></tr>
<tr><td>AO</td><td>Operating Mode</td></tr>
<tr><td>0</td><td>ALE is emitted at a constant rate of 1/6 the oscillator frequency (or 1/3 if X2 mode is used)</td></tr>
<tr><td>1</td><td>ALE is active only during a MOVX or MOVC instruction</td></tr>
<tr><td rowspan="4">EXTRAM</td><td colspan="2">Internal/External RAM (00H-FFH) access using MOVX @ Ri/ @ DPTR</td></tr>
<tr><td>EXTRAM</td><td>Operating Mode</td></tr>
<tr><td>0</td><td>Internal XRAM access using MOVX @ Ri/ @ DPTR</td></tr>
<tr><td>1</td><td>External data memory access</td></tr>
</table>

1. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

6.2 Timer 2

The timer 2 in the TS80C51RX2 is compatible with the timer 2 in the 80C52.
It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 6-2) and T2MOD register (See Table 6-3). Timer 2 operation is similar to Timer 0 and Timer 1. $C/\overline{T2}$ selects $F_{OSC}/12$ (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and $CP/\overline{RL2}$ (T2CON), as described in the Atmel 8-bit Microcontroller Hardware description.

Refer to the Atmel 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C51RX2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

6.2.1 Auto-reload Mode

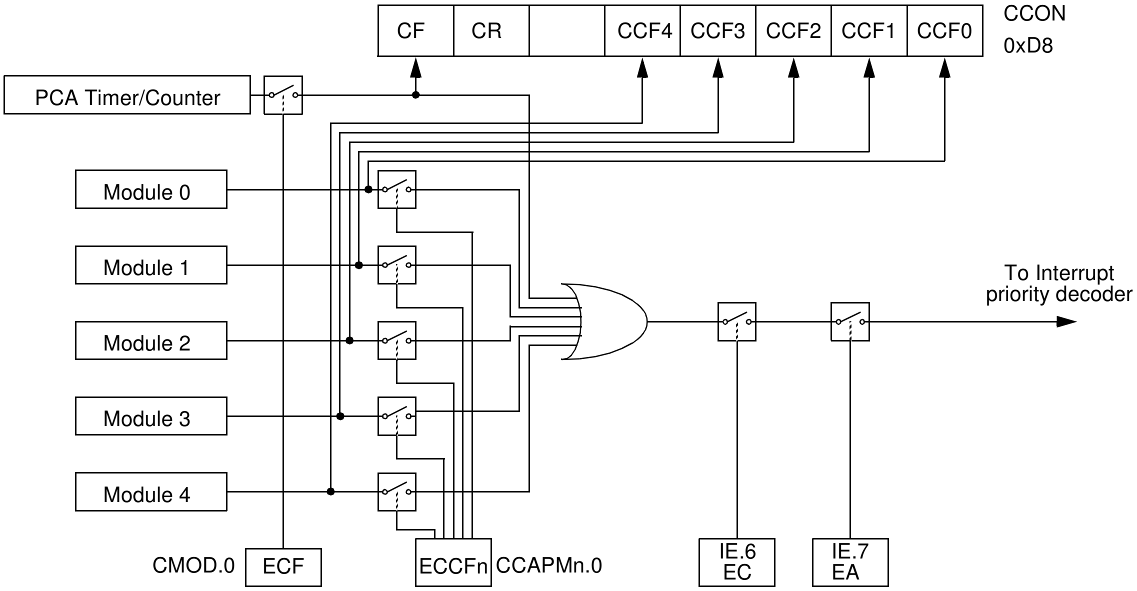
The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 6-2. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.

Figure 6-5. PCA Interrupt System



PCA Modules: each one of the five compare/capture modules has six possible functions. It can perform:

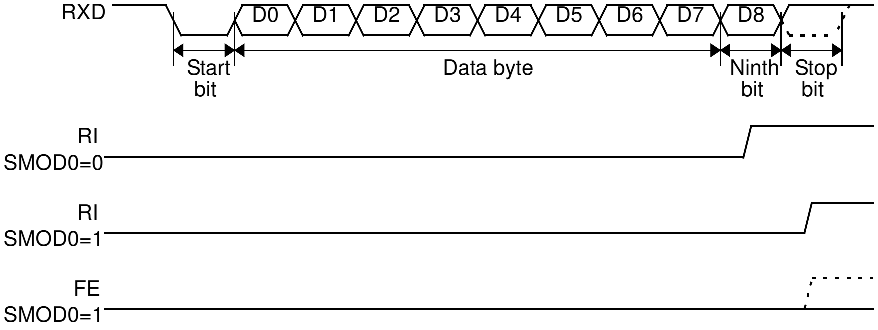
- 16-bit Capture, positive-edge triggered,
- 16-bit Capture, negative-edge triggered,
- 16-bit Capture, both positive and negative-edge triggered,
- 16-bit Software Timer,
- 16-bit High Speed Output,
- 8-bit Pulse Width Modulator.

In addition, module 4 can be used as a Watchdog Timer.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (See Table 6-6). The registers contain the bits that control the mode that each module will operate in.

- The ECCF bit (CCAPMn.0 where n=0, 1, 2, 3, or 4 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module.
- PWM (CCAPMn.1) enables the pulse width modulation mode.
- The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register.
- The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.
- The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition.

Figure 6-12. UART Timings in Modes 2 and 3



6.4.2 Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

Note: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

6.4.3 Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be `1111 1111b`.

For example:

```
SADDR0101 0110b
SADEN1111 1100b
Given0101 01XXb
```

The following is an example of how to use given addresses to address different slaves:

```
Slave A:SADDR1111 0001b
        SADEN1111 1010b
        Given1111 0X0Xb

Slave B:SADDR1111 0011b
        SADEN1111 1001b
        Given1111 0XX1b
```

```
Slave C:SADDR1111 0010b
    SADEN1111 1101b
    Given1111 00X1b
```

The SADEN byte is selected so that each slave may be addressed separately.
For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. `1111 0000b`).

For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. `1111 0011b`).

To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. `1111 0001b`).

6.4.4 Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

```
    SADDR0101 0110b
    SADEN1111 1100b
  Broadcast =SADDR OR SADEN1111 111Xb
```

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

```
Slave A:SADDR1111 0001b
    SADEN1111 1010b
    Broadcast1111 1X11b,

Slave B:SADDR1111 0011b
    SADEN1111 1001b
    Broadcast1111 1X11B,

Slave C:SADDR=1111 0010b
    SADEN1111 1101b
    Broadcast1111 1111b
```

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.

6.4.5 Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are `XXXX XXXXb` (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

Table 6-12. SADEN - Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 6-13. SADDR - Slave Address Register (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 6-14. SCON Register
SCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Table 6-19. IPH Register
IPH - Interrupt Priority High Register (B7h)

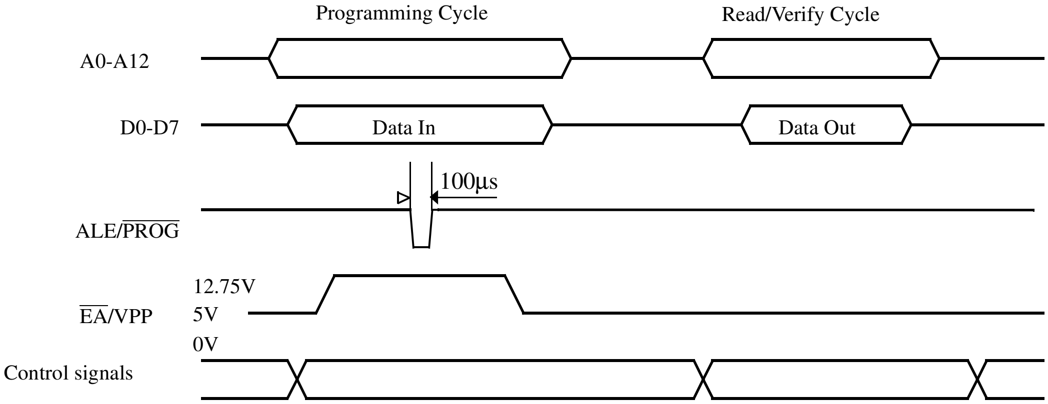
7	6	5	4	3	2	1	0
-	**PPCH**	**PT2H**	**PSH**	**PT1H**	**PX1H**	**PT0H**	**PX0H**

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	PPCH	PCA interrupt priority bit high. PPCHPPC Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
5	PT2H	Timer 2 overflow interrupt Priority High bit PT2H PT2 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
4	PSH	Serial port Priority High bit PSH PS Priority Level 0 0Lowest 0 1 1 0 1 1Highest
3	PT1H	Timer 1 overflow interrupt Priority High bit PT1H PT1Priority Level 0 0Lowest 0 1 1 0 1 1Highest
2	PX1H	External interrupt 1 Priority High bit PX1HPX1Priority Level 0 0Lowest 0 1 1 0 1 1Highest
1	PT0H	Timer 0 overflow interrupt Priority High bit PT0H PT0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
0	PX0H	External interrupt 0 Priority High bit PX0HPX0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest

Reset Value = X000 0000b
Not bit addressable

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.

Figure 9-2. Programming and Verification Signal's Waveform



9.4 EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

9.4.1 Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 µW/cm^2 rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

10. Signature Bytes

The TS83/87C51RB2/RC2/RD2 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 31. for Read Signature Bytes. Table 10-1. shows the content of the signature byte for the TS87C51RB2/RC2/RD2.

Table 10-1. Signature Bytes Content

Location	Contents	Comment
30h	58h	Manufacturer Code: Atmel
31h	57h	Family Code: C51 X2
60h	7Ch	Product name: TS83C51RD2

11.4 DC Parameters for Low Voltage

$T_A = 0°C$ to $+70°C$; $V_{SS} = 0$ V; $V_{CC} = 2.7$ V to 5.5 V ± 10%; F = 0 to 30 MHz.
$T_A = -40°C$ to $+85°C$; $V_{SS} = 0$ V; $V_{CC} = 2.7$ V to 5.5 V ± 10%; F = 0 to 30 MHz.

Table 11-2. DC Parameters for Low Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		$0.2\ V_{CC} - 0.1$	V	
V_{IH}	Input High Voltage except XTAL1, RST	$0.2\ V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage, XTAL1, RST	$0.7\ V_{CC}$		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage, ports 1, 2, 3, 4, 5 (6)			0.45	V	$I_{OL} = 0.8$ mA(4)
V_{OL1}	Output Low Voltage, port 0, ALE, $\overline{PSEN}$ (6)			0.45	V	$I_{OL} = 1.6$ mA(4)
V_{OH}	Output High Voltage, ports 1, 2, 3, 4, 5	$0.9\ V_{CC}$			V	$I_{OH} = -10$ µA
V_{OH1}	Output High Voltage, port 0, ALE, $\overline{PSEN}$	$0.9\ V_{CC}$			V	$I_{OH} = -40$ µA
I_{IL}	Logical 0 Input Current ports 1, 2, 3, 4, 5			-50	µA	Vin = 0.45 V
I_{LI}	Input Leakage Current			±10	µA	0.45 V < Vin < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3, 4, 5			-650	µA	Vin = 2.0 V
R_{RST}	RST Pulldown Resistor	50	90 (5)	200	kΩ	
CIO	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz $T_A = 25°C$
I_{PD}	Power-down Current		20 (5) 10 (5)	50 30	µA	$V_{CC} = 2.0$ V to 5.5 V(3) $V_{CC} = 2.0$ V to 3.3 V(3)
I_{PD}	Power-down Current (Only for TS87C51RD2 S287-xxx Very Low power)		2 (5)	15	µA	2.0 V < V_{CC} < 3.6 V(3)
I_{CC} under RESET	Power Supply Current Maximum values, X1 mode: (7)			1 + 0.2 Freq (MHz) @12MHz 3.4 @16MHz 4.2	mA	$V_{CC} = 3.3$ V(1)
I_{CC} operating	Power Supply Current Maximum values, X1 mode: (7)			1 + 0.3 Freq (MHz) @12MHz 4.6 @16MHz 5.8	mA	$V_{CC} = 3.3$ V(8)
I_{CC} idle	Power Supply Current Maximum values, X1 mode: (7)			0.15 Freq (MHz) + 0.2 @12MHz 2 @16MHz 2.6	mA	$V_{CC} = 3.3$ V(2)

Notes:
1. I_{CC} under reset is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, $T_{CHCL} = 5$ ns (see Figure 11-5.), $V_{IL} = V_{SS} + 0.5$ V,
$V_{IH} = V_{CC} - 0.5$V; XTAL2 N.C.; $\overline{EA}$ = RST = Port 0 = V_{CC}. I_{CC} would be slightly higher if a crystal oscillator used..
2. Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, $T_{CHCL} = 5$ ns, $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V; XTAL2 N.C; Port 0 = V_{CC}; $\overline{EA}$ = RST = V_{SS} (see Figure 11-3.).
3. Power-down I_{CC} is measured with all output pins disconnected; $\overline{EA} = V_{SS}$, PORT 0 = V_{CC}; XTAL2 NC.; RST = V_{SS} (see Figure 11-4.).

11.5.9 EPROM Programming and Verification Characteristics

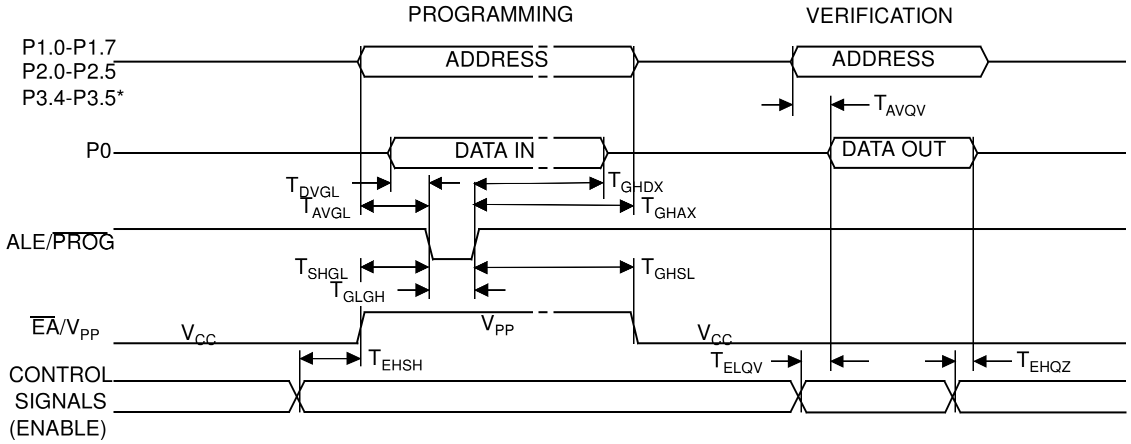
T_A = 21°C to 27°C; V_{SS} = 0V; V_{CC} = 5V ± 10% while programming. V_{CC} = operating range while

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13	V
I_{PP}	Programming Supply Current		75	mA
$1/T_{CLCL}$	Oscillator Frquency	4	6	MHz
T_{AVGL}	Address Setup to $\overline{\text{PROG}}$ Low	48 T_{CLCL}		
T_{GHAX}	Adress Hold after $\overline{\text{PROG}}$	48 T_{CLCL}		
T_{DVGL}	Data Setup to $\overline{\text{PROG}}$ Low	48 T_{CLCL}		
T_{GHDX}	Data Hold after $\overline{\text{PROG}}$	48 T_{CLCL}		
T_{EHSH}	(Enable) High to V_{PP}	48 T_{CLCL}		
T_{SHGL}	V_{PP} Setup to $\overline{\text{PROG}}$ Low	10		µs
T_{GHSL}	V_{PP} Hold after $\overline{\text{PROG}}$	10		µs
T_{GLGH}	$\overline{\text{PROG}}$ Width	90	110	µs
T_{AVQV}	Address to Valid Data		48 T_{CLCL}	
T_{ELQV}	ENABLE Low to Data Valid		48 T_{CLCL}	
T_{EHQZ}	Data Float after ENABLE	0	48 T_{CLCL}	

verifying

11.5.10 EPROM Programming and Verification Waveforms

Figure 11-10. EPROM Programming and Verification Waveforms



* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

11.5.11 External Clock Drive Characteristics (XTAL1)

Symbol	Parameter	Min	Max	Units
T_{CLCL}	Oscillator Period	25		ns
T_{CHCX}	High Time	5		ns
T_{CLCX}	Low Time	5		ns
T_{CLCH}	Rise Time		5	ns
T_{CHCL}	Fall Time		5	ns
T_{CHCX}/T_{CLCX}	Cyclic ratio in X2 mode	40	60	%

11.5.12 External Clock Drive Waveforms

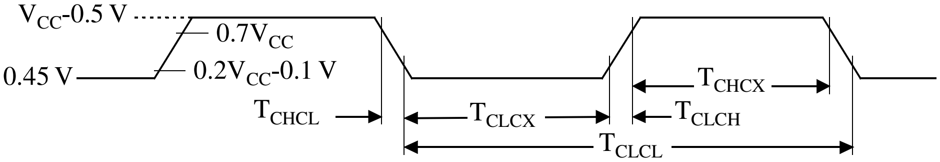


Figure 11-11. External Clock Drive Waveforms

11.5.13 AC Testing Input/Output Waveforms

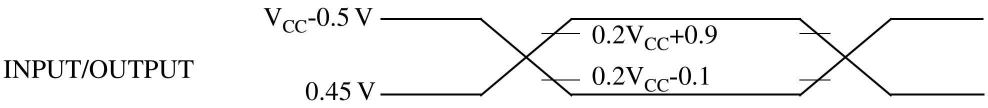


Figure 11-12. AC Testing Input/Output Waveforms

AC inputs during testing are driven at V_{CC} - 0.5 for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at V_{IH} min for a logic “1” and V_{IL} max for a logic “0”.

11.5.14 Float Waveforms

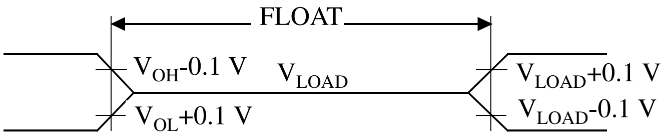


Figure 11-13. Float Waveforms

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. I_{OL}/I_{OH} $\geq \pm$ 20mA.

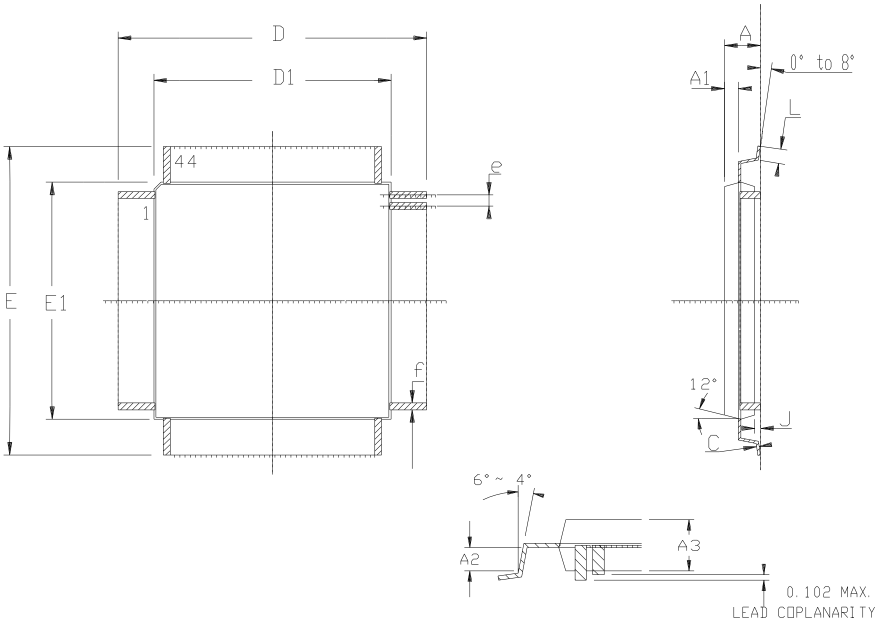
Part Number	Memory size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS87C51RB2-MCA	OBSOLETE					
TS87C51RB2-MCB						
TS87C51RB2-MCE						
TS87C51RB2-MIA						
TS87C51RB2-MIB						
TS87C51RB2-MIE						
TS87C51RB2-LCA						
TS87C51RB2-LCB						
TS87C51RB2-LCE						
TS87C51RB2-LIA						
TS87C51RB2-LIB						
TS87C51RB2-LIE						
TS87C51RB2-VCA						
TS87C51RB2-VCB						
TS87C51RB2-VCE						
TS87C51RB2-VIA						
TS87C51RB2-VIB						
TS87C51RB2-VIE						
AT87C51RB2-3CSUM	OTP 16k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PDIL40	Stick
AT87C51RB2-SLSUM	OTP 16k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PLCC44	Stick
AT87C51RB2-RLTUM	OTP 16k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	VQFP44	Tray
AT87C51RB2-3CSUL	OTP 16k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PDIL40	Stick
AT87C51RB2-SLSUL	OTP 16k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PLCC44	Stick
AT87C51RB2-RLTUL	OTP 16k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	VQFP44	Tray

Part Number	Memory size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS87C51RD2-MCA	OBSOLETE					
TS87C51RD2-MCB						
TS87C51RD2-MCE						
TS87C51RD2-MIA						
TS87C51RD2-MIB						
TS87C51RD2-MIE						
TS87C51RD2-LCA						
TS87C51RD2-LCB						
TS87C51RD2-LCE						
TS87C51RD2-LIA						
TS87C51RD2-LIB						
TS87C51RD2-LIE						
TS87C51RD2-VCA						
TS87C51RD2-VCB						
TS87C51RD2-VCE						
TS87C51RD2-VCL						
TS87C51RD2-VIA						
TS87C51RD2-VIB						
TS87C51RD2-VIE						
AT87C51RD2-3CSUM	OTP 64k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PDIL40	Stick
AT87C51RD2-SLSUM	OTP 64k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PLCC44	Stick
AT87C51RD2-RLTUM	OTP 64k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	VQFP44	Tray
AT87C51RD2-3CSUL	OTP 64k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PDIL40	Stick
AT87C51RD2-SLSUL	OTP 64k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PLCC44	Stick
AT87C51RD2-RLTUL	OTP 64k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	VQFP44	Tray

Part Number	Memory size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS83C51RB2-MCA	OBSOLETE					
TS83C51RB2-MCB						
TS83C51RB2-MCE						
TS83C51RB2-MIA						
TS83C51RB2-MIB						
TS83C51RB2-MIE						
TS83C51RB2-LCA						
TS83C51RB2-LCB						
TS83C51RB2-LCE						
TS83C51RB2-LIA						
TS83C51RB2-LIB						
TS83C51RB2-LIE						
TS83C51RB2-VCA						
TS83C51RB2-VCB						
TS83C51RB2-VCE						
TS83C51RB2-VIA						
TS83C51RB2-VIB						
TS83C51RB2-VIE						
AT83C51RB2-3CSUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PDIL40	Stick
AT83C51RB2-SLSUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PLCC44	Stick
AT83C51RB2-RLTUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	VQFP44	Tray
AT83C51RB2-3CSUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PDIL40	Stick
AT83C51RB2-SLSUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PLCC44	Stick
AT83C51RB2-RLTUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	VQFP44	Tray

Part Number	Memory size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS83C51RC2-MCA	OBSOLETE					
TS83C51RC2-MCB						
TS83C51RC2-MCE						
TS83C51RC2-MIA						
TS83C51RC2-MIB						
TS83C51RC2-MIE						
TS83C51RC2-LCA						
TS83C51RC2-LCB						
TS83C51RC2-LCE						
TS83C51RC2-LIA						
TS83C51RC2-LIB						
TS83C51RC2-LIE						
TS83C51RC2-VCA						
TS83C51RC2-VCB						
TS83C51RC2-VCE						
TS83C51RC2-VIA						
TS83C51RC2-VIB						
TS83C51RC2-VIE						
AT83C51RC2-3CSUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PDIL40	Stick
AT83C51RC2-SLSUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PLCC44	Stick
AT83C51RC2-RLTUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	VQFP44	Tray
AT83C51RC2-3CSUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PDIL40	Stick
AT83C51RC2-SLSUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PLCC44	Stick
AT83C51RC2-RLTUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	VQFP44	Tray

13.3 VQFP44



	MM		INCH	
	Min	Max	Min	Max
A	-	1.60	-	.063
A1	0.64 REF		.025 REF	
A2	0.64 REF		.025 REF	
A3	1.35	1.45	.053	.057
D	11.90	12.10	.468	.476
D1	9.90	10.10	.390	.398
E	11.90	12.10	.468	.476
E1	9.90	10.10	.390	.398
J	0.05	-	.002	-
L	0.45	0.75	.018	.030
e	0.80 BSC		.0315 BSC	
f	0.35 BSC		.014 BSC	