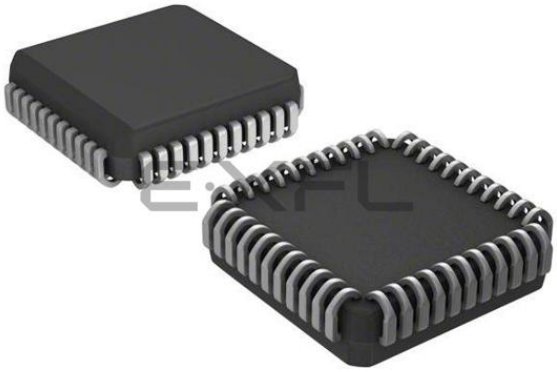

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at80c51ra2-slrul

facilitates multiprocessor communication (EUART) and an X2 speed improvement mechanism.

The fully static design of the TS80C51Rx2 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The TS80C51Rx2 has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the timers, the serial port and the interrupt system are still operating. In the power-down mode the RAM is saved and all other functions are inoperative.

PDIL40 PLCC44 VQFP44 1.4	ROM (bytes)	EPROM (bytes)	XRAM (bytes)	TOTAL RAM (bytes)	I/O
TS80C51RA2	0	0	256	512	32
TS80C51RD2	0	0	768	1024	32
TS83C51RB2	16k	0	256	512	32
TS83C51RC2	32k	0	256	512	32
TS83C51RD2	64k	0	768	1024	32
TS87C51RB2	0	16k	256	512	32
TS87C51RC2	0	32k	256	512	32
TS87C51RD2	0	64k	768	1024	32

PLCC68 VQFP64 1.4	ROM (bytes)	EPROM (bytes)	XRAM (bytes)	TOTAL RAM (bytes)	I/O
TS80C51RD2	0	0	768	1024	48
TS83C51RD2	64k	0	768	1024	48
TS87C51RD2	0	64k	768	1024	48

4. SFR Mapping

The Special Function Registers (SFRs) of the TS80C51Rx2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3, P4, P5
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- HDW Watchdog Timer Reset: WDTRST, WDTPRG
- PCA registers: CL, CH, CCAPiL, CCAPiH, CCON, CMOD, CCAPMi
- Interrupt system registers: IE, IP, IPH
- Others: AUXR, CKCON

P0.0	15	6
P0.1	14	5
P0.2	12	3
P0.3	11	2
P0.4	9	64
P0.5	6	61
P0.6	5	60
P0.7	3	59
P1.0	19	10
P1.1	21	12
P1.2	22	13
P1.3	23	14
P1.4	25	16
P1.5	27	18
P1.6	28	19
P1.7	29	20
P2.0	54	43
P2.1	55	44
P2.2	56	45
P2.3	58	47
P2.4	59	48
P2.5	61	50
P2.6	64	53
P2.7	65	54
P3.0	34	25
P3.1	39	28

Pin	PLCC68	SQUARE VQFP64 1.4
P3.2	40	29
P3.3	41	30
P3.4	42	31
P3.5	43	32
P3.6	45	34
P3.7	47	36
RESET	30	21
ALE/$\overline{\text{PROG}}$	68	56

5.4 Dual Data Pointer Register

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 (Table 5-3) that allows the program code to switch between them (Refer to Figure 5-3).

Figure 5-3. Use of Dual Pointer

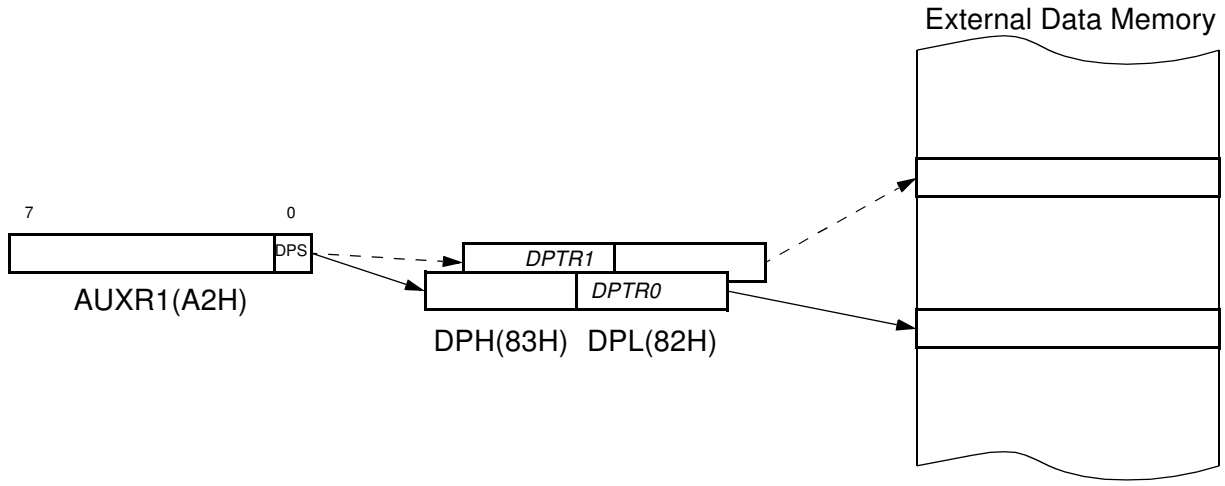


Table 5-3. AUXR1: Auxiliary Register 1

AUXR1 Address 0A2H		-	-	-	-	GF3	-	-	DPS
	Reset value	X	X	X	X	0	X	X	0

Symbol	Function	
-	Not implemented, reserved for future use (1)	
DPS	Data Pointer Selection.	
	DPS	Operating Mode
	0	DPTR0 Selected
	1	DPTR1 Selected
GF3	This bit is a general purpose user flag(2).	

1. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

GF3 will not be available on first version of the RC devices.

It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.

Figure 6-3. Clock-Out Mode C/$\overline{T2}$ = 0

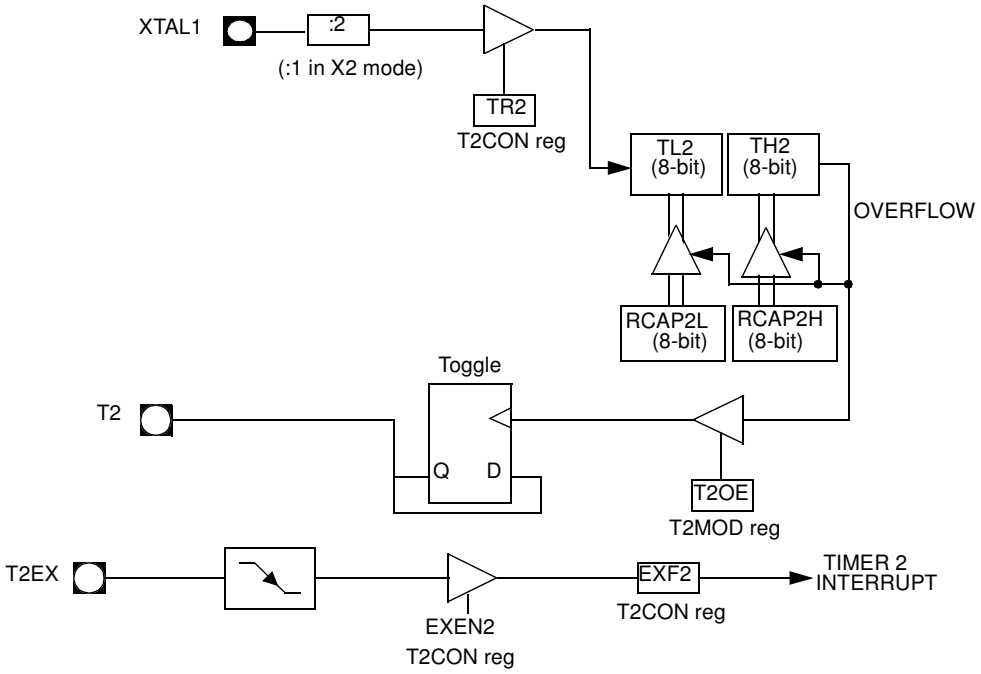


Table 6-2. T2CON Register

T2CON - Timer 2 Control Register (C8h)

7	6	5	4	3	2	1	0
TF2	**EXF2**	**RCLK**	**TCLK**	**EXEN2**	**TR2**	**C/T2#**	**CP/RL2#**

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output (See Table 6-8 & Table 6-9)

Table 6-8. CCAPnH: PCA Modules Capture/Compare Registers High

CCAPnH Address
n = 0 - 4

CCAP0H=0FAH
CCAP1H=0FBH
CCAP2H=0FCH
CCAP3H=0FDH
CCAP4H=0FEH

	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

Table 6-9. CCAPnL: PCA Modules Capture/Compare Registers Low

CCAPnL Address
n = 0 - 4

CCAP0L=0EAH
CCAP1L=0EBH
CCAP2L=0ECH
CCAP3L=0EDH
CCAP4L=0EEH

	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

Table 6-10. CH: PCA Counter High

CH
Address 0F9H

	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

Table 6-11. CL: PCA Counter Low

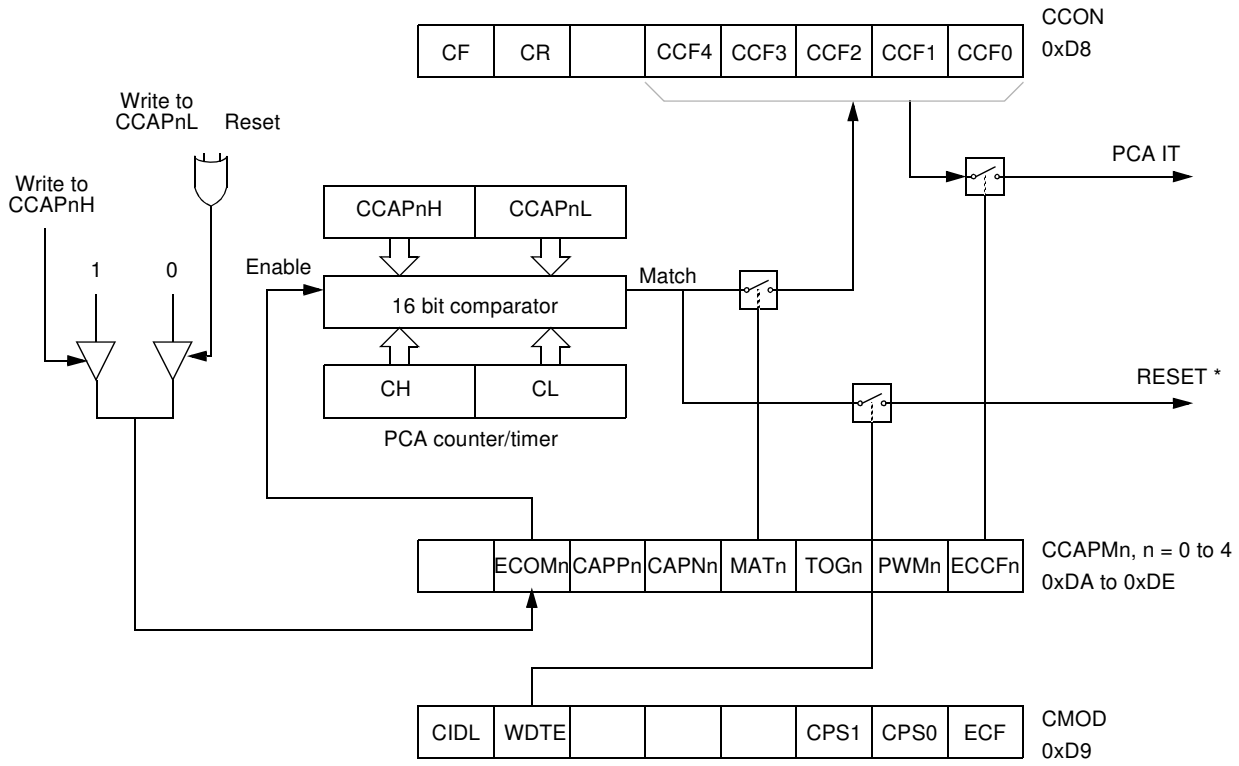
CL
Address 0E9H

	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

6.3.1 PCA Capture Mode

To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated (Refer to Figure 6-6).

Figure 6-7. PCA Compare Mode and PCA Watchdog Timer



* Only for Module 4

Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen. Writing to CCAPnH will set the ECOM bit.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.

6.3.3 High Speed Output Mode

In this mode the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (See Figure 6-8).

A prior write must be done to CCAPnL and CCAPnH before writing the ECOMn bit.

6.4 TS80C51Rx2 Serial I/O Port

The serial I/O port in the TS80C51Rx2 is compatible with the serial I/O port in the 80C52.

It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

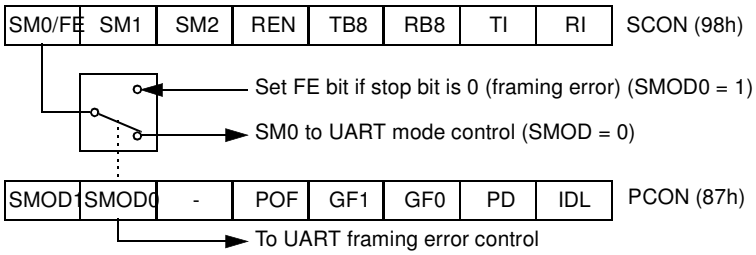
Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

6.4.1 Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 6-10).

Figure 6-10. Framing Error Block Diagram



When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 6-14.) bit is set.
Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 6-11 and Figure 6-12).

Figure 6-11. UART Timings in Mode 1

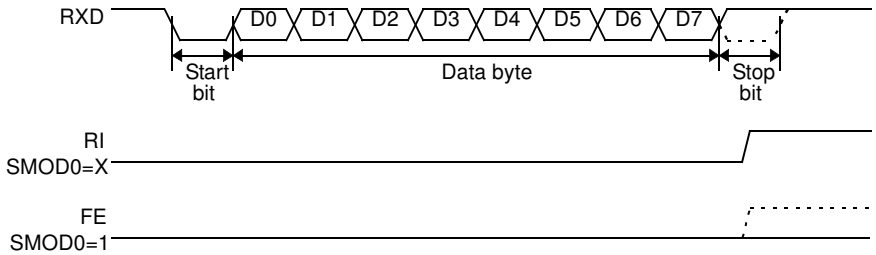
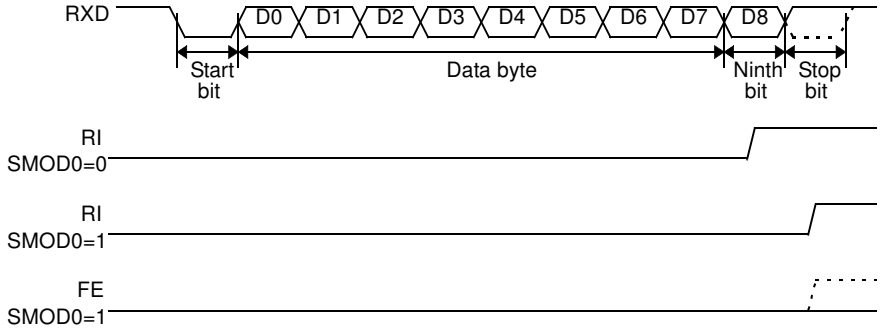


Figure 6-12. UART Timings in Modes 2 and 3



6.4.2 Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.
If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

Note: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

6.4.3 Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.
To address a device by its individual address, the SADEN mask byte must be `1111 1111b`.

For example:

```
SADDR0101 0110b
SADEN1111 1100b
Given0101 01XXb
```

The following is an example of how to use given addresses to address different slaves:

```
Slave A:SADDR1111 0001b
   SADEN1111 1010b
   Given1111 0X0Xb


Slave B:SADDR1111 0011b
   SADEN1111 1001b
   Given1111 0XX1b
```

Table 6-12. SADEN - Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 6-13. SADDR - Slave Address Register (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 6-14. SCON Register
SCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0
FE/SM0	**SM1**	**SM2**	**REN**	**TB8**	**RB8**	**TI**	**RI**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0** Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-Off Flag** Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-Down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b
Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

7.1 Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 7-2. AUXR Register
AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	EXTRAM	AO

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	EXTRAM	**EXTRAM bit** See Table 6-1.
0	AO	**ALE Output bit** Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = XXXX XX00b
Not bit addressable

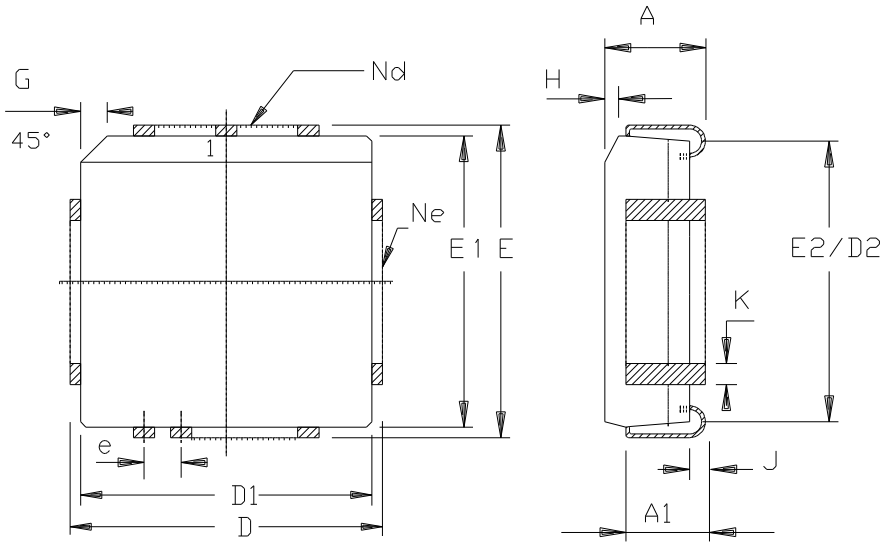
60h	FCh	Product name: TS87C51RD2
60h	37h	Product name: TS83C51RC2
60h	B7h	Product name: TS87C51RC2
60h	3Bh	Product name: TS83C51RB2
60h	BBh	Product name: TS87C51RB2
61h	FFh	Product revision number

Part Number	Memory size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT80C51RA2-3CSCV	OBSOLETE					
AT80C51RA2-SLSCV						
AT80C51RA2-RLTCV						
AT80C51RA2-3CSIV						
AT80C51RA2-SLSIV						
AT80C51RA2-RLSIV						
TS80C51RD2-MCA	Not recommended use AT87C51RD2					
TS80C51RD2-MCB	Not recommended use AT87C51RD2					
TS80C51RD2-MCE	Not recommended use AT87C51RD2					
TS80C51RD2-MIA	Not recommended use AT87C51RD2					
TS80C51RD2-MIB	Not recommended use AT87C51RD2					
TS80C51RD2-MIE	Not recommended use AT87C51RD2					
TS80C51RD2-LCA	Not recommended use AT87C51RD2					
TS80C51RD2-LCB	Not recommended use AT87C51RD2					
TS80C51RD2-LCE	Not recommended use AT87C51RD2					
TS80C51RD2-LIA	Not recommended use AT87C51RD2					
TS80C51RD2-LIB	Not recommended use AT87C51RD2					
TS80C51RD2-LIE	Not recommended use AT87C51RD2					
TS80C51RD2-VCA	Not recommended use AT87C51RD2					
TS80C51RD2-VCB	Not recommended use AT87C51RD2					
TS80C51RD2-VCE	Not recommended use AT87C51RD2					
TS80C51RD2-VIA	Not recommended use AT87C51RD2					
TS80C51RD2-VIB	Not recommended use AT87C51RD2					
TS80C51RD2-VIE	Not recommended use AT87C51RD2					
AT80C51RD2-3CSUM	Not recommended use AT87C51RD2					
AT80C51RD2-SLSUM	Not recommended use AT87C51RD2					
AT80C51RD2-RLTUM	Not recommended use AT87C51RD2					
AT80C51RD2-3CSUL	Not recommended use AT87C51RD2					
AT80C51RD2-SLSUL	Not recommended use AT87C51RD2					
AT80C51RD2-RLTUL	Not recommended use AT87C51RD2					

Part Number	Memory size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS83C51RB2-MCA	OBSOLETE					
TS83C51RB2-MCB						
TS83C51RB2-MCE						
TS83C51RB2-MIA						
TS83C51RB2-MIB						
TS83C51RB2-MIE						
TS83C51RB2-LCA						
TS83C51RB2-LCB						
TS83C51RB2-LCE						
TS83C51RB2-LIA						
TS83C51RB2-LIB						
TS83C51RB2-LIE						
TS83C51RB2-VCA						
TS83C51RB2-VCB						
TS83C51RB2-VCE						
TS83C51RB2-VIA						
TS83C51RB2-VIB						
TS83C51RB2-VIE						
AT83C51RB2-3CSUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PDIL40	Stick
AT83C51RB2-SLSUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PLCC44	Stick
AT83C51RB2-RLTUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	VQFP44	Tray
AT83C51RB2-3CSUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PDIL40	Stick
AT83C51RB2-SLSUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PLCC44	Stick
AT83C51RB2-RLTUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	VQFP44	Tray

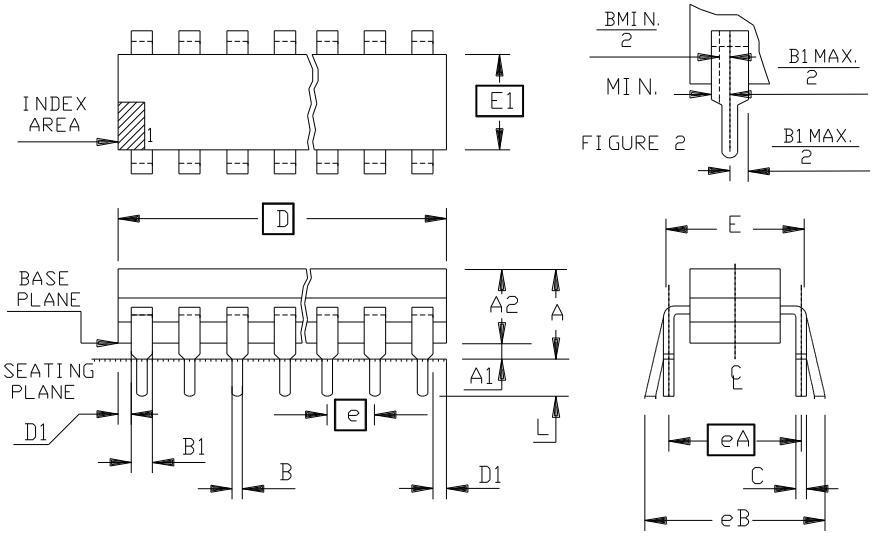
13. Package Drawings

13.1 PLCC44



	MM		INCH	
A	4.20	4.57	.165	.180
A1	2.29	3.04	.090	.120
D	17.40	17.65	.685	.695
D1	16.44	16.66	.647	.656
D2	14.99	16.00	.590	.630
E	17.40	17.65	.685	.695
E1	16.44	16.66	.647	.656
E2	14.99	16.00	.590	.630
e	1.27	BSC	.050	BSC
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	-	.020	-
K	0.33	0.53	.013	.021
Nd	11		11	
Ne	11		11	
PKG STD	00			

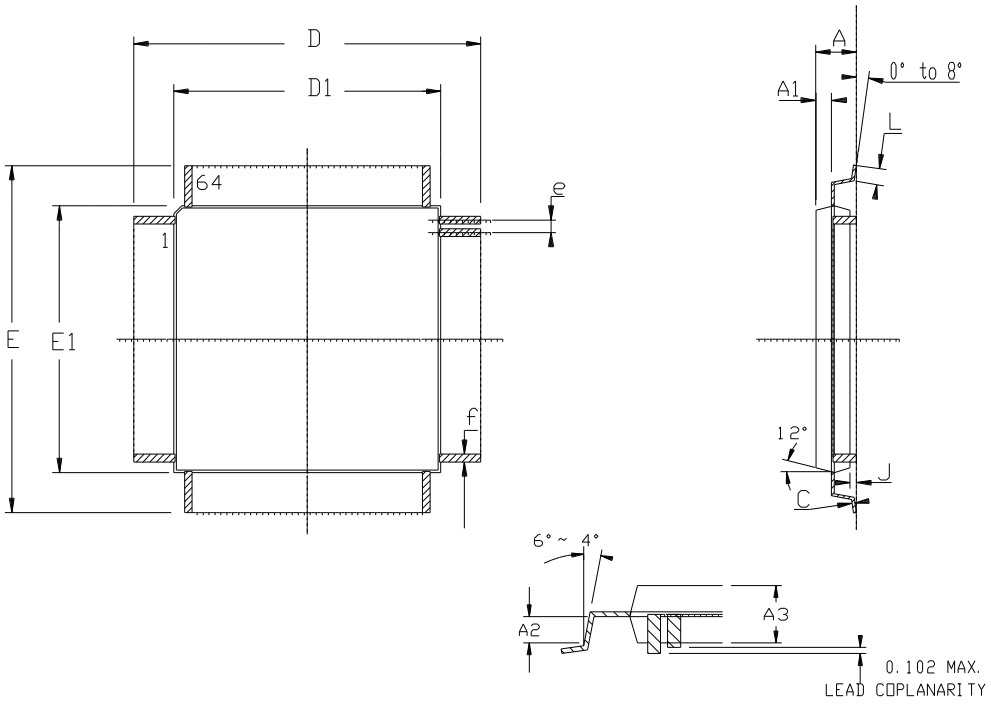
13.2 PDIL40



	MM		INCH	
A	-	5.08	-	.200
A1	0.38	-	.015	-
A2	3.18	4.95	.125	.195
B	0.36	0.56	.014	.022
B1	0.76	1.78	.030	.070
C	0.20	0.38	.008	.015
D	50.29	53.21	1.980	2.095
E	15.24	15.87	.600	.625
E1	12.32	14.73	.485	.580
e	2.54	B.S.C	.100	B.S.C
eA	15.24	B.S.C	.600	B.S.C
eB	-	17.78	-	.700
L	2.93	3.81	.115	.150
D1	0.13	-	.005	-
PKG STD		02		

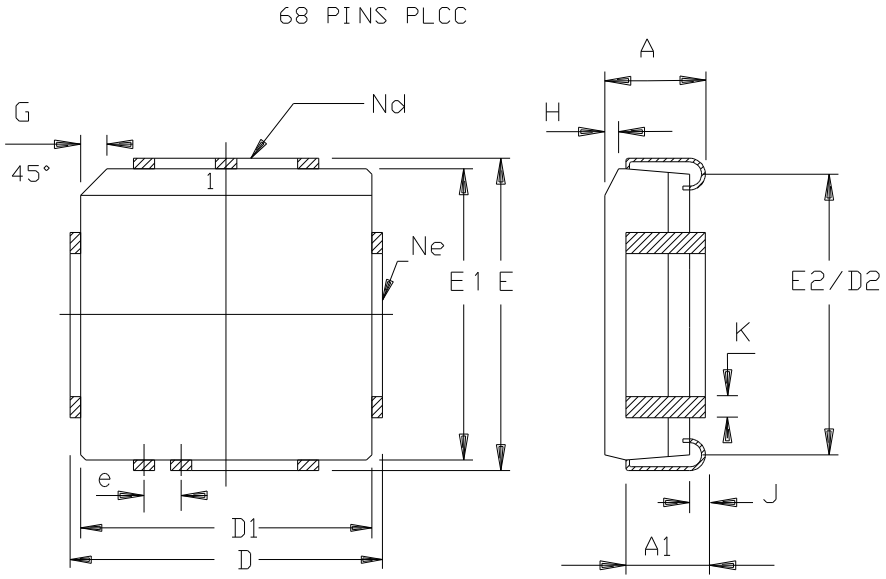
13.4 VQFP64

SQUARE GULL WING (1.4 mm)



	MM		INCH	
	Min	Max	Min	Max
A	-	1.60	-	.063
A1	0.64 REF		.025 REF	
A2	0.64 REF		.025 REF	
A3	1.35	1.45	.053	.057
D	11.75	12.25	.463	.483
D1	9.90	10.10	.390	.398
E	11.75	12.25	.463	.483
E1	9.90	10.10	.390	.398
J	0.05	-	.002	-
L	0.45	0.75	.018	.030
e	0.50 BSC		.0197 BSC	
f	0.25 BSC		.010 BSC	

13.5 PLCC68



	MM		INCH	
A	4.20	5.08	.165	.200
A1	2.29	3.30	.090	.130
D	25.02	25.27	.985	.995
D1	24.13	24.33	.950	.958
D2	22.61	23.62	.890	.930
E	25.02	25.27	.985	.995
E1	24.13	24.33	.950	.958
E2	22.61	23.62	.890	.930
e	1.27	BSC	.050	BSC
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	-	.020	-
K	0.33	0.53	.013	.021
Nd	17		17	
Ne	17		17	
PKG STD	00			

14. Datasheet Revision History

14.1 Changes from 4188E to 4188F

1. Removed TS80C51RD2 and AT80C51RD2 from “Ordering Information” on page 73.
2. Removed non-green part numbers from ordering information.

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