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Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at87c51rc2-slsul

facilitates multiprocessor communication (EUSART) and an X2 speed improvement mechanism.

The fully static design of the TS80C51Rx2 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The TS80C51Rx2 has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the timers, the serial port and the interrupt system are still operating. In the power-down mode the RAM is saved and all other functions are inoperative.

PDIL40 PLCC44 VQFP44 1.4	ROM (bytes)	EPROM (bytes)	XRAM (bytes)	TOTAL RAM (bytes)	I/O
TS80C51RA2	0	0	256	512	32
TS80C51RD2	0	0	768	1024	32
TS83C51RB2	16k	0	256	512	32
TS83C51RC2	32k	0	256	512	32
TS83C51RD2	64k	0	768	1024	32
TS87C51RB2	0	16k	256	512	32
TS87C51RC2	0	32k	256	512	32
TS87C51RD2	0	64k	768	1024	32

PLCC68 VQFP64 1.4	ROM (bytes)	EPROM (bytes)	XRAM (bytes)	TOTAL RAM (bytes)	I/O
TS80C51RD2	0	0	768	1024	48
TS83C51RD2	64k	0	768	1024	48
TS87C51RD2	0	64k	768	1024	48

5.2 TS80C51Rx2 Enhanced Features

In comparison to the original 80C52, the TS8xC51Rx2 implements some new features, which are:

- The X2 option.
- The Dual Data Pointer.
- The extended RAM.
- The Programmable Counter Array (PCA).
- The Watchdog.
- The 4 level interrupt priority system.
- The power-off flag.
- The ONCE mode.
- The ALE disabling.
- Some enhanced features are also located in the UART and the timer 2.

5.3 X2 Feature

The TS80C51Rx2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divides frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Saves power consumption while keeping same CPU power (oscillator power saving).
- Saves power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increases CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

5.3.1 Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. [Figure 5-1](#) shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. [Figure 5-2](#) shows the mode switching waveforms.

5.4 Dual Data Pointer Register

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 (Table 5-3) that allows the program code to switch between them (Refer to Figure 5-3).

Figure 5-3. Use of Dual Pointer

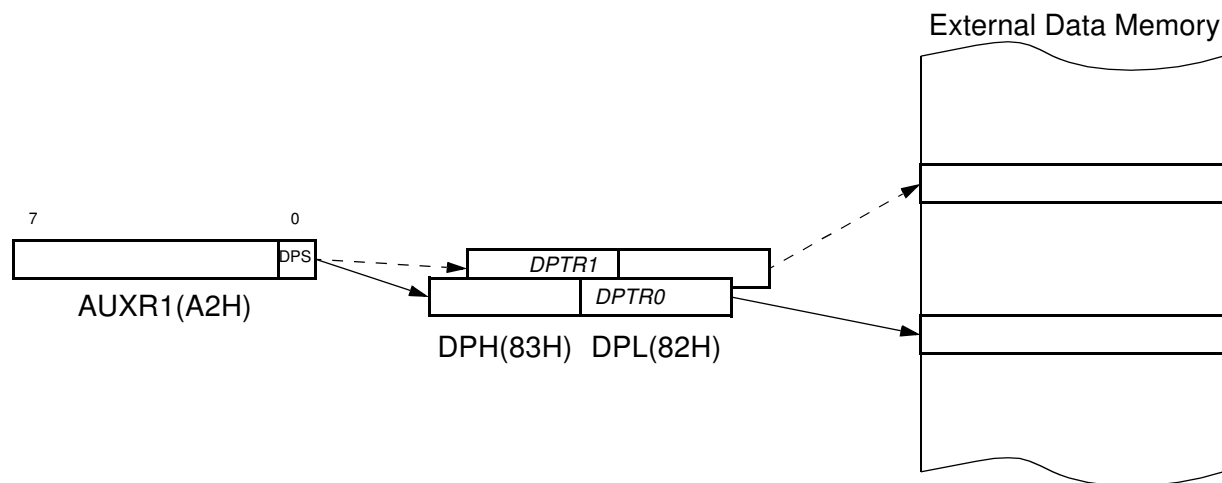


Table 5-3. AUXR1: Auxiliary Register 1

AUXR1 Address 0A2H		-	-	-	-	GF3	-	-	DPS
	Reset value	X	X	X	X	0	X	X	0
Symbol	Function								
-	Not implemented, reserved for future use ⁽¹⁾								
DPS	Data Pointer Selection.								
	DPS	Operating Mode							
	0	DPTR0 Selected							
	1	DPTR1 Selected							
GF3	This bit is a general purpose user flag ⁽²⁾ .								

1. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

GF3 will not be available on first version of the RC devices.

Bit Number	Bit Mnemonic	Description
7	TF2	Timer 2 overflow Flag Must be cleared by software. Set by hardware on timer 2 overflow, if RCLK = 0 and TCLK = 0.
6	EXF2	Timer 2 External Flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. When set, causes the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled. Must be cleared by software. EXF2 doesn't cause an interrupt in Up/down counter mode (DCEN = 1)
5	RCLK	Receive Clock bit Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3. Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3.
4	TCLK	Transmit Clock bit Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3. Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3.
3	EXEN2	Timer 2 External Enable bit Clear to ignore events on T2EX pin for timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port.
2	TR2	Timer 2 Run control bit Clear to turn off timer 2. Set to turn on timer 2.
1	C/T2#	Timer/Counter 2 select bit Clear for timer operation (input from internal clock system: F _{osc}). Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode.
0	CP/RL2#	Timer 2 Capture/Reload bit If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to auto-reload on timer 2 overflow. Clear to auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1. Set to capture on negative transitions on T2EX pin if EXEN2=1.

Reset Value = 0000 0000b

Bit addressable

Table 6-3. T2MOD Register
T2MOD - Timer 2 Mode Control Register (C9h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN

Figure 6-4. PCA Timer/Counter

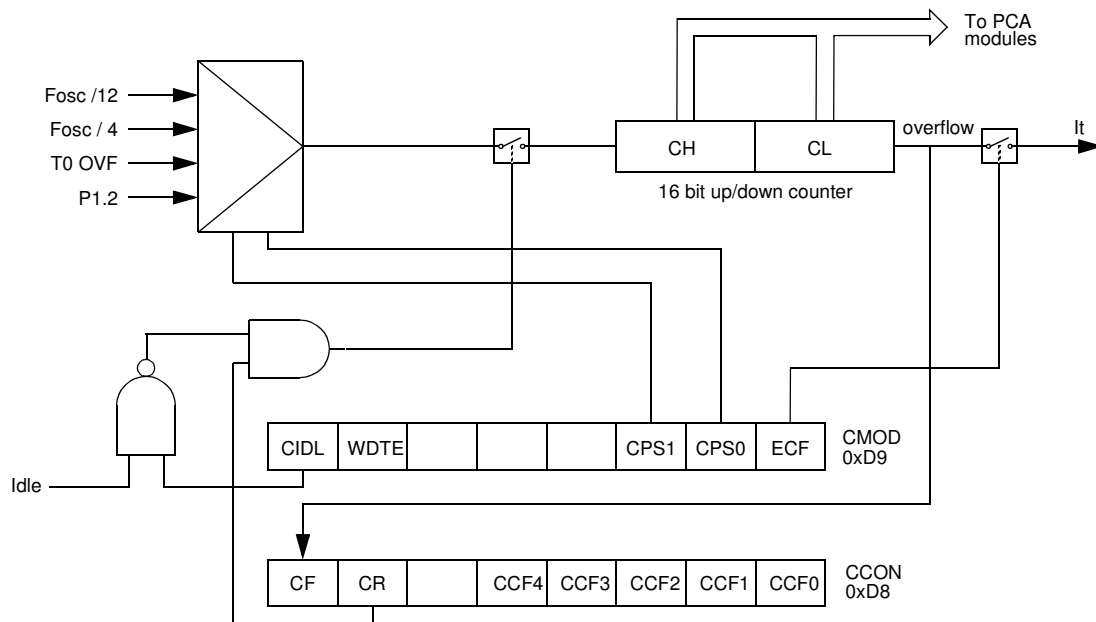


Table 6-4. CMOD: PCA Counter Mode Register

CMOD									
Address 0D9H		CIDL	WDTE	-	-	-	CPS1	CPS0	ECF
Reset value		0	0	X	X	X	0	0	0

Symbol	Function		
CIDL	Counter Idle control: CIDL = 0 programs the PCA Counter to continue functioning during idle Mode. CIDL = 1 programs it to be gated off during idle.		
WDTE	Watchdog Timer Enable: WDTE = 0 disables Watchdog Timer function on PCA Module 4. WDTE = 1 enables it.		
-	Not implemented, reserved for future use. ⁽¹⁾		
CPS1	PCA Count Pulse Select bit 1.		
CPS0	PCA Count Pulse Select bit 0.		
	CPS1	CPS0	Selected PCA input. ⁽²⁾
	0	0	Internal clock $f_{osc}/12$ (Or $f_{osc}/6$ in X2 Mode).
	0	1	Internal clock $f_{osc}/4$ (Or $f_{osc}/2$ in X2 Mode).
	1	0	Timer 0 Overflow
	1	1	External clock at ECI/P1.2 pin (max rate = $f_{osc}/8$)
ECF	PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function of CF.		

1. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.
2. f_{osc} = oscillator frequency

The CMOD SFR includes three additional bits associated with the PCA (See Figure 6-4 and Table 6-4).

- The CIDL bit which allows the PCA to stop during idle mode.
- The WDTE bit which enables or disables the watchdog function on module 4.
- The ECF bit which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows.

The **CCON SFR** contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (Refer to Table 6-5).

- Bit CR (CCON.6) must be set by software to run the PCA. The PCA is shut off by clearing this bit.
- Bit CF: The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software.
- Bits 0 through 4 are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software.

Table 6-5. CCON: PCA Counter Control Register

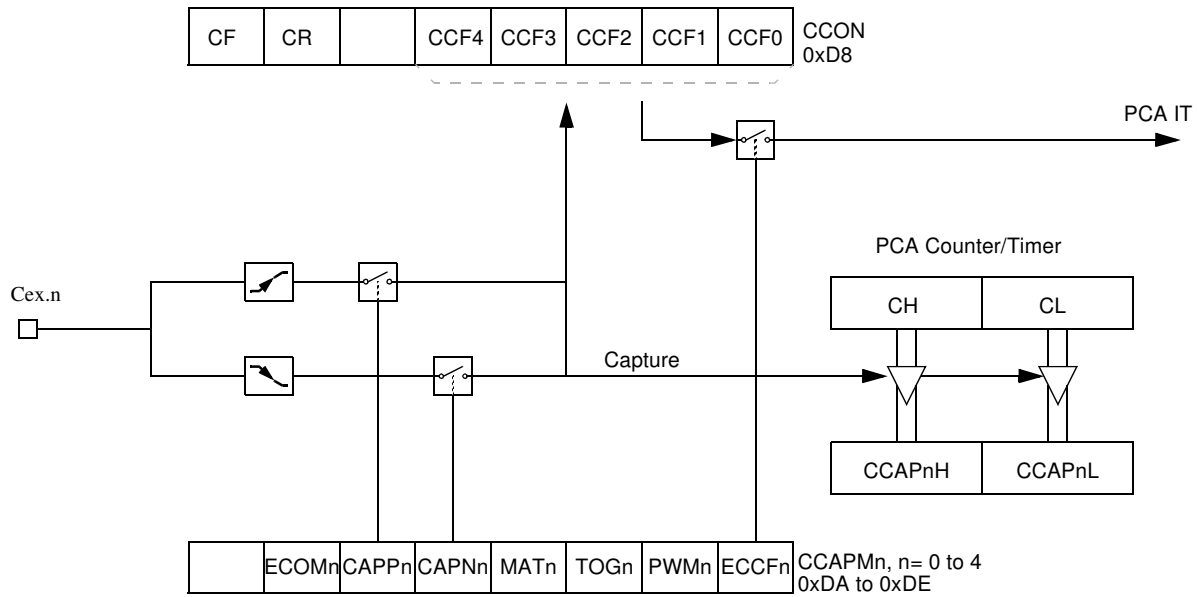
CCON Address 0D8H		CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0
Reset value		0	0	X	0	0	0	0	0
Symbol	Function								
CF	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.								
CR	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.								
-	Not implemented, reserved for future use. ⁽¹⁾								
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.								

1. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

The **watchdog timer** function is implemented in module 4 (See Figure 6-7).

The **PCA interrupt** system is shown in Figure 6-5.

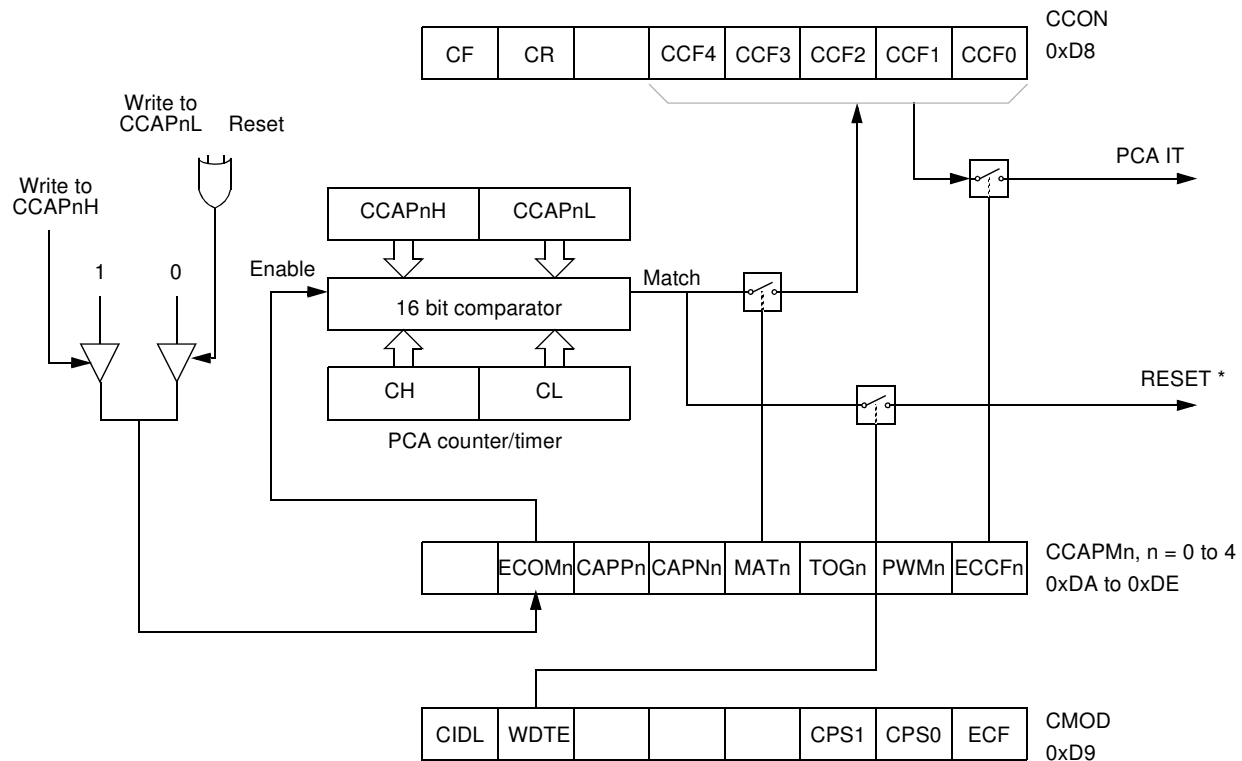
Figure 6-6. PCA Capture Mode



6.3.2 16-bit Software Timer/ Compare Mode

The PCA modules can be used as software timers by setting both the **ECOM** and **MAT** bits in the modules **CCAPMn** register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the **CCFn** (**CCON** SFR) and the **ECCFn** (**CCAPMn** SFR) bits for the module are both set (See Figure 6-7).

Figure 6-7. PCA Compare Mode and PCA Watchdog Timer



* Only for Module 4

Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen. Writing to CCAPnH will set the ECOM bit.

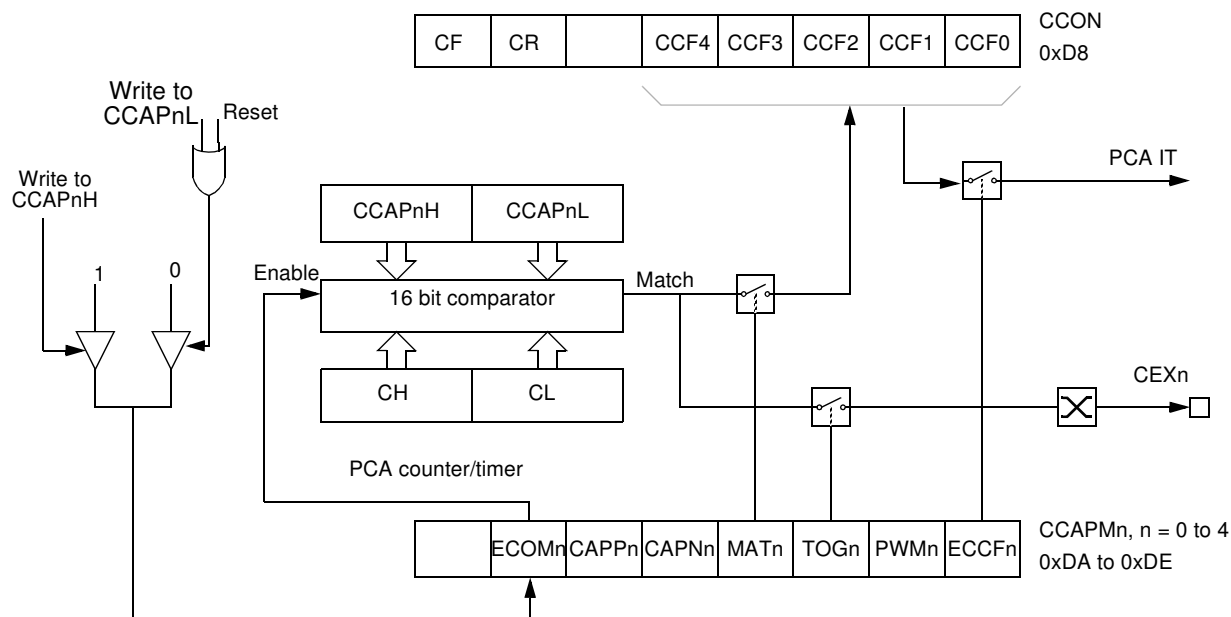
Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.

6.3.3 High Speed Output Mode

In this mode the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (See Figure 6-8).

A prior write must be done to CCAPnL and CCAPnH before writing the ECOMn bit.

Figure 6-8. PCA High Speed Output Mode



Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.

6.3.4 Pulse Width Modulator Mode

All of the PCA modules can be used as PWM outputs. Figure 6-9 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPL_n. When the value of the PCA CL SFR is less than the value in the module's CCAPL_n SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPL_n is reloaded with the value in CCAPH_n. This allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPM_n register must be set to enable the PWM mode.

Bit Number	Bit Mnemonic	Description
7	SMOD1	Serial port Mode bit 1 Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	Serial port Mode bit 0 Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	POF	Power-Off Flag Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	Power-Down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	Idle mode bit Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b

Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

Bit Number	Bit Mnemonic	Description																																				
7	T4	Reserved Do not try to set or clear this bit.																																				
6	T3																																					
5	T2																																					
4	T1																																					
3	T0																																					
2	S2	WDT Time-out select bit 2																																				
1	S1	WDT Time-out select bit 1																																				
0	S0	WDT Time-out select bit 0																																				
		<table><tr><td><u>S2</u></td><td><u>S1</u></td><td><u>S0</u></td><td><u>Selected Time-out</u></td></tr><tr><td>0</td><td>0</td><td>0</td><td>$0(2^{14} - 1)$ machine cycles, 16.3 ms @ 12 MHz</td></tr><tr><td>0</td><td>0</td><td>1</td><td>$1(2^{15} - 1)$ machine cycles, 32.7 ms @ 12 MHz</td></tr><tr><td>0</td><td>1</td><td>0</td><td>$0(2^{16} - 1)$ machine cycles, 65.5 ms @ 12 MHz</td></tr><tr><td>0</td><td>1</td><td>1</td><td>$1(2^{17} - 1)$ machine cycles, 131 ms @ 12 MHz</td></tr><tr><td>1</td><td>0</td><td>0</td><td>$0(2^{18} - 1)$ machine cycles, 262 ms @ 12 MHz</td></tr><tr><td>1</td><td>0</td><td>1</td><td>$1(2^{19} - 1)$ machine cycles, 542 ms @ 12 MHz</td></tr><tr><td>1</td><td>1</td><td>0</td><td>$0(2^{20} - 1)$ machine cycles, 1.05 s @ 12 MHz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>$1(2^{21} - 1)$ machine cycles, 2.09 s @ 12 MHz</td></tr></table>	<u>S2</u>	<u>S1</u>	<u>S0</u>	<u>Selected Time-out</u>	0	0	0	$0(2^{14} - 1)$ machine cycles, 16.3 ms @ 12 MHz	0	0	1	$1(2^{15} - 1)$ machine cycles, 32.7 ms @ 12 MHz	0	1	0	$0(2^{16} - 1)$ machine cycles, 65.5 ms @ 12 MHz	0	1	1	$1(2^{17} - 1)$ machine cycles, 131 ms @ 12 MHz	1	0	0	$0(2^{18} - 1)$ machine cycles, 262 ms @ 12 MHz	1	0	1	$1(2^{19} - 1)$ machine cycles, 542 ms @ 12 MHz	1	1	0	$0(2^{20} - 1)$ machine cycles, 1.05 s @ 12 MHz	1	1	1	$1(2^{21} - 1)$ machine cycles, 2.09 s @ 12 MHz
<u>S2</u>	<u>S1</u>	<u>S0</u>	<u>Selected Time-out</u>																																			
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0	1	1	$1(2^{17} - 1)$ machine cycles, 131 ms @ 12 MHz																																			
1	0	0	$0(2^{18} - 1)$ machine cycles, 262 ms @ 12 MHz																																			
1	0	1	$1(2^{19} - 1)$ machine cycles, 542 ms @ 12 MHz																																			
1	1	0	$0(2^{20} - 1)$ machine cycles, 1.05 s @ 12 MHz																																			
1	1	1	$1(2^{21} - 1)$ machine cycles, 2.09 s @ 12 MHz																																			

Reset value XXXX X000

6.8.2 WDT during Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode the user does not need to service the WDT. There are 2 methods of exiting Power-down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally should whenever the TS80C51Rx2 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service routine.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is best to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the TS80C51Rx2 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

6.9 ONCE™ Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS8xC51Rx2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C51Rx2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and $\overline{\text{PSEN}}$ is high.
- Hold ALE low as RST is deactivated.

While the TS80C51Rx2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 26. shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

Table 6-23. External Pin Status during ONCE Mode

ALE	PSEN	Port 0	Port 1	Port 2	Port 3	XTAL1/2
Weak pull-up	Weak pull-up	Float	Weak pull-up	Weak pull-up	Weak pull-up	Active

Table 11-1. DC Parameters in Standard Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	Output High Voltage, ports 1, 2, 3, 4, 5	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V V V	$I_{OH} = -10 \mu A$ $I_{OH} = -30 \mu A$ $I_{OH} = -60 \mu A$ $V_{CC} = 5 V \pm 10\%$
V_{OH1}	Output High Voltage, port 0	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V V V	$I_{OH} = -200 \mu A$ $I_{OH} = -3.2 mA$ $I_{OH} = -7.0 mA$ $V_{CC} = 5 V \pm 10\%$
V_{OH2}	Output High Voltage, ALE, \overline{PSEN}	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V V V	$I_{OH} = -100 \mu A$ $I_{OH} = -1.6 mA$ $I_{OH} = -3.5 mA$ $V_{CC} = 5 V \pm 10\%$
R_{RST}	RST Pulldown Resistor	50	90 ⁽⁵⁾	200	k Ω	
I_{IL}	Logical 0 Input Current ports 1, 2, 3, 4, 5			-50	μA	$V_{in} = 0.45 V$
I_{LI}	Input Leakage Current			± 10	μA	$0.45 V < V_{in} < V_{CC}$
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3, 4, 5			-650	μA	$V_{in} = 2.0 V$
C_{IO}	Capacitance of I/O Buffer			10	pF	$F_c = 1 MHz$ $T_A = 25^\circ C$
I_{PD}	Power-down Current		20 ⁽⁵⁾	50	μA	$2.0 V < V_{CC} < 5.5 V^{(3)}$
I_{CC} under RESET	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			1 + 0.4 Freq (MHz) @12MHz 5.8 @16MHz 7.4	mA	$V_{CC} = 5.5 V^{(1)}$
I_{CC} operating	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			3 + 0.6 Freq (MHz) @12MHz 10.2 @16MHz 12.6	mA	$V_{CC} = 5.5 V^{(8)}$
I_{CC} idle	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			0.25+0.3 Freq (MHz) @12MHz 3.9 @16MHz 5.1	mA	$V_{CC} = 5.5 V^{(2)}$

11.5.2 External Program Memory Characteristics

Table 11-5. Symbol Description

Symbol	Parameter
T	Oscillator clock period
T _{LHLL}	ALE pulse width
T _{AVLL}	Address Valid to ALE
T _{LLAX}	Address Hold After ALE
T _{LLIV}	ALE to Valid Instruction In
T _{LLPL}	ALE to $\overline{\text{PSEN}}$
T _{PLPH}	$\overline{\text{PSEN}}$ Pulse Width
T _{PLIV}	$\overline{\text{PSEN}}$ to Valid Instruction In
T _{PXIX}	Input Instruction Hold After $\overline{\text{PSEN}}$
T _{PXIZ}	Input Instruction Float After $\overline{\text{PSEN}}$
T _{PXAV}	$\overline{\text{PSEN}}$ to Address Valid
T _{AVIV}	Address to Valid Instruction In
T _{PLAZ}	$\overline{\text{PSEN}}$ Low to Address Float

Table 11-6. AC Parameters for Fix Clock

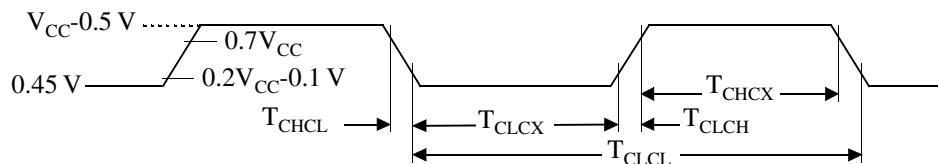
Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T	25		33		25		50		33		ns
T _{LHLL}	40		25		42		35		52		ns
T _{AVLL}	10		4		12		5		13		ns
T _{LLAX}	10		4		12		5		13		ns
T _{LLIV}		70		45		78		65		98	ns
T _{LLPL}	15		9		17		10		18		ns
T _{PLPH}	55		35		60		50		75		ns
T _{PLIV}		35		25		50		30		55	ns
T _{PXIX}	0		0		0		0		0		ns
T _{PXIZ}		18		12		20		10		18	ns
T _{AVIV}		85		53		95		80		122	ns
T _{PLAZ}		10		10		10		10		10	ns

11.5.11 External Clock Drive Characteristics (XTAL1)

Symbol	Parameter	Min	Max	Units
T_{CLCL}	Oscillator Period	25		ns
T_{CHCX}	High Time	5		ns
T_{CLCX}	Low Time	5		ns
T_{CLCH}	Rise Time		5	ns
T_{CHCL}	Fall Time		5	ns
T_{CHCX}/T_{CLCX}	Cyclic ratio in X2 mode	40	60	%

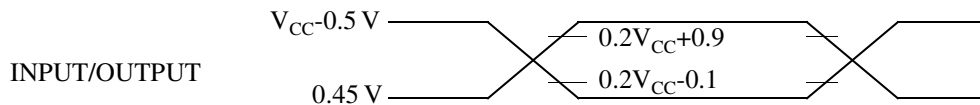
11.5.12 External Clock Drive Waveforms

Figure 11-11. External Clock Drive Waveforms



11.5.13 AC Testing Input/Output Waveforms

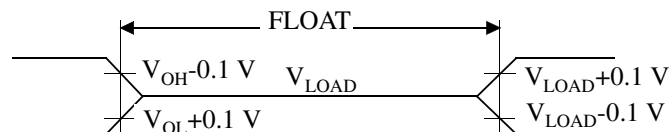
Figure 11-12. AC Testing Input/Output Waveforms



AC inputs during testing are driven at $V_{CC} - 0.5$ for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at V_{IH} min for a logic “1” and V_{IL} max for a logic “0”.

11.5.14 Float Waveforms

Figure 11-13. Float Waveforms



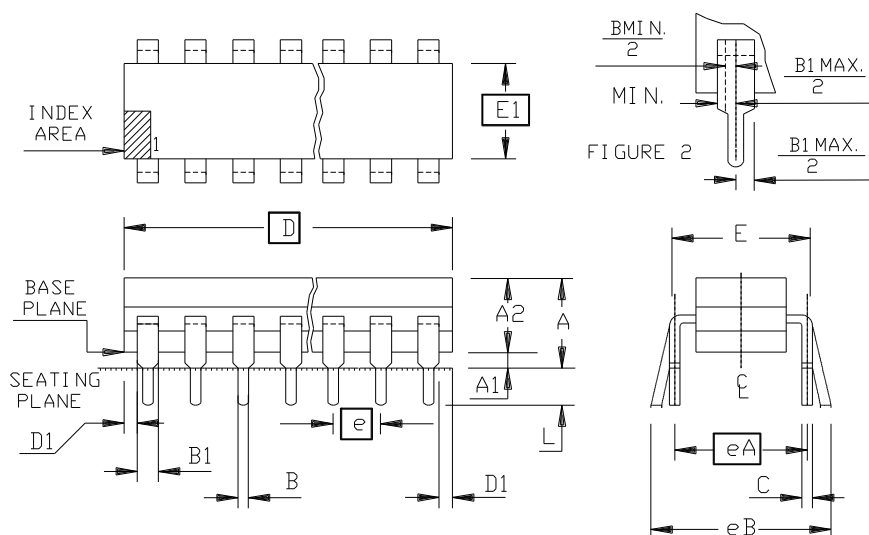
For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20mA$.

Part Number	Memory size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT80C51RA2-3CSCV	OBSOLETE					
AT80C51RA2-SLSCV						
AT80C51RA2-RLTCV						
AT80C51RA2-3CSIV						
AT80C51RA2-SLSIV						
AT80C51RA2-RLSIV						
TS80C51RD2-MCA	Not recommended use AT87C51RD2					
TS80C51RD2-MCB	Not recommended use AT87C51RD2					
TS80C51RD2-MCE	Not recommended use AT87C51RD2					
TS80C51RD2-MIA	Not recommended use AT87C51RD2					
TS80C51RD2-MIB	Not recommended use AT87C51RD2					
TS80C51RD2-MIE	Not recommended use AT87C51RD2					
TS80C51RD2-LCA	Not recommended use AT87C51RD2					
TS80C51RD2-LCB	Not recommended use AT87C51RD2					
TS80C51RD2-LCE	Not recommended use AT87C51RD2					
TS80C51RD2-LIA	Not recommended use AT87C51RD2					
TS80C51RD2-LIB	Not recommended use AT87C51RD2					
TS80C51RD2-LIE	Not recommended use AT87C51RD2					
TS80C51RD2-VCA	Not recommended use AT87C51RD2					
TS80C51RD2-VCB	Not recommended use AT87C51RD2					
TS80C51RD2-VCE	Not recommended use AT87C51RD2					
TS80C51RD2-VIA	Not recommended use AT87C51RD2					
TS80C51RD2-VIB	Not recommended use AT87C51RD2					
TS80C51RD2-VIE	Not recommended use AT87C51RD2					
AT80C51RD2-3CSUM	Not recommended use AT87C51RD2					
AT80C51RD2-SLSUM	Not recommended use AT87C51RD2					
AT80C51RD2-RLTUM	Not recommended use AT87C51RD2					
AT80C51RD2-3CSUL	Not recommended use AT87C51RD2					
AT80C51RD2-SLSUL	Not recommended use AT87C51RD2					
AT80C51RD2-RLTUL	Not recommended use AT87C51RD2					

Part Number	Memory size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS83C51RB2-MCA	OBSOLETE					
TS83C51RB2-MCB						
TS83C51RB2-MCE						
TS83C51RB2-MIA						
TS83C51RB2-MIB						
TS83C51RB2-MIE						
TS83C51RB2-LCA						
TS83C51RB2-LCB						
TS83C51RB2-LCE						
TS83C51RB2-LIA						
TS83C51RB2-LIB						
TS83C51RB2-LIE						
TS83C51RB2-VCA						
TS83C51RB2-VCB						
TS83C51RB2-VCE						
TS83C51RB2-VIA						
TS83C51RB2-VIB						
TS83C51RB2-VIE						
AT83C51RB2-3CSUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PDIL40	Stick
AT83C51RB2-SLSUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PLCC44	Stick
AT83C51RB2-RLTUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	VQFP44	Tray
AT83C51RB2-3CSUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PDIL40	Stick
AT83C51RB2-SLSUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PLCC44	Stick
AT83C51RB2-RLTUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	VQFP44	Tray

Part Number	Memory size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS83C51RD2-MCA	OBSOLETE					
TS83C51RD2-MCB						
TS83C51RD2-MCE						
TS83C51RD2-MIA						
TS83C51RD2-MIB						
TS83C51RD2-MIE						
TS83C51RD2-LCB						
TS83C51RD2-LCE						
TS83C51RD2-LIA						
TS83C51RD2-LIB						
TS83C51RD2-LIE						
TS83C51RD2-VCA						
TS83C51RD2-VCB						
TS83C51RD2-VCE						
TS83C51RD2-VIA						
TS83C51RD2-VIB						
TS83C51RD2-VIE						
AT83C51RD2-3CSUM	ROM 64k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PDIL40	Stick
AT83C51RD2-SLSUM	ROM 64k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PLCC44	Stick
AT83C51RD2-RLTUM	ROM 64k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	VQFP44	Tray
AT83C51RD2-3CSUL	ROM 64k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PLCC44	Stick
AT83C51RD2-SLSUL	ROM 64k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	VQFP44	Tray
AT83C51RD2-RLTUL	ROM 64k Bytes	5V	Industrial & Green	40 MHz (30 MHz X2)	PDIL40	Stick

13.2 PDIL40



	MM		INCH	
A	-	5.08	-	.200
A1	0.38	-	.015	-
A2	3.18	4.95	.125	.195
B	0.36	0.56	.014	.022
B1	0.76	1.78	.030	.070
C	0.20	0.38	.008	.015
D	50.29	53.21	1.980	2.095
E	15.24	15.87	.600	.625
E1	12.32	14.73	.485	.580
e	2.54	B. S. C	.100	B. S. C
eA	15.24	B. S. C	.600	B. S. C
eB	-	17.78	-	.700
L	2.93	3.81	.115	.150
D1	0.13	-	.005	-
PKG STD		02		



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