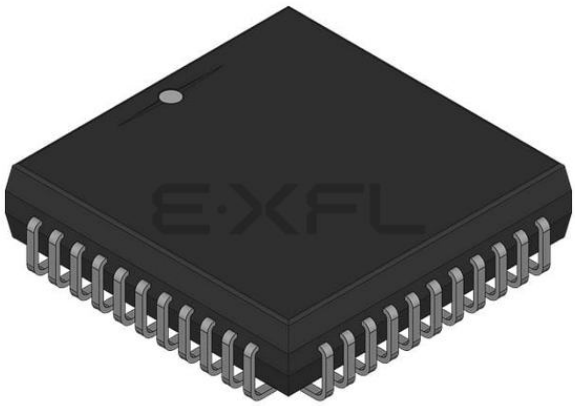

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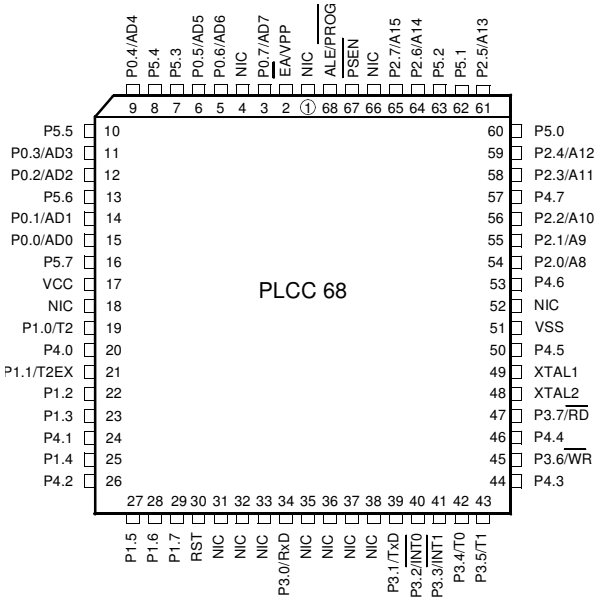
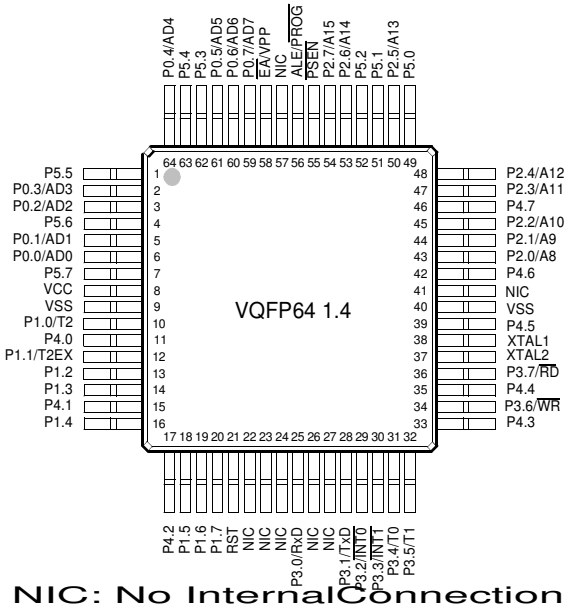
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 80C51 |
| Core Size | 8-Bit |
| Speed | 40/20MHz |
| Connectivity | UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 32 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC (16.6x16.6) |
| Purchase URL | https://www.e-xfl.com/product-detail/atmel/at87c51rc2-slsum |




NIC: No Internal Connection

| | | |
|---|---|---|
| PSEN | 67 | 55 |
| $\overline{EA}$/VPP | 2 | 58 |
| XTAL1 | 49 | 38 |
| XTAL2 | 48 | 37 |
| P4.0 | 20 | 11 |
| P4.1 | 24 | 15 |
| P4.2 | 26 | 17 |
| P4.3 | 44 | 33 |
| P4.4 | 46 | 35 |
| P4.5 | 50 | 39 |
| P4.6 | 53 | 42 |
| P4.7 | 57 | 46 |
| P5.0 | 60 | 49 |
| P5.1 | 62 | 51 |
| P5.2 | 63 | 52 |
| P5.3 | 7 | 62 |
| P5.4 | 8 | 63 |
| P5.5 | 10 | 1 |
| P5.6 | 13 | 4 |
| P5.7 | 16 | 7 |

## 6.1 Expanded RAM (XRAM)

The TS80C51Rx2 provide additional Bytes of ramdom access memory (RAM) space for increased data parameter handling and high level language usage.

RA2, RB2 and RC2 devices have 256 bytes of expanded RAM, from 00H to FFH in external data space; RD2 devices have 768 bytes of expanded RAM, from 00H to 2FFH in external data space.

The TS80C51Rx2 has internal data memory that is mapped into four separate segments.

The four segments are:

- 1. The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
- 2. The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
- 3. The Special Function Registers, SFRs, (addresses 80H to FFH) are directly addressable only.
- 4. The expanded RAM bytes are indirectly accessed by MOVX instructions, and with the EXTRAM bit cleared in the AUXR register. (See Table 6-1.)

The Lower 128 bytes can be accessed by either direct or indirect addressing. The Upper 128 bytes can be accessed by indirect addressing only. The Upper 128 bytes occupy the same address space as the SFR. That means they have the same address, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of data RAM or to SFR space by the addressing mode used in the instruction.

- Instructions that use direct addressing access SFR space. **For example: MOV 0A0H, # data**, accesses the SFR at location 0A0H (which is P2).
- Instructions that use indirect addressing access the Upper 128 bytes of data RAM. **For example: MOV @R0, # data** where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).
- The 256 or 768 XRAM bytes can be accessed by indirect addressing, with EXTRAM bit cleared and MOVX instructions. This part of memory which is physically located on-chip, logically occupies the first 256 or 768 bytes of external data memory.
- With EXTRAM = 0, the XRAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. **An access to XRAM will not affect ports P0, P2, P3.6 (WR) and P3.7 (RD)**. **For example, with EXTRAM = 0, MOVX @R0, # data** where R0 contains 0A0H, accesses the XRAM at address 0A0H rather than external memory. An access to external data memory locations higher than FFH (i.e. 0100H to FFFFH) (higher than 2FFH (i.e. 0300H to FFFFH for RD devices) will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51, so with P0 and P2 as data/address busses, and P3.6 and P3.7 as write and read timing signals. Refer to Figure 6-1. For RD devices, accesses to expanded RAM from 100H to 2FFH can only be done thanks to the use of DPTR.
- With EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 80C51. MOVX @ Ri will provide an eight-bit address multiplexed with data on Port0 and any output port pins can be used to output higher order address bits. This is to provide the external paging capability. MOVX @DPTR will generate a sixteen-bit address. Port2 outputs the high-order eight address bits (the contents of DPH) while Port0 multiplexes the low-order eight

## 6.2 Timer 2

The timer 2 in the TS80C51RX2 is compatible with the timer 2 in the 80C52.
It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 6-2) and T2MOD register (See Table 6-3). Timer 2 operation is similar to Timer 0 and Timer 1. C/$\overline{T2}$ selects $F_{OSC}/12$ (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/$\overline{RL2}$ (T2CON), as described in the Atmel 8-bit Microcontroller Hardware description.

Refer to the Atmel 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C51RX2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

### 6.2.1 Auto-reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 6-2. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | TF2 | **Timer 2 overflow Flag**<br>Must be cleared by software.<br>Set by hardware on timer 2 overflow, if RCLK = 0 and TCLK = 0. |
| 6 | EXF2 | **Timer 2 External Flag**<br>Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1.<br>When set, causes the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled.<br>Must be cleared by software. EXF2 doesn't cause an interrupt in Up/down counter mode (DCEN = 1) |
| 5 | RCLK | **Receive Clock bit**<br>Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3.<br>Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3. |
| 4 | TCLK | **Transmit Clock bit**<br>Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3.<br>Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3. |
| 3 | EXEN2 | **Timer 2 External Enable bit**<br>Clear to ignore events on T2EX pin for timer 2 operation.<br>Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port. |
| 2 | TR2 | **Timer 2 Run control bit**<br>Clear to turn off timer 2.<br>Set to turn on timer 2. |
| 1 | C/T2# | **Timer/Counter 2 select bit**<br>Clear for timer operation (input from internal clock system: $F_{OSC}$).<br>Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode. |
| 0 | CP/RL2# | **Timer 2 Capture/Reload bit**<br>If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to auto-reload on timer 2 overflow.<br>Clear to auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1.<br>Set to capture on negative transitions on T2EX pin if EXEN2=1. |

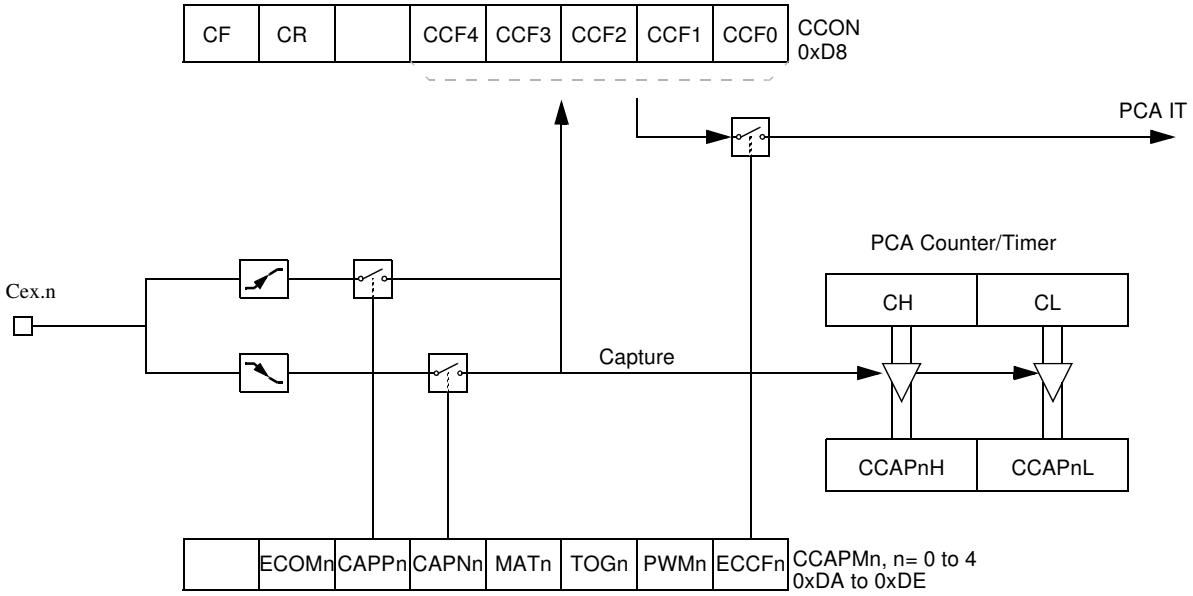
Reset Value = 0000 0000b
Bit addressable

**Table 6-3.** T2MOD Register

T2MOD - Timer 2 Mode Control Register (C9h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | - | - | - | T2OE | DCEN |

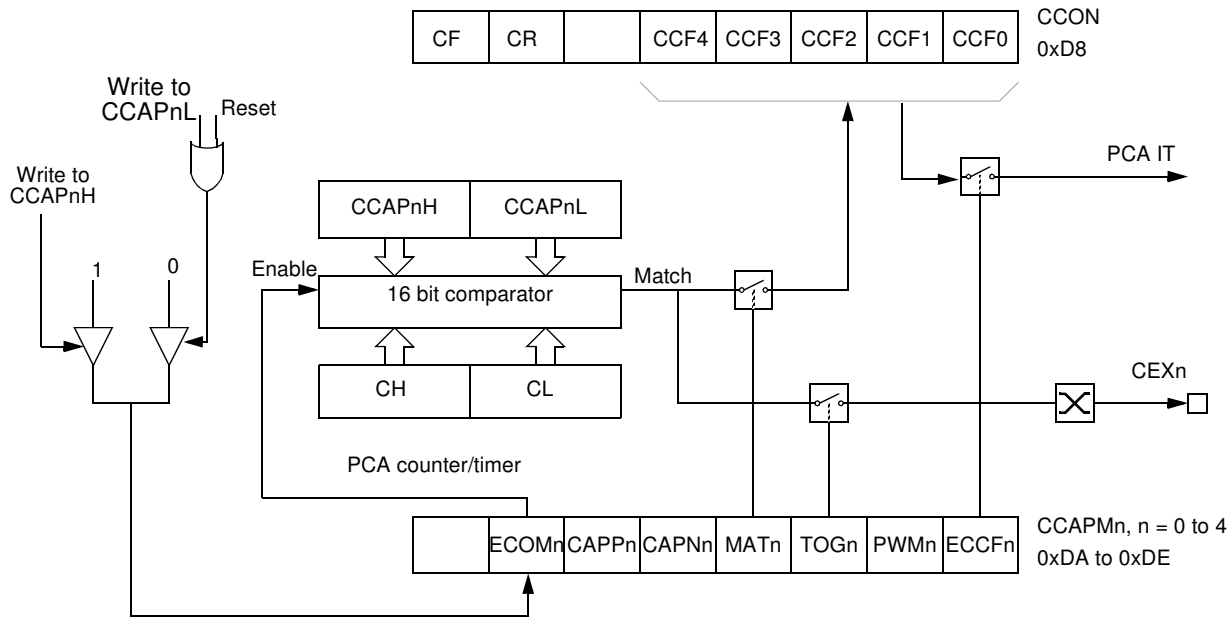
**Figure 6-6.** PCA Capture Mode




### 6.3.2 16-bit Software Timer/ Compare Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set (See Figure 6-7).

**Figure 6-8.** PCA High Speed Output Mode




Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.

### 6.3.4 Pulse Width Modulator Mode

All of the PCA modules can be used as PWM outputs. Figure 6-9 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn. This allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.

**Table 6-12.** SADEN - Slave Address Mask Register (B9h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

Reset Value = 0000 0000b
Not bit addressable

**Table 6-13.** SADDR - Slave Address Register (A9h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

Reset Value = 0000 0000b
Not bit addressable

**Table 6-14.** SCON Register
SCON - Serial Control Register (98h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **FE/SM0** | **SM1** | **SM2** | **REN** | **TB8** | **RB8** | **TI** | **RI** |

**Table 6-16.** Priority Level Bit Values

| IPH.x | IP.x | Interrupt Level Priority |
|---|---|---|
| 0 | 0 | 0 (Lowest) |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 (Highest) |

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

**Table 6-17.** IE Register

IE - Interrupt Enable Register (A8h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **EA** | **EC** | **ET2** | **ES** | **ET1** | **EX1** | **ET0** | **EX0** |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | EA | Enable All interrupt bit<br>Clear to disable all interrupts.<br>Set to enable all interrupts.<br>If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit. |
| 6 | EC | **PCA interrupt enable bit**<br>Clear to disable . Set to enable. |
| 5 | ET2 | Timer 2 overflow interrupt Enable bit<br>Clear to disable timer 2 overflow interrupt.<br>Set to enable timer 2 overflow interrupt. |
| 4 | ES | Serial port Enable bit<br>Clear to disable serial port interrupt.<br>Set to enable serial port interrupt. |
| 3 | ET1 | Timer 1 overflow interrupt Enable bit<br>Clear to disable timer 1 overflow interrupt.<br>Set to enable timer 1 overflow interrupt. |
| 2 | EX1 | External interrupt 1 Enable bit<br>Clear to disable external interrupt 1.<br>Set to enable external interrupt 1. |
| 1 | ET0 | Timer 0 overflow interrupt Enable bit<br>Clear to disable timer 0 overflow interrupt.<br>Set to enable timer 0 overflow interrupt. |
| 0 | EX0 | External interrupt 0 Enable bit<br>Clear to disable external interrupt 0.<br>Set to enable external interrupt 0. |

Reset Value = 0000 0000b

Bit addressable

**Table 6-18.** IP Register

IP - Interrupt Priority Register (B8h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | PPC | PT2 | PS | PT1 | PX1 | PT0 | PX0 |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 6 | PPC | **PCA interrupt priority bit**<br>Refer to PPCH for priority level. |
| 5 | PT2 | **Timer 2 overflow interrupt Priority bit**<br>Refer to PT2H for priority level. |
| 4 | PS | **Serial port Priority bit**<br>Refer to PSH for priority level. |
| 3 | PT1 | **Timer 1 overflow interrupt Priority bit**<br>Refer to PT1H for priority level. |
| 2 | PX1 | **External interrupt 1 Priority bit**<br>Refer to PX1H for priority level. |
| 1 | PT0 | **Timer 0 overflow interrupt Priority bit**<br>Refer to PT0H for priority level. |
| 0 | PX0 | **External interrupt 0 Priority bit**<br>Refer to PX0H for priority level. |

Reset Value = X000 0000b

Bit addressable

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | T4 | **Reserved**<br>Do not try to set or clear this bit. |
| 6 | T3 | |
| 5 | T2 | |
| 4 | T1 | |
| 3 | T0 | |
| 2 | S2 | WDT Time-out select bit 2 |
| 1 | S1 | WDT Time-out select bit 1 |
| 0 | S0 | WDT Time-out select bit 0 |
| | | S2 S1 S0Selected Time-out<br>0 0 0($2^{14}$ - 1) machine cycles, 16.3 ms @ 12 MHz<br>0 0 1($2^{15}$ - 1) machine cycles, 32.7 ms @ 12 MHz<br>0 1 0($2^{16}$ - 1) machine cycles, 65.5 ms @ 12 MHz<br>0 1 1($2^{17}$ - 1) machine cycles, 131 ms @ 12 MHz<br>1 0 0($2^{18}$ - 1) machine cycles, 262 ms @ 12 MHz<br>1 0 1($2^{19}$ - 1) machine cycles, 542 ms @ 12 MHz<br>1 1 0($2^{20}$ - 1) machine cycles, 1.05 s @ 12 MHz<br>1 1 1($2^{21}$ - 1) machine cycles, 2.09 s @ 12 MHz |

Reset value XXXX X000

### 6.8.2 WDT during Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode the user does not need to service the WDT. There are 2 methods of exiting Power-down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally should whenever the TS80C51Rx2 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service routine.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is best to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the TS80C51Rx2 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

## 6.9 ONCE™ Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS8xC51Rx2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C51Rx2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and $\overline{\text{PSEN}}$ is high.
- Hold ALE low as RST is deactivated.

While the TS80C51Rx2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 26. shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

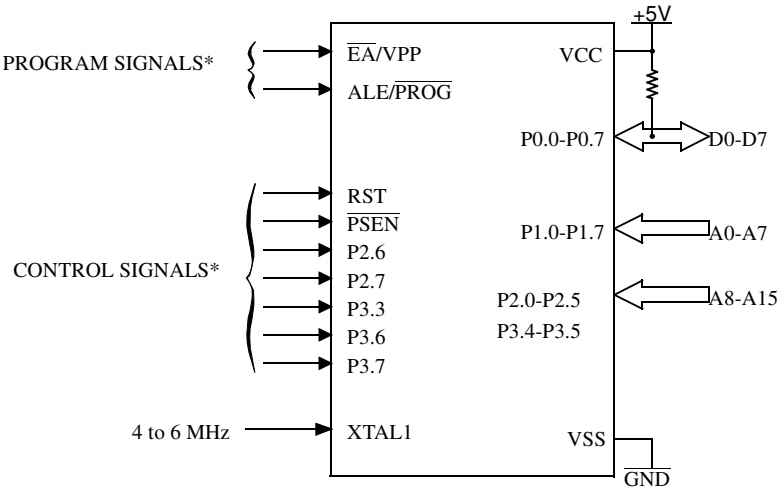
**Table 6-23.** External Pin Status during ONCE Mode

| ALE | PSEN | Port 0 | Port 1 | Port 2 | Port 3 | XTAL1/2 |
|---|---|---|---|---|---|---|
| Weak pull-up | Weak pull-up | Float | Weak pull-up | Weak pull-up | Weak pull-up | Active |

### 8.2.4 Verify Algorithm

Refer to Section “Verify algorithm”.

**Figure 9-1.** Set-Up Modes Configuration




* See Table 31. for proper value on these inputs

### 9.3.3 Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS87C51RB2/RC2/RD2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise $\overline{EA}$/VPP from VCC to VPP (typical 12.75V).
- Step 5: Pulse ALE/$\overline{PROG}$ once.
- Step 6: Lower $\overline{EA}$/VPP from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 9-2).

### 9.3.4 Verify algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C51RB2/RC2/RD2.

P 2.7 is used to enable data output.

To verify the TS87C51RB2/RC2/RD2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 9-2.)

**Table 11-1.** DC Parameters in Standard Voltage

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage, ports 1, 2, 3, 4, 5 | $V_{CC}$ - 0.3<br>$V_{CC}$ - 0.7<br>$V_{CC}$ - 1.5 | | | V<br>V<br>V | $I_{OH}$ = -10 µA<br>$I_{OH}$ = -30 µA<br>$I_{OH}$ = -60 µA<br>$V_{CC}$ = 5 V ± 10% |
| $V_{OH1}$ | Output High Voltage, port 0 | $V_{CC}$ - 0.3<br>$V_{CC}$ - 0.7<br>$V_{CC}$ - 1.5 | | | V<br>V<br>V | $I_{OH}$ = -200 µA<br>$I_{OH}$ = -3.2 mA<br>$I_{OH}$ = -7.0 mA<br>$V_{CC}$ = 5 V ± 10% |
| $V_{OH2}$ | Output High Voltage,ALE, $\overline{PSEN}$ | $V_{CC}$ - 0.3<br>$V_{CC}$ - 0.7<br>$V_{CC}$ - 1.5 | | | V<br>V<br>V | $I_{OH}$ = -100 µA<br>$I_{OH}$ = -1.6 mA<br>$I_{OH}$ = -3.5 mA<br>$V_{CC}$ = 5 V ± 10% |
| $R_{RST}$ | RST Pulldown Resistor | 50 | 90 (5) | 200 | kΩ | |
| $I_{IL}$ | Logical 0 Input Current ports 1, 2, 3, 4, 5 | | | -50 | µA | Vin = 0.45 V |
| $I_{LI}$ | Input Leakage Current | | | ±10 | µA | 0.45 V < Vin < $V_{CC}$ |
| $I_{TL}$ | Logical 1 to 0 Transition Current, ports 1, 2, 3, 4, 5 | | | -650 | µA | Vin = 2.0 V |
| $C_{IO}$ | Capacitance of I/O Buffer | | | 10 | pF | Fc = 1 MHz<br>$T_A$ = 25°C |
| $I_{PD}$ | Power-down Current | | 20(5) | 50 | µA | 2.0 V < $V_{CC}$ < 5.5 V(3) |
| $I_{CC}$ under RESET | Power Supply Current Maximum values, X1 mode: (7) | | | 1 + 0.4 Freq (MHz)<br>@12MHz 5.8<br>@16MHz 7.4 | mA | $V_{CC}$ = 5.5 V(1) |
| $I_{CC}$ operating | Power Supply Current Maximum values, X1 mode: (7) | | | 3 + 0.6 Freq (MHz)<br>@12MHz 10.2<br>@16MHz 12.6 | mA | $V_{CC}$ = 5.5 V(8) |
| $I_{CC}$ idle | Power Supply Current Maximum values, X1 mode: (7) | | | 0.25+0.3 Freq (MHz)<br>@12MHz 3.9<br>@16MHz 5.1 | mA | $V_{CC}$ = 5.5 V(2) |

## 11.4 DC Parameters for Low Voltage

$T_A$ = 0°C to +70°C; $V_{SS}$ = 0 V; $V_{CC}$ = 2.7 V to 5.5 V ± 10%; F = 0 to 30 MHz.
$T_A$ = -40°C to +85°C; $V_{SS}$ = 0 V; $V_{CC}$ = 2.7 V to 5.5 V ± 10%; F = 0 to 30 MHz.

**Table 11-2.** DC Parameters for Low Voltage

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.5 | | 0.2 $V_{CC}$ - 0.1 | V | |
| $V_{IH}$ | Input High Voltage except XTAL1, RST | 0.2 $V_{CC}$ + 0.9 | | $V_{CC}$ + 0.5 | V | |
| $V_{IH1}$ | Input High Voltage, XTAL1, RST | 0.7 $V_{CC}$ | | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage, ports 1, 2, 3, 4, 5 (6) | | | 0.45 | V | $I_{OL}$ = 0.8 mA(4) |
| $V_{OL1}$ | Output Low Voltage, port 0, ALE, $\overline{PSEN}$ (6) | | | 0.45 | V | $I_{OL}$ = 1.6 mA(4) |
| $V_{OH}$ | Output High Voltage, ports 1, 2, 3, 4, 5 | 0.9 $V_{CC}$ | | | V | $I_{OH}$ = -10 µA |
| $V_{OH1}$ | Output High Voltage, port 0, ALE, $\overline{PSEN}$ | 0.9 $V_{CC}$ | | | V | $I_{OH}$ = -40 µA |
| $I_{IL}$ | Logical 0 Input Current ports 1, 2, 3, 4, 5 | | | -50 | µA | Vin = 0.45 V |
| $I_{LI}$ | Input Leakage Current | | | ±10 | µA | 0.45 V < Vin < $V_{CC}$ |
| $I_{TL}$ | Logical 1 to 0 Transition Current, ports 1, 2, 3, 4, 5 | | | -650 | µA | Vin = 2.0 V |
| $R_{RST}$ | RST Pulldown Resistor | 50 | 90 (5) | 200 | kΩ | |
| CIO | Capacitance of I/O Buffer | | | 10 | pF | Fc = 1 MHz<br>$T_A$ = 25°C |
| $I_{PD}$ | Power-down Current | | 20 (5)<br>10 (5) | 50<br>30 | µA | $V_{CC}$ = 2.0 V to 5.5 V(3)<br>$V_{CC}$ = 2.0 V to 3.3 V(3) |
| $I_{PD}$ | Power-down Current (Only for TS87C51RD2 S287-xxx Very Low power) | | 2 (5) | 15 | µA | 2.0 V < $V_{CC}$ < 3.6 V(3) |
| $I_{CC}$ under RESET | Power Supply Current Maximum values, X1 mode: (7) | | | 1 + 0.2 Freq (MHz)<br>@12MHz 3.4<br>@16MHz 4.2 | mA | $V_{CC}$ = 3.3 V(1) |
| $I_{CC}$ operating | Power Supply Current Maximum values, X1 mode: (7) | | | 1 + 0.3 Freq (MHz)<br>@12MHz 4.6<br>@16MHz 5.8 | mA | $V_{CC}$ = 3.3 V(8) |
| $I_{CC}$ idle | Power Supply Current Maximum values, X1 mode: (7) | | | 0.15 Freq (MHz) + 0.2<br>@12MHz 2<br>@16MHz 2.6 | mA | $V_{CC}$ = 3.3 V(2) |

Notes:
1. $I_{CC}$ under reset is measured with all output pins disconnected; XTAL1 driven with $T_{CLCH}$, $T_{CHCL}$ = 5 ns (see Figure 11-5.), $V_{IL}$ = $V_{SS}$ + 0.5 V,
   $V_{IH}$ = $V_{CC}$ - 0.5V; XTAL2 N.C.; $\overline{EA}$ = RST = Port 0 = $V_{CC}$. $I_{CC}$ would be slightly higher if a crystal oscillator used..
2. Idle $I_{CC}$ is measured with all output pins disconnected; XTAL1 driven with $T_{CLCH}$, $T_{CHCL}$ = 5 ns, $V_{IL}$ = $V_{SS}$ + 0.5 V, $V_{IH}$ = $V_{CC}$ - 0.5 V; XTAL2 N.C; Port 0 = $V_{CC}$; $\overline{EA}$ = RST = $V_{SS}$ (see Figure 11-3.).
3. Power-down $I_{CC}$ is measured with all output pins disconnected; $\overline{EA}$ = $V_{SS}$, PORT 0 = $V_{CC}$; XTAL2 NC.; RST = $V_{SS}$ (see Figure 11-4.).

**Figure 11-3.** $I_{CC}$ Test Condition, Idle Mode

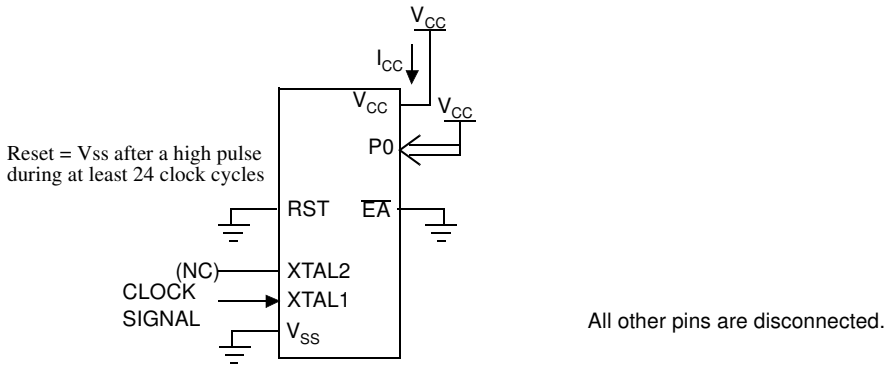



**Figure 11-4.** $I_{CC}$ Test Condition, Power-Down Mode

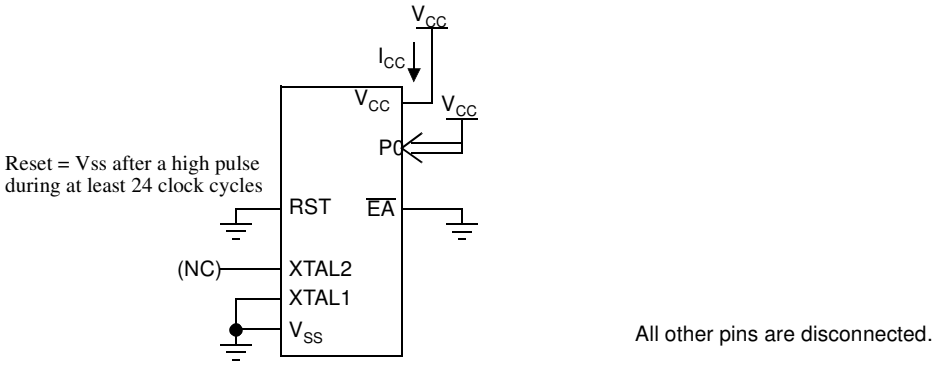
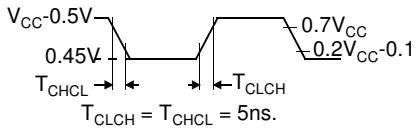



**Figure 11-5.** Clock Signal Waveform for $I_{CC}$ Tests in Active and Idle Modes




## 11.5 AC Parameters

### 11.5.1 Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example: $T_{AVLL}$ = Time for Address Valid to ALE Low.

$T_{LLPL}$ = Time for ALE Low to $\overline{PSEN}$ Low.

$T_A$ = 0 to +70°C (commercial temperature range); $V_{SS}$ = 0 V; $V_{CC}$ = 5 V ± 10%; -M and -V ranges.
$T_A$ = -40°C to +85°C (industrial temperature range); $V_{SS}$ = 0 V; $V_{CC}$ = 5 V ± 10%; -M and -V ranges.

## 12. Ordering Information

| Part Number | Memory size | Supply Voltage | Temperature Range | Max Frequency | Package | Packing |
|---|---|---|---|---|---|---|
| TS80C51RA2-MCA | OBSOLETE | | | | | |
| TS80C51RA2-MCB | | | | | | |
| TS80C51RA2-MCE | | | | | | |
| TS80C51RA2-MIA | | | | | | |
| TS80C51RA2-MIB | | | | | | |
| TS80C51RA2-MIE | | | | | | |
| TS80C51RA2-LCA | | | | | | |
| TS80C51RA2-LCB | | | | | | |
| TS80C51RA2-LCE | | | | | | |
| TS80C51RA2-LIA | | | | | | |
| TS80C51RA2-LIB | | | | | | |
| TS80C51RA2-LIE | | | | | | |
| TS80C51RA2-VCA | | | | | | |
| TS80C51RA2-VCB | | | | | | |
| TS80C51RA2-VCE | | | | | | |
| TS80C51RA2-VIA | | | | | | |
| TS80C51RA2-VIB | | | | | | |
| TS80C51RA2-VIE | | | | | | |
| | | | | | | |
| AT80C51RA2-3CSUM | Romless | 5V | Industrial & Green | 40 MHz (20 MHz X2) | PDIL40 | Stick |
| AT80C51RA2-SLSUM | Romless | 5V | Industrial & Green | 40 MHz (20 MHz X2) | PLCC44 | Stick |
| AT80C51RA2-RLTUM | Romless | 5V | Industrial & Green | 40 MHz (20 MHz X2) | VQFP44 | Tray |
| AT80C51RA2-3CSIM | OBSOLETE | | | | | |
| AT80C51RA2-SLSIM | | | | | | |
| AT80C51RA2-RLTIM | | | | | | |
| AT80C51RA2-3CSCL | | | | | | |
| AT80C51RA2-SLSCL | | | | | | |
| AT80C51RA2-RLTCL | | | | | | |
| AT80C51RA2-3CSUL | Romless | 3-5V | Industrial & Green | 30 MHz (20 MHz X2) | PDIL40 | Stick |
| AT80C51RA2-SLSUL | Romless | 3-5V | Industrial & Green | 30 MHz (20 MHz X2) | PLCC44 | Stick |
| AT80C51RA2-RLTUL | Romless | 3-5V | Industrial & Green | 30 MHz (20 MHz X2) | VQFP44 | Tray |

| Part Number | Memory size | Supply Voltage | Temperature Range | Max Frequency | Package | Packing |
|---|---|---|---|---|---|---|
| TS83C51RB2-MCA | OBSOLETE | | | | | |
| TS83C51RB2-MCB | | | | | | |
| TS83C51RB2-MCE | | | | | | |
| TS83C51RB2-MIA | | | | | | |
| TS83C51RB2-MIB | | | | | | |
| TS83C51RB2-MIE | | | | | | |
| TS83C51RB2-LCA | | | | | | |
| TS83C51RB2-LCB | | | | | | |
| TS83C51RB2-LCE | | | | | | |
| TS83C51RB2-LIA | | | | | | |
| TS83C51RB2-LIB | | | | | | |
| TS83C51RB2-LIE | | | | | | |
| TS83C51RB2-VCA | | | | | | |
| TS83C51RB2-VCB | | | | | | |
| TS83C51RB2-VCE | | | | | | |
| TS83C51RB2-VIA | | | | | | |
| TS83C51RB2-VIB | | | | | | |
| TS83C51RB2-VIE | | | | | | |
| | | | | | | |
| AT83C51RB2-3CSUM | ROM 32k Bytes | 5V | Industrial & Green | 40 MHz (20 MHz X2) | PDIL40 | Stick |
| AT83C51RB2-SLSUM | ROM 32k Bytes | 5V | Industrial & Green | 40 MHz (20 MHz X2) | PLCC44 | Stick |
| AT83C51RB2-RLTUM | ROM 32k Bytes | 5V | Industrial & Green | 40 MHz (20 MHz X2) | VQFP44 | Tray |
| AT83C51RB2-3CSUL | ROM 32k Bytes | 3-5V | Industrial & Green | 30 MHz (20 MHz X2) | PDIL40 | Stick |
| AT83C51RB2-SLSUL | ROM 32k Bytes | 3-5V | Industrial & Green | 30 MHz (20 MHz X2) | PLCC44 | Stick |
| AT83C51RB2-RLTUL | ROM 32k Bytes | 3-5V | Industrial & Green | 30 MHz (20 MHz X2) | VQFP44 | Tray |

| Part Number | Memory size | Supply Voltage | Temperature Range | Max Frequency | Package | Packing |
|---|---|---|---|---|---|---|
| TS83C51RD2-MCA | OBSOLETE | | | | | |
| TS83C51RD2-MCB | | | | | | |
| TS83C51RD2-MCE | | | | | | |
| TS83C51RD2-MIA | | | | | | |
| TS83C51RD2-MIB | | | | | | |
| TS83C51RD2-MIE | | | | | | |
| TS83C51RD2-LCB | | | | | | |
| TS83C51RD2-LCE | | | | | | |
| TS83C51RD2-LIA | | | | | | |
| TS83C51RD2-LIB | | | | | | |
| TS83C51RD2-LIE | | | | | | |
| TS83C51RD2-VCA | | | | | | |
| TS83C51RD2-VCB | | | | | | |
| TS83C51RD2-VCE | | | | | | |
| TS83C51RD2-VIA | | | | | | |
| TS83C51RD2-VIB | | | | | | |
| TS83C51RD2-VIE | | | | | | |
| | | | | | | |
| AT83C51RD2-3CSUM | ROM 64k Bytes | 5V | Industrial & Green | 40 MHz (20 MHz X2) | PDIL40 | Stick |
| AT83C51RD2-SLSUM | ROM 64k Bytes | 5V | Industrial & Green | 40 MHz (20 MHz X2) | PLCC44 | Stick |
| AT83C51RD2-RLTUM | ROM 64k Bytes | 5V | Industrial & Green | 40 MHz (20 MHz X2) | VQFP44 | Tray |
| AT83C51RD2-3CSUL | ROM 64k Bytes | 3-5V | Industrial & Green | 30 MHz (20 MHz X2) | PLCC44 | Stick |
| AT83C51RD2-SLSUL | ROM 64k Bytes | 3-5V | Industrial & Green | 30 MHz (20 MHz X2) | VQFP44 | Tray |
| AT83C51RD2-RLTUL | ROM 64k Bytes | 5V | Industrial & Green | 40 MHz (30 MHz X2) | PDIL40 | Stick |