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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 80C51 |
| Core Size | 8-Bit |
| Speed | 30/20MHz |
| Connectivity | UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 48 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/at87c51rd2-rdtul |

facilitates multiprocessor communication (EUART) and an X2 speed improvement mechanism.

The fully static design of the TS80C51Rx2 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The TS80C51Rx2 has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the timers, the serial port and the interrupt system are still operating. In the power-down mode the RAM is saved and all other functions are inoperative.

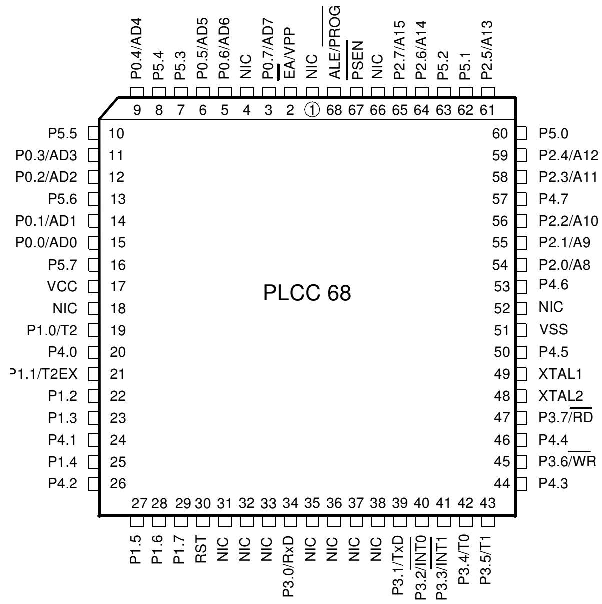
| PDIL40 PLCC44 VQFP44 1.4 | ROM (bytes) | EPROM (bytes) | XRAM (bytes) | TOTAL RAM (bytes) | I/O |
|---|---|---|---|---|---|
| TS80C51RA2 | 0 | 0 | 256 | 512 | 32 |
| TS80C51RD2 | 0 | 0 | 768 | 1024 | 32 |
| TS83C51RB2 | 16k | 0 | 256 | 512 | 32 |
| TS83C51RC2 | 32k | 0 | 256 | 512 | 32 |
| TS83C51RD2 | 64k | 0 | 768 | 1024 | 32 |
| TS87C51RB2 | 0 | 16k | 256 | 512 | 32 |
| TS87C51RC2 | 0 | 32k | 256 | 512 | 32 |
| TS87C51RD2 | 0 | 64k | 768 | 1024 | 32 |

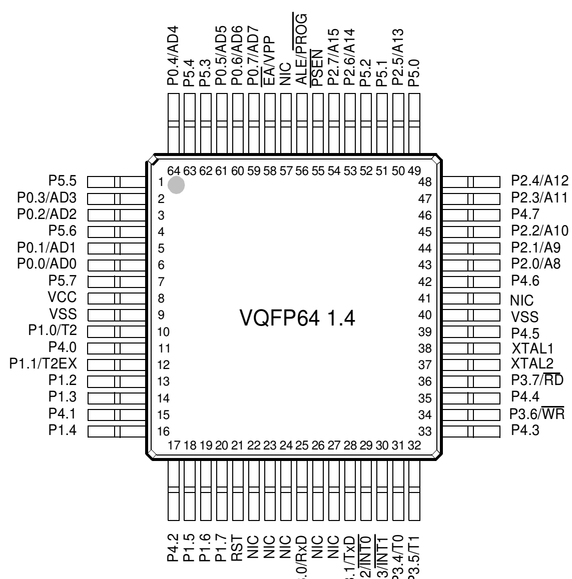
| PLCC68 VQFP64 1.4 | ROM (bytes) | EPROM (bytes) | XRAM (bytes) | TOTAL RAM (bytes) | I/O |
|---|---|---|---|---|---|
| TS80C51RD2 | 0 | 0 | 768 | 1024 | 48 |
| TS83C51RD2 | 64k | 0 | 768 | 1024 | 48 |
| TS87C51RD2 | 0 | 64k | 768 | 1024 | 48 |

# 4. SFR Mapping

The Special Function Registers (SFRs) of the TS80C51Rx2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3, P4, P5
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- HDW Watchdog Timer Reset: WDTRST, WDTPRG
- PCA registers: CL, CH, CCAPiL, CCAPiH, CCON, CMOD, CCAPMi
- Interrupt system registers: IE, IP, IPH
- Others: AUXR, CKCON




NIC: No InternalConnection

| | | |
|---|---|---|
| P0.0 | 15 | 6 |
| P0.1 | 14 | 5 |
| P0.2 | 12 | 3 |
| P0.3 | 11 | 2 |
| P0.4 | 9 | 64 |
| P0.5 | 6 | 61 |
| P0.6 | 5 | 60 |
| P0.7 | 3 | 59 |
| P1.0 | 19 | 10 |
| P1.1 | 21 | 12 |
| P1.2 | 22 | 13 |
| P1.3 | 23 | 14 |
| P1.4 | 25 | 16 |
| P1.5 | 27 | 18 |
| P1.6 | 28 | 19 |
| P1.7 | 29 | 20 |
| P2.0 | 54 | 43 |
| P2.1 | 55 | 44 |
| P2.2 | 56 | 45 |
| P2.3 | 58 | 47 |
| P2.4 | 59 | 48 |
| P2.5 | 61 | 50 |
| P2.6 | 64 | 53 |
| P2.7 | 65 | 54 |
| P3.0 | 34 | 25 |
| P3.1 | 39 | 28 |

| Pin | PLCC68 | SQUARE VQFP64 1.4 |
|---|---|---|
| P3.2 | 40 | 29 |
| P3.3 | 41 | 30 |
| P3.4 | 42 | 31 |
| P3.5 | 43 | 32 |
| P3.6 | 45 | 34 |
| P3.7 | 47 | 36 |
| RESET | 30 | 21 |
| ALE/$\overline{\text{PROG}}$ | 68 | 56 |

## 6.1 Expanded RAM (XRAM)

The TS80C51Rx2 provide additional Bytes of ramdom access memory (RAM) space for increased data parameter handling and high level language usage.

RA2, RB2 and RC2 devices have 256 bytes of expanded RAM, from 00H to FFH in external data space; RD2 devices have 768 bytes of expanded RAM, from 00H to 2FFH in external data space.

The TS80C51Rx2 has internal data memory that is mapped into four separate segments.

The four segments are:

- 1. The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
- 2. The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
- 3. The Special Function Registers, SFRs, (addresses 80H to FFH) are directly addressable only.
- 4. The expanded RAM bytes are indirectly accessed by MOVX instructions, and with the EXTRAM bit cleared in the AUXR register. (See Table 6-1.)

The Lower 128 bytes can be accessed by either direct or indirect addressing. The Upper 128 bytes can be accessed by indirect addressing only. The Upper 128 bytes occupy the same address space as the SFR. That means they have the same address, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of data RAM or to SFR space by the addressing mode used in the instruction.

- Instructions that use direct addressing access SFR space. **For example: MOV 0A0H, # data**, accesses the SFR at location 0A0H (which is P2).
- Instructions that use indirect addressing access the Upper 128 bytes of data RAM. **For example: MOV @R0, # data** where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).
- The 256 or 768 XRAM bytes can be accessed by indirect addressing, with EXTRAM bit cleared and MOVX instructions. This part of memory which is physically located on-chip, logically occupies the first 256 or 768 bytes of external data memory.
- With EXTRAM = 0, the XRAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. **An access to XRAM will not affect ports P0, P2, P3.6 ($\overline{\text{WR}}$) and P3.7 ($\overline{\text{RD}}$). For example, with EXTRAM = 0, MOVX @R0, # data** where R0 contains 0A0H, accesses the XRAM at address 0A0H rather than external memory. An access to external data memory locations higher than FFH (i.e. 0100H to FFFFH) (higher than 2FFH (i.e. 0300H to FFFFH for RD devices) will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51, so with P0 and P2 as data/address busses, and P3.6 and P3.7 as write and read timing signals. Refer to Figure 6-1. For RD devices, accesses to expanded RAM from 100H to 2FFH can only be done thanks to the use of DPTR.
- With EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 80C51. MOVX @ Ri will provide an eight-bit address multiplexed with data on Port0 and any output port pins can be used to output higher order address bits. This is to provide the external paging capability. MOVX @DPTR will generate a sixteen-bit address. Port2 outputs the high-order eight address bits (the contents of DPH) while Port0 multiplexes the low-order eight

## 6.2 Timer 2

The timer 2 in the TS80C51RX2 is compatible with the timer 2 in the 80C52.

It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 6-2) and T2MOD register (See Table 6-3). Timer 2 operation is similar to Timer 0 and Timer 1. C/$\overline{T2}$ selects $F_{OSC}/12$ (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/$\overline{RL2}$ (T2CON), as described in the Atmel 8-bit Microcontroller Hardware description.

Refer to the Atmel 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C51RX2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

### 6.2.1 Auto-reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 6-2. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.

It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.

**Figure 6-3.** Clock-Out Mode $C/\overline{T2} = 0$

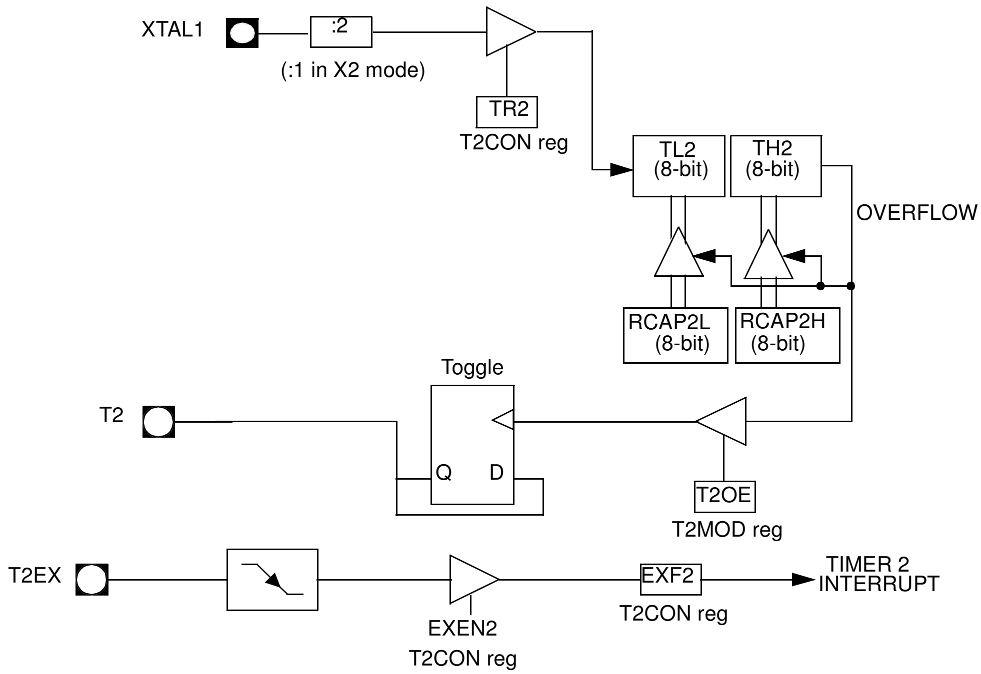



**Table 6-2.** T2CON Register
T2CON - Timer 2 Control Register (C8h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | C/T2# | CP/RL2# |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | TF2 | **Timer 2 overflow Flag**<br>Must be cleared by software.<br>Set by hardware on timer 2 overflow, if RCLK = 0 and TCLK = 0. |
| 6 | EXF2 | **Timer 2 External Flag**<br>Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1.<br>When set, causes the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled.<br>Must be cleared by software. EXF2 doesn't cause an interrupt in Up/down counter mode (DCEN = 1) |
| 5 | RCLK | **Receive Clock bit**<br>Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3.<br>Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3. |
| 4 | TCLK | **Transmit Clock bit**<br>Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3.<br>Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3. |
| 3 | EXEN2 | **Timer 2 External Enable bit**<br>Clear to ignore events on T2EX pin for timer 2 operation.<br>Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port. |
| 2 | TR2 | **Timer 2 Run control bit**<br>Clear to turn off timer 2.<br>Set to turn on timer 2. |
| 1 | C/T2# | **Timer/Counter 2 select bit**<br>Clear for timer operation (input from internal clock system: $F_{OSC}$).<br>Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode. |
| 0 | CP/RL2# | **Timer 2 Capture/Reload bit**<br>If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to auto-reload on timer 2 overflow.<br>Clear to auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1.<br>Set to capture on negative transitions on T2EX pin if EXEN2=1. |

Reset Value = 0000 0000b
Bit addressable

**Table 6-3.** T2MOD Register
T2MOD - Timer 2 Mode Control Register (C9h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | - | - | - | T2OE | DCEN |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 4 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 3 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 2 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 1 | T2OE | **Timer 2 Output Enable bit**<br>Clear to program P1.0/T2 as clock input or I/O port.<br>Set to program P1.0/T2 as clock output. |
| 0 | DCEN | **Down Counter Enable bit**<br>Clear to disable timer 2 as up/down counter.<br>Set to enable timer 2 as up/down counter. |

Reset Value = XXXX XX00b
Not bit addressable

• The CIDL bit which allows the PCA to stop during idle mode.
• The WDTE bit which enables or disables the watchdog function on module 4.
• The ECF bit which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows.

**The CCON SFR** contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (Refer to Table 6-5).

• Bit CR (CCON.6) must be set by software to run the PCA. The PCA is shut off by clearing this bit.
• Bit CF: The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software.
• Bits 0 through 4 are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software.

**Table 6-5.** CCON: PCA Counter Control Register

| CCON Address 0D8H | CF | CR | - | CCF4 | CCF3 | CCF2 | CCF1 | CCF0 |
|---|---|---|---|---|---|---|---|---|
| Reset value | 0 | 0 | X | 0 | 0 | 0 | 0 | 0 |

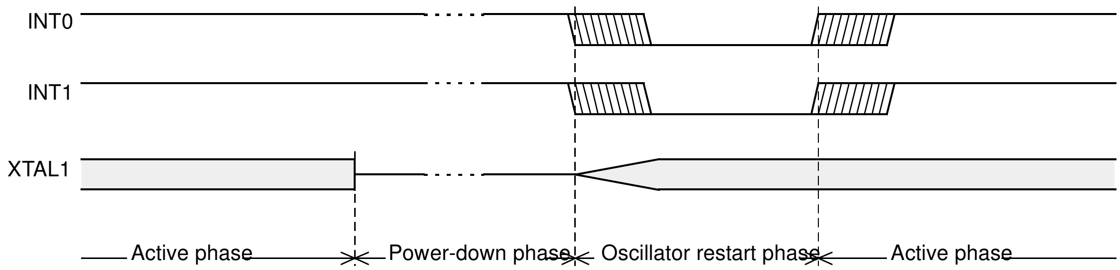
| Symbol | Function |
|---|---|
| CF | PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software. |
| CR | PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off. |
| - | Not implemented, reserved for future use. (1) |
| CCF4 | PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software. |
| CCF3 | PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software. |
| CCF2 | PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software. |
| CCF1 | PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software. |
| CCF0 | PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software. |

1. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

**The watchdog timer** function is implemented in module 4 (See Figure 6-7).

**The PCA interrupt** system is shown in Figure 6-5.

**Figure 6-14.** Power-Down Exit Waveform




Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

Note: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

**Table 6-20.** The state of ports during idle and power-down mode

| Mode | Program Memory | ALE | PSEN | PORT0 | PORT1 | PORT2 | PORT3 |
|---|---|---|---|---|---|---|---|
| Idle | Internal | 1 | 1 | Port Data* | Port Data | Port Data | Port Data |
| Idle | External | 1 | 1 | Floating | Port Data | Address | Port Data |
| Power-down | Internal | 0 | 0 | Port Data* | Port Data | Port Data | Port Data |
| Power-down | External | 0 | 0 | Floating | Port Data | Port Data | Port Data |

* Port 0 can force a "zero" level. A "one" will leave port floating.

## 6.9 ONCE™ Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS8xC51Rx2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C51Rx2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and $\overline{\text{PSEN}}$ is high.
- Hold ALE low as RST is deactivated.

While the TS80C51Rx2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 26. shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

**Table 6-23.** External Pin Status during ONCE Mode

| ALE | PSEN | Port 0 | Port 1 | Port 2 | Port 3 | XTAL1/2 |
|---|---|---|---|---|---|---|
| Weak pull-up | Weak pull-up | Float | Weak pull-up | Weak pull-up | Weak pull-up | Active |

## 7.1 Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

**Table 7-2.** AUXR Register
AUXR - Auxiliary Register (8Eh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | - | - | - | EXTRAM | AO |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 4 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 3 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 2 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 1 | EXTRAM | **EXTRAM bit**<br>See Table 6-1. |
| 0 | AO | **ALE Output bit**<br>Clear to restore ALE operation during internal fetches.<br>Set to disable ALE operation during internal fetches. |

Reset Value = XXXX XX00b
Not bit addressable

# 9. TS87C51RB2/RC2/RD2 EPROM

## 9.1 EPROM Structure

The TS87C51RB2/RC2/RD2 EPROM is divided in two different arrays:

- the code array:16/32/64 Kbytes.
- the encryption array:64 bytes.

In addition a third non programmable array is implemented:

- the signature array: 4 bytes.

## 9.2 EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

### 9.2.1 Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

### 9.2.2 Program Lock Bits

The three lock bits, when programmed according to Table 9-1.9.2.3, will provide different level of protection for the on-chip code and data.

**Table 9-1.** Program Lock bits

| Program Lock Bits | | | | |
|---|---|---|---|---|
| Security level | LB1 | LB2 | LB3 | Protection Description |
| 1 | U | U | U | No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data. |
| 2 | P | U | U | MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the EPROM is disabled. |
| 3 | U | P | U | Same as 2, also verify is disabled. |
| 4 | U | U | P | Same as 3, also external execution is disabled. |

U: unprogrammed,
P: programmed

### 11.5.2 External Program Memory Characteristics

**Table 11-5.** Symbol Description

| Symbol | Parameter |
|---|---|
| T | Oscillator clock period |
| $T_{LHLL}$ | ALE pulse width |
| $T_{AVLL}$ | Address Valid to ALE |
| $T_{LLAX}$ | Address Hold After ALE |
| $T_{LLIV}$ | ALE to Valid Instruction In |
| $T_{LLPL}$ | ALE to $\overline{PSEN}$ |
| $T_{PLPH}$ | $\overline{PSEN}$ Pulse Width |
| $T_{PLIV}$ | $\overline{PSEN}$ to Valid Instruction In |
| $T_{PXIX}$ | Input Instruction Hold After $\overline{PSEN}$ |
| $T_{PXIZ}$ | Input Instruction FloatAfter $\overline{PSEN}$ |
| $T_{PXAV}$ | $\overline{PSEN}$ to Address Valid |
| $T_{AVIV}$ | Address to Valid Instruction In |
| $T_{PLAZ}$ | $\overline{PSEN}$ Low to Address Float |

**Table 11-6.** AC Parameters for Fix Clock

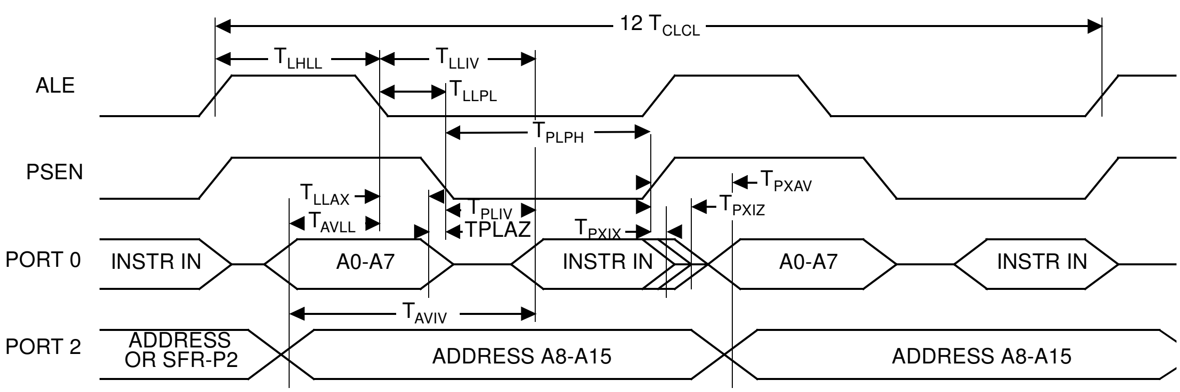
| Speed | -M 40 MHz | | -V X2 mode 30 MHz 60 MHz equiv. | | -V standard mode 40 MHz | | -L X2 mode 20 MHz 40 MHz equiv. | | -L standard mode 30 MHz | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| T | 25 | | 33 | | 25 | | 50 | | 33 | | ns |
| $T_{LHLL}$ | 40 | | 25 | | 42 | | 35 | | 52 | | ns |
| $T_{AVLL}$ | 10 | | 4 | | 12 | | 5 | | 13 | | ns |
| $T_{LLAX}$ | 10 | | 4 | | 12 | | 5 | | 13 | | ns |
| $T_{LLIV}$ | | 70 | | 45 | | 78 | | 65 | | 98 | ns |
| $T_{LLPL}$ | 15 | | 9 | | 17 | | 10 | | 18 | | ns |
| $T_{PLPH}$ | 55 | | 35 | | 60 | | 50 | | 75 | | ns |
| $T_{PLIV}$ | | 35 | | 25 | | 50 | | 30 | | 55 | ns |
| $T_{PXIX}$ | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $T_{PXIZ}$ | | 18 | | 12 | | 20 | | 10 | | 18 | ns |
| $T_{AVIV}$ | | 85 | | 53 | | 95 | | 80 | | 122 | ns |
| $T_{PLAZ}$ | | 10 | | 10 | | 10 | | 10 | | 10 | ns |

Table 11-7. AC Parameters for a Variable Clock: derating formula

| Symbol | Type | Standard Clock | X2 Clock | -M | -V | -L | Units |
|---|---|---|---|---|---|---|---|
| $T_{LHLL}$ | Min | 2 T - x | T - x | 10 | 8 | 15 | ns |
| $T_{AVLL}$ | Min | T - x | 0.5 T - x | 15 | 13 | 20 | ns |
| $T_{LLAX}$ | Min | T - x | 0.5 T - x | 15 | 13 | 20 | ns |
| $T_{LLIV}$ | Max | 4 T - x | 2 T - x | 30 | 22 | 35 | ns |
| $T_{LLPL}$ | Min | T - x | 0.5 T - x | 10 | 8 | 15 | ns |
| $T_{PLPH}$ | Min | 3 T - x | 1.5 T - x | 20 | 15 | 25 | ns |
| $T_{PLIV}$ | Max | 3 T - x | 1.5 T - x | 40 | 25 | 45 | ns |
| $T_{PXIX}$ | Min | x | x | 0 | 0 | 0 | ns |
| $T_{PXIZ}$ | Max | T - x | 0.5 T - x | 7 | 5 | 15 | ns |
| $T_{AVIV}$ | Max | 5 T - x | 2.5 T - x | 40 | 30 | 45 | ns |
| $T_{PLAZ}$ | Max | x | x | 10 | 10 | 10 | ns |

### 11.5.3 External Program Memory Read Cycle

Figure 11-6. External Program Memory Read Cycle

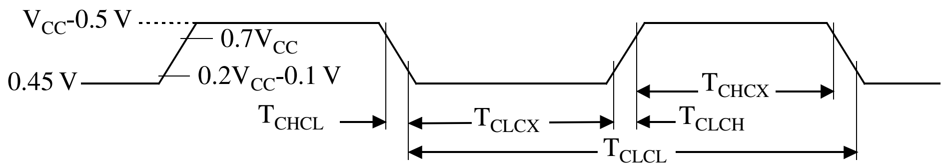


### 11.5.11 External Clock Drive Characteristics (XTAL1)

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{CLCL}$ | Oscillator Period | 25 | | ns |
| $T_{CHCX}$ | High Time | 5 | | ns |
| $T_{CLCX}$ | Low Time | 5 | | ns |
| $T_{CLCH}$ | Rise Time | | 5 | ns |
| $T_{CHCL}$ | Fall Time | | 5 | ns |
| $T_{CHCX}/T_{CLCX}$ | Cyclic ratio in X2 mode | 40 | 60 | % |

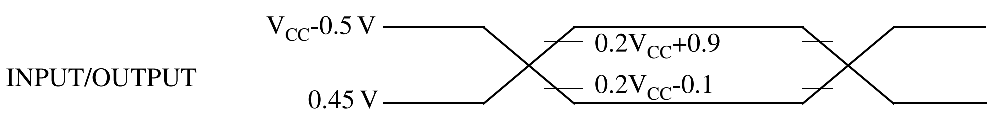
### 11.5.12 External Clock Drive Waveforms

**Figure 11-11.** External Clock Drive Waveforms




### 11.5.13 AC Testing Input/Output Waveforms

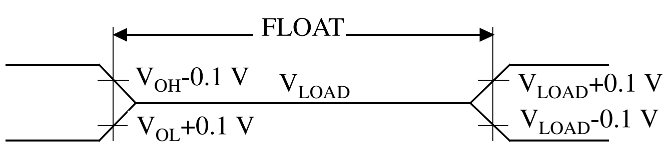
**Figure 11-12.** AC Testing Input/Output Waveforms




AC inputs during testing are driven at $V_{CC}$ - 0.5 for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at $V_{IH}$ min for a logic “1” and $V_{IL}$ max for a logic “0”.

### 11.5.14 Float Waveforms

**Figure 11-13.** Float Waveforms

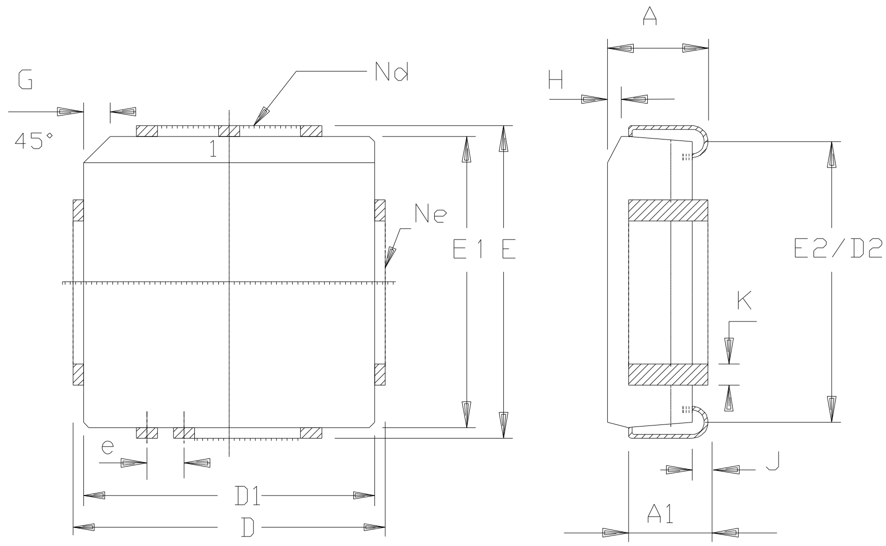



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded $V_{OH}/V_{OL}$ level occurs. $I_{OL}/I_{OH}$ $\geq \pm$ 20mA.

| Part Number | Memory size | Supply Voltage | Temperature Range | Max Frequency | Package | Packing |
|---|---|---|---|---|---|---|
| TS83C51RC2-MCA | OBSOLETE | | | | | |
| TS83C51RC2-MCB | | | | | | |
| TS83C51RC2-MCE | | | | | | |
| TS83C51RC2-MIA | | | | | | |
| TS83C51RC2-MIB | | | | | | |
| TS83C51RC2-MIE | | | | | | |
| TS83C51RC2-LCA | | | | | | |
| TS83C51RC2-LCB | | | | | | |
| TS83C51RC2-LCE | | | | | | |
| TS83C51RC2-LIA | | | | | | |
| TS83C51RC2-LIB | | | | | | |
| TS83C51RC2-LIE | | | | | | |
| TS83C51RC2-VCA | | | | | | |
| TS83C51RC2-VCB | | | | | | |
| TS83C51RC2-VCE | | | | | | |
| TS83C51RC2-VIA | | | | | | |
| TS83C51RC2-VIB | | | | | | |
| TS83C51RC2-VIE | | | | | | |
| | | | | | | |
| AT83C51RC2-3CSUM | ROM 32k Bytes | 5V | Industrial & Green | 40 MHz (20 MHz X2) | PDIL40 | Stick |
| AT83C51RC2-SLSUM | ROM 32k Bytes | 5V | Industrial & Green | 40 MHz (20 MHz X2) | PLCC44 | Stick |
| AT83C51RC2-RLTUM | ROM 32k Bytes | 5V | Industrial & Green | 40 MHz (20 MHz X2) | VQFP44 | Tray |
| AT83C51RC2-3CSUL | ROM 32k Bytes | 3-5V | Industrial & Green | 30 MHz (20 MHz X2) | PDIL40 | Stick |
| AT83C51RC2-SLSUL | ROM 32k Bytes | 3-5V | Industrial & Green | 30 MHz (20 MHz X2) | PLCC44 | Stick |
| AT83C51RC2-RLTUL | ROM 32k Bytes | 3-5V | Industrial & Green | 30 MHz (20 MHz X2) | VQFP44 | Tray |

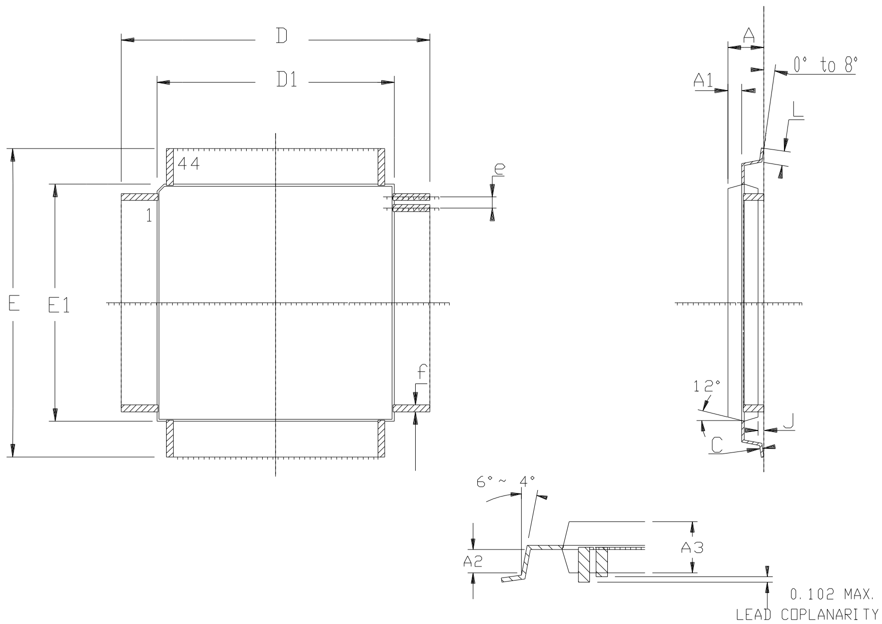
# 13. Package Drawings

## 13.1 PLCC44




| | MM | | INCH | |
|---|---|---|---|---|
| A | 4. 20 | 4. 57 | . 165 | . 180 |
| A1 | 2. 29 | 3. 04 | . 090 | . 120 |
| D | 17. 40 | 17. 65 | . 685 | . 695 |
| D1 | 16. 44 | 16. 66 | . 647 | . 656 |
| D2 | 14. 99 | 16. 00 | . 590 | . 630 |
| E | 17. 40 | 17. 65 | . 685 | . 695 |
| E1 | 16. 44 | 16. 66 | . 647 | . 656 |
| E2 | 14. 99 | 16. 00 | . 590 | . 630 |
| e | 1. 27 | BSC | . 050 | BSC |
| G | 1. 07 | 1. 22 | . 042 | . 048 |
| H | 1. 07 | 1. 42 | . 042 | . 056 |
| J | 0. 51 | - | . 020 | - |
| K | 0. 33 | 0. 53 | . 013 | . 021 |
| Nd | 11 | | 11 | |
| Ne | 11 | | 11 | |
| PKG STD | 00 | | | |

### 13.3 VQFP44




| | MM | | INCH | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | - | 1.60 | - | .063 |
| A1 | 0.64 REF | | .025 REF | |
| A2 | 0.64 REF | | .025 REF | |
| A3 | 1.35 | 1.45 | .053 | .057 |
| D | 11.90 | 12.10 | .468 | .476 |
| D1 | 9.90 | 10.10 | .390 | .398 |
| E | 11.90 | 12.10 | .468 | .476 |
| E1 | 9.90 | 10.10 | .390 | .398 |
| J | 0.05 | - | .002 | - |
| L | 0.45 | 0.75 | .018 | .030 |
| e | 0.80 BSC | | .0315 BSC | |
| f | 0.35 BSC | | .014 BSC | |