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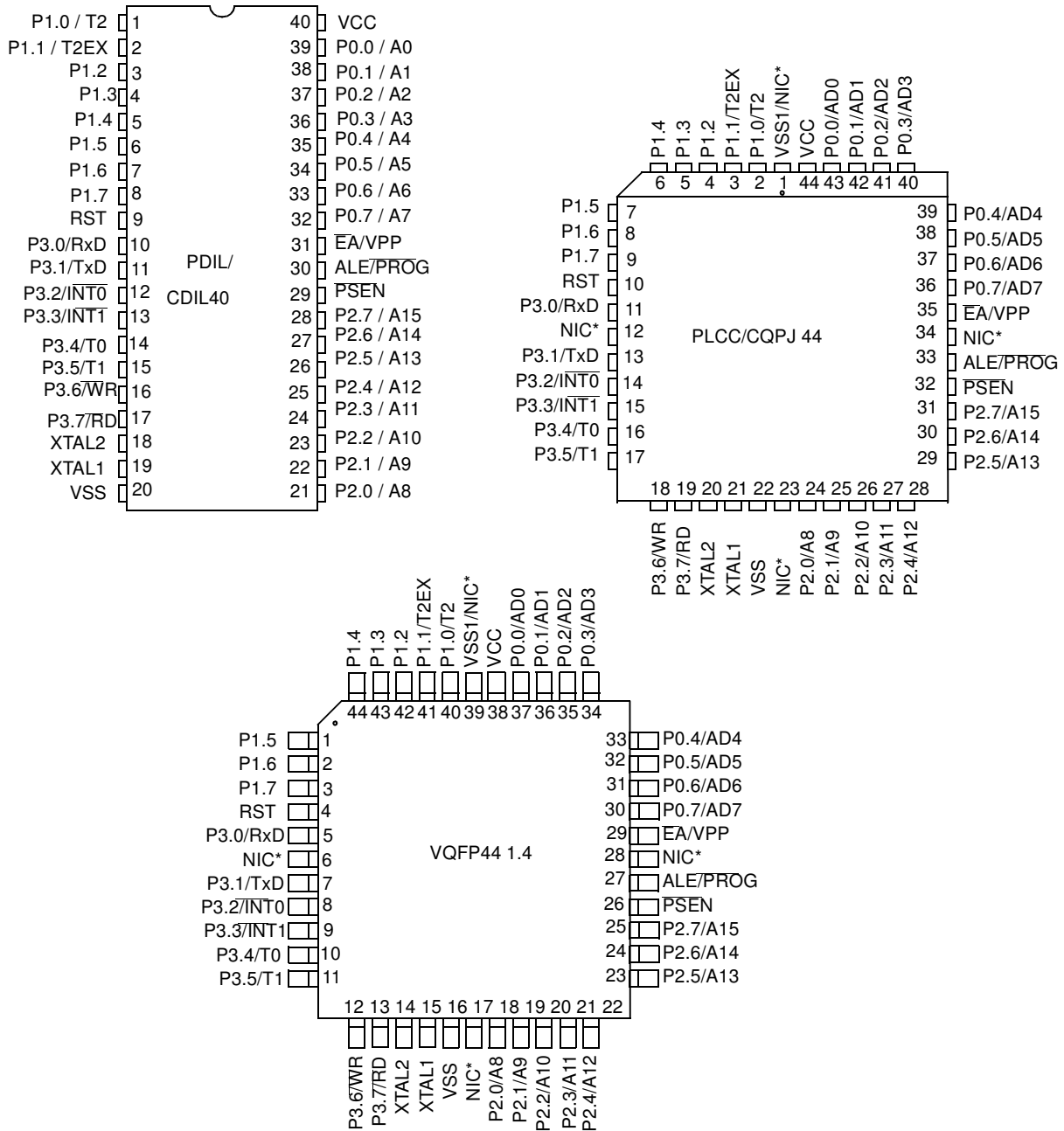
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	48
Program Memory Size	64KB (64K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at87c51rd2-rdtum

5. Pin Configuration



*NIC: No Internal Connection

Bit Number	Bit Mnemonic	Description
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	X2	CPU and peripheral clock bit Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$).

Reset Value = XXXX XXX0b

Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (<http://www.atmel.com>)

6.1 Expanded RAM (XRAM)

The TS80C51Rx2 provide additional Bytes of ramdom access memory (RAM) space for increased data parameter handling and high level language usage.

RA2, RB2 and RC2 devices have 256 bytes of expanded RAM, from 00H to FFH in external data space; RD2 devices have 768 bytes of expanded RAM, from 00H to 2FFH in external data space.

The TS80C51Rx2 has internal data memory that is mapped into four separate segments.

The four segments are:

- 1. The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
- 2. The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
- 3. The Special Function Registers, SFRs, (addresses 80H to FFH) are directly addressable only.
- 4. The expanded RAM bytes are indirectly accessed by MOVX instructions, and with the EXTRAM bit cleared in the AUXR register. (See Table 6-1.)

The Lower 128 bytes can be accessed by either direct or indirect addressing. The Upper 128 bytes can be accessed by indirect addressing only. The Upper 128 bytes occupy the same address space as the SFR. That means they have the same address, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of data RAM or to SFR space by the addressing mode used in the instruction.

- Instructions that use direct addressing access SFR space. **For example: MOV 0A0H, # data**, accesses the SFR at location 0A0H (which is P2).
- Instructions that use indirect addressing access the Upper 128 bytes of data RAM. **For example: MOV @R0, # data** where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).
- The 256 or 768 XRAM bytes can be accessed by indirect addressing, with EXTRAM bit cleared and MOVX instructions. This part of memory which is physically located on-chip, logically occupies the first 256 or 768 bytes of external data memory.
- With EXTRAM = 0, the XRAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. **An access to XRAM will not affect ports P0, P2, P3.6 (WR) and P3.7 (RD).** **For example, with EXTRAM = 0, MOVX @R0, # data** where R0 contains 0A0H, accesses the XRAM at address 0A0H rather than external memory. An access to external data memory locations higher than FFH (i.e. 0100H to FFFFH) (higher than 2FFH (i.e. 0300H to FFFFH for RD devices) will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51, so with P0 and P2 as data/address busses, and P3.6 and P3.7 as write and read timing signals. Refer to Figure 6-1. For RD devices, accesses to expanded RAM from 100H to 2FFH can only be done thanks to the use of DPTR.
- With EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 80C51. MOVX @ Ri will provide an eight-bit address multiplexed with data on Port0 and any output port pins can be used to output higher order address bits. This is to provide the external paging capability. MOVX @DPTR will generate a sixteen-bit address. Port2 outputs the high-order eight address bits (the contents of DPH) while Port0 multiplexes the low-order eight

6.2 Timer 2

The timer 2 in the TS80C51RX2 is compatible with the timer 2 in the 80C52.

It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 6-2) and T2MOD register (See Table 6-3). Timer 2 operation is similar to Timer 0 and Timer 1. $\overline{C}/T2$ selects $F_{OSC}/12$ (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and $CP/\overline{RL2}$ (T2CON), as described in the Atmel 8-bit Microcontroller Hardware description.

Refer to the Atmel 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C51RX2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

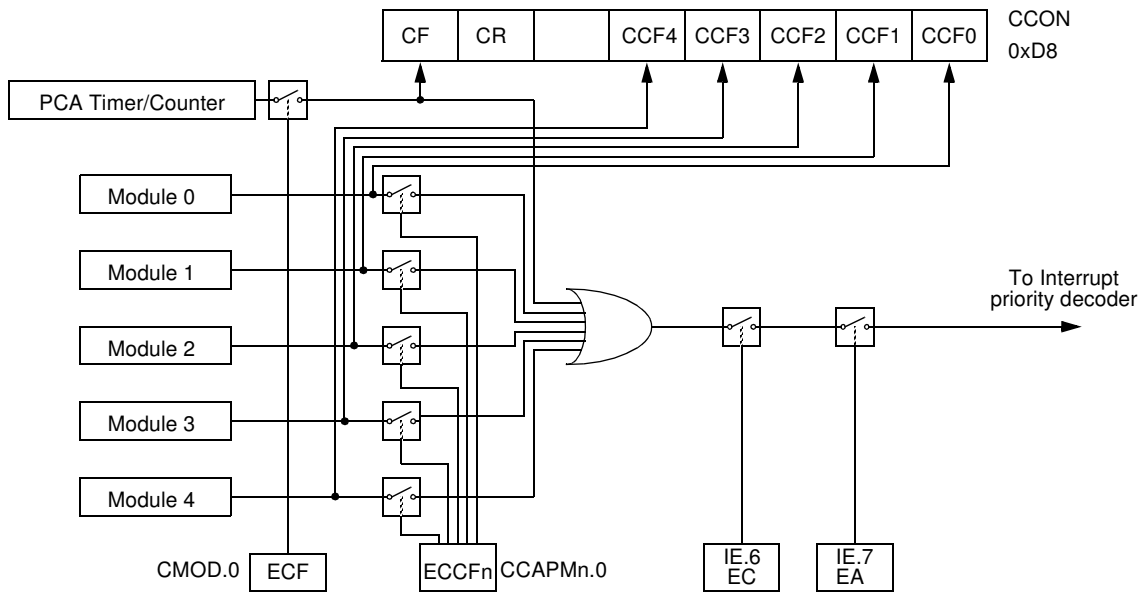
6.2.1 Auto-reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 6-2. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.

Figure 6-5. PCA Interrupt System


PCA Modules: each one of the five compare/capture modules has six possible functions. It can perform:

- 16-bit Capture, positive-edge triggered,
- 16-bit Capture, negative-edge triggered,
- 16-bit Capture, both positive and negative-edge triggered,
- 16-bit Software Timer,
- 16-bit High Speed Output,
- 8-bit Pulse Width Modulator.

In addition, module 4 can be used as a Watchdog Timer.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (See Table 6-6). The registers contain the bits that control the mode that each module will operate in.

- The ECCF bit (CCAPMn.0 where n=0, 1, 2, 3, or 4 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module.
- PWM (CCAPMn.1) enables the pulse width modulation mode.
- The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register.
- The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.
- The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output (See Table 6-8 & Table 6-9)

Table 6-8. CCAPnH: PCA Modules Capture/Compare Registers High

CCAPnH Address n = 0 - 4	CCAP0H=0FAH							
	CCAP1H=0FBH							
	CCAP2H=0FCH							
	CCAP3H=0FDH							
	CCAP4H=0FEH							
	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

Table 6-9. CCAPnL: PCA Modules Capture/Compare Registers Low

CCAPnL Address n = 0 - 4	CCAP0L=0EAH							
	CCAP1L=0EBH							
	CCAP2L=0ECH							
	CCAP3L=0EDH							
	CCAP4L=0EEH							
	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

Table 6-10. CH: PCA Counter High

CH Address 0F9H	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

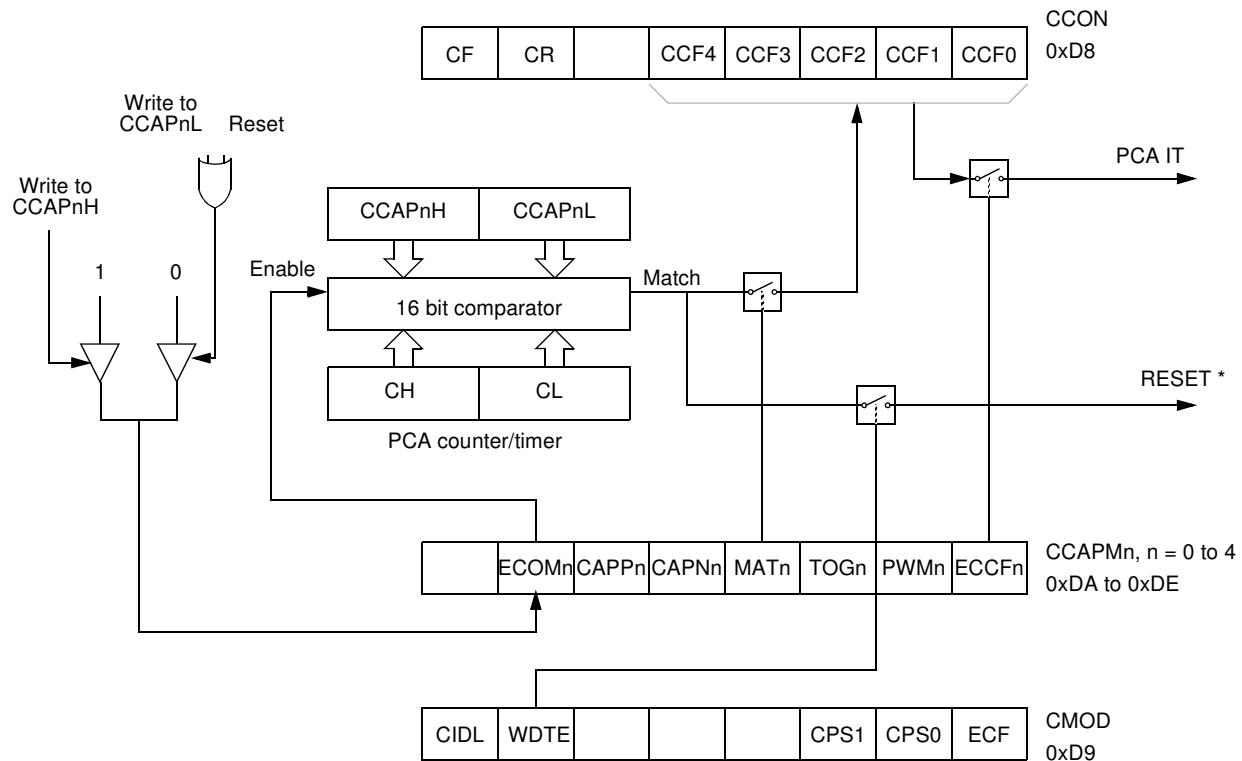
Table 6-11. CL: PCA Counter Low

CL Address 0E9H	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

6.3.1 PCA Capture Mode

To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated (Refer to Figure 6-6).

Figure 6-7. PCA Compare Mode and PCA Watchdog Timer



* Only for Module 4

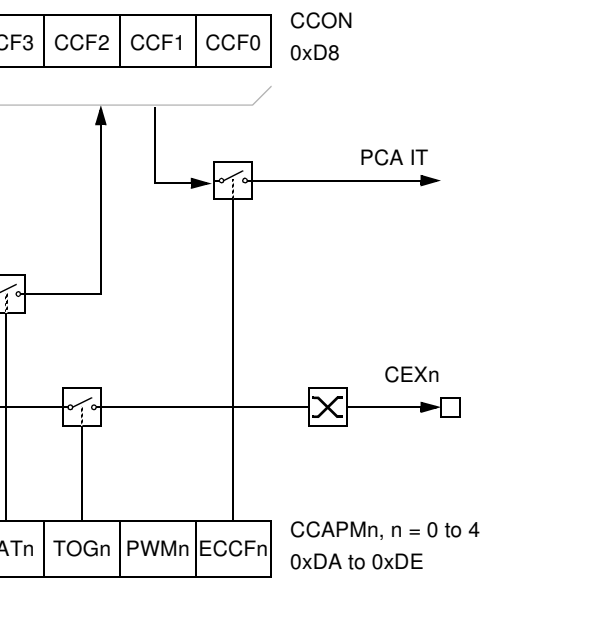
Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen. Writing to CCAPnH will set the ECOM bit.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.

6.3.3 High Speed Output Mode

In this mode the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (See Figure 6-8).

A prior write must be done to CCAPnL and CCAPnH before writing the ECOMn bit.



APnH should be set with a non zero value, other-

ECOM so that an unwanted match doesn't occur to CCAPnH will set ECOM. For this reason, user n CCAPnH. Of course, the ECOM bit can still be

outputs. Figure 6-9 shows the PWM function. The PCA timer is used for the PCA timer. All of the modules will have their own capture register CCAPL_n. The duty cycle of each module's capture register CCAPL_n. When the value of the module's CCAPL_n SFR the output will be low, and it will be high. When CL overflows from FF to 00, the output will be high. This allows updating the PWM without glitches. The CCAPM_n register must be set to enable the PWM

Bit Number	Bit Mnemonic	Description
7	SMOD1	Serial port Mode bit 1 Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	Serial port Mode bit 0 Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	POF	Power-Off Flag Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	Power-Down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	Idle mode bit Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b

Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

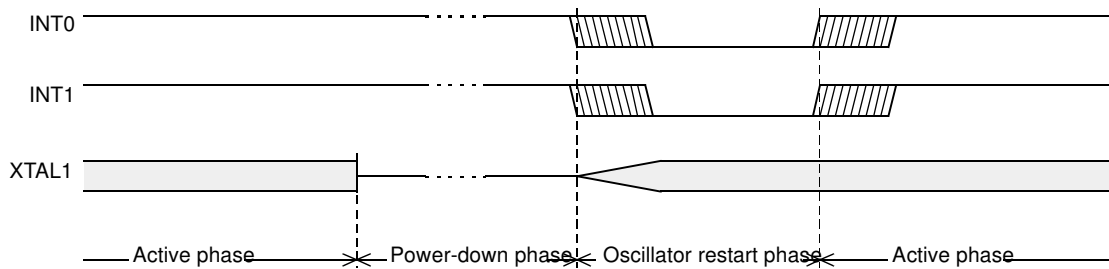
Table 6-19. IPH Register
IPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
Bit Number	Bit Mnemonic	Description					
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
6	PPCH	PCA interrupt priority bit high. <u>PPCH</u> <u>PPC</u> <u>Priority Level</u> 0 0 Lowest 0 1 1 0 1 1 Highest					
5	PT2H	Timer 2 overflow interrupt Priority High bit <u>PT2H</u> <u>PT2</u> <u>Priority Level</u> 0 0 Lowest 0 1 1 0 1 1 Highest					
4	PSH	Serial port Priority High bit <u>PSH</u> <u>PS</u> <u>Priority Level</u> 0 0 Lowest 0 1 1 0 1 1 Highest					
3	PT1H	Timer 1 overflow interrupt Priority High bit <u>PT1H</u> <u>PT1</u> <u>Priority Level</u> 0 0 Lowest 0 1 1 0 1 1 Highest					
2	PX1H	External interrupt 1 Priority High bit <u>PX1H</u> <u>PX1</u> <u>Priority Level</u> 0 0 Lowest 0 1 1 0 1 1 Highest					
1	PT0H	Timer 0 overflow interrupt Priority High bit <u>PT0H</u> <u>PT0</u> <u>Priority Level</u> 0 0 Lowest 0 1 1 0 1 1 Highest					
0	PX0H	External interrupt 0 Priority High bit <u>PX0H</u> <u>PX0</u> <u>Priority Level</u> 0 0 Lowest 0 1 1 0 1 1 Highest					

Reset Value = X000 0000b

Not bit addressable

Figure 6-14. Power-Down Exit Waveform



Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does not affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

Note: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

Table 6-20. The state of ports during idle and power-down mode

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data*	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power-down	Internal	0	0	Port Data*	Port Data	Port Data	Port Data
Power-down	External	0	0	Floating	Port Data	Port Data	Port Data

* Port 0 can force a "zero" level. A "one" will leave port floating.

7.1 Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 7-2. AUXR Register
AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	EXTRAM	AO

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	EXTRAM	EXTRAM bit See Table 6-1.
0	AO	ALE Output bit Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = XXXX XX00b

Not bit addressable

9. TS87C51RB2/RC2/RD2 EPROM

9.1 EPROM Structure

The TS87C51RB2/RC2/RD2 EPROM is divided in two different arrays:

- the code array: 16/32/64 Kbytes.
- the encryption array: 64 bytes.

In addition a third non programmable array is implemented:

- the signature array: 4 bytes.

9.2 EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

9.2.1 Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

9.2.2 Program Lock Bits

The three lock bits, when programmed according to Table 9-1.9.2.3, will provide different level of protection for the on-chip code and data.

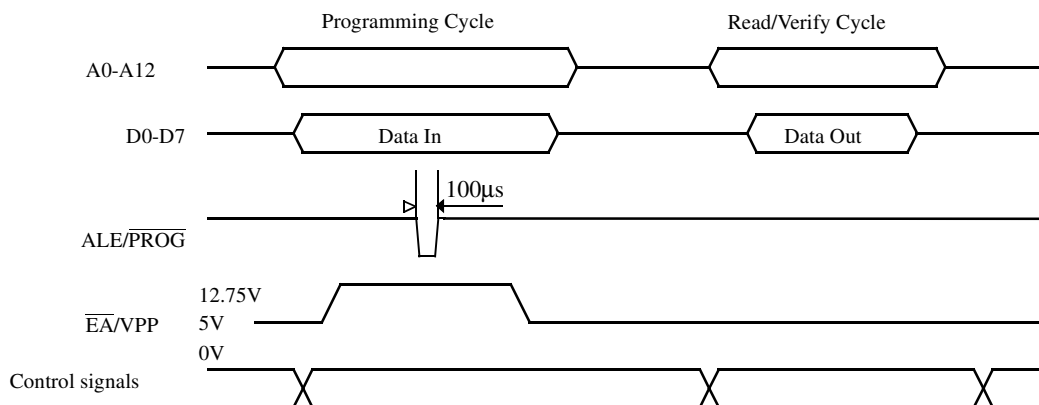
Table 9-1. Program Lock bits

Program Lock Bits				Protection Description
Security level	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	P	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the EPROM is disabled.
3	U	P	U	Same as 2, also verify is disabled.
4	U	U	P	Same as 3, also external execution is disabled.

U: unprogrammed,
P: programmed

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.

Figure 9-2. Programming and Verification Signal's Waveform



9.4 EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

9.4.1 Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm². Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm² rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

10. Signature Bytes

The TS83/87C51RB2/RC2/RD2 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 31. for Read Signature Bytes. Table 10-1. shows the content of the signature byte for the TS87C51RB2/RC2/RD2.

Table 10-1. Signature Bytes Content

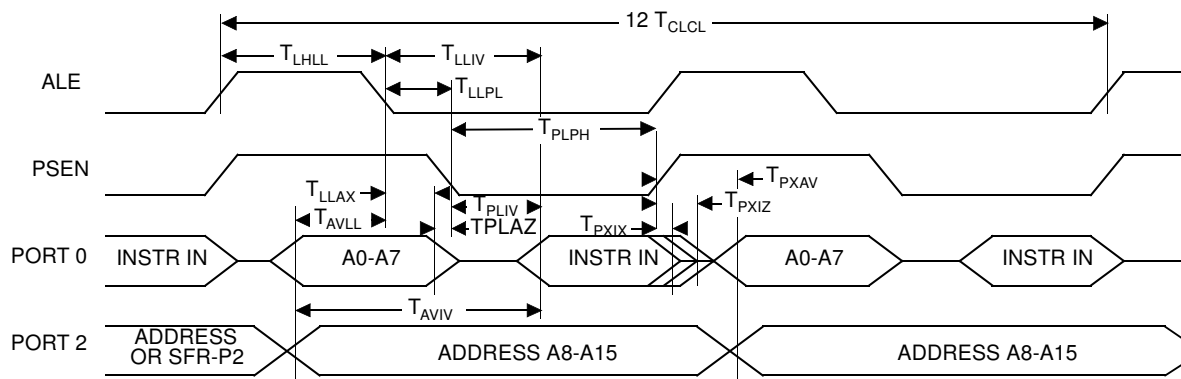
Location	Contents	Comment
30h	58h	Manufacturer Code: Atmel
31h	57h	Family Code: C51 X2
60h	7Ch	Product name: TS83C51RD2

Table 11-7. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{LHLL}	Min	$2 T - x$	$T - x$	10	8	15	ns
T_{AVLL}	Min	$T - x$	$0.5 T - x$	15	13	20	ns
T_{LLAX}	Min	$T - x$	$0.5 T - x$	15	13	20	ns
T_{LLIV}	Max	$4 T - x$	$2 T - x$	30	22	35	ns
T_{LLPL}	Min	$T - x$	$0.5 T - x$	10	8	15	ns
T_{PLPH}	Min	$3 T - x$	$1.5 T - x$	20	15	25	ns
T_{PLIV}	Max	$3 T - x$	$1.5 T - x$	40	25	45	ns
T_{PXIX}	Min	x	x	0	0	0	ns
T_{PXIZ}	Max	$T - x$	$0.5 T - x$	7	5	15	ns
T_{AVIV}	Max	$5 T - x$	$2.5 T - x$	40	30	45	ns
T_{PLAZ}	Max	x	x	10	10	10	ns

11.5.3 External Program Memory Read Cycle

Figure 11-6. External Program Memory Read Cycle



11.5.4 External Data Memory Characteristics

Symbol	Parameter
T_{RLRH}	\overline{RD} Pulse Width
T_{WLWH}	\overline{WR} Pulse Width
T_{RLDV}	\overline{RD} to Valid Data In
T_{RHDx}	Data Hold After \overline{RD}
T_{RHDZ}	Data Float After \overline{RD}
T_{LLDV}	ALE to Valid Data In
T_{AVDV}	Address to Valid Data In
T_{LLWL}	ALE to \overline{WR} or \overline{RD}
T_{AVWL}	Address to \overline{WR} or \overline{RD}
T_{QVWX}	Data Valid to \overline{WR} Transition
T_{QVWH}	Data set-up to \overline{WR} High
T_{WHQX}	Data Hold After \overline{WR}
T_{RLAZ}	\overline{RD} Low to Address Float
T_{WHLH}	\overline{RD} or \overline{WR} High to ALE high

Table 11-8. AC Parameters for a Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
T_{RLRH}	130		85		135		125		175		ns
T_{WLWH}	130		85		135		125		175		ns
T_{RLDV}		100		60		102		95		137	ns
T_{RHDx}	0		0		0		0		0		ns
T_{RHDZ}		30		18		35		25		42	ns
T_{LLDV}		160		98		165		155		222	ns
T_{AVDV}		165		100		175		160		235	ns
T_{LLWL}	50	100	30	70	55	95	45	105	70	130	ns
T_{AVWL}	75		47		80		70		103		ns
T_{QVWX}	10		7		15		5		13		ns
T_{QVWH}	160		107		165		155		213		ns
T_{WHQX}	15		9		17		10		18		ns
T_{RLAZ}		0		0		0		0		0	ns
T_{WHLH}	10	40	7	27	15	35	5	45	13	53	ns

11.5.9 EPROM Programming and Verification Characteristics

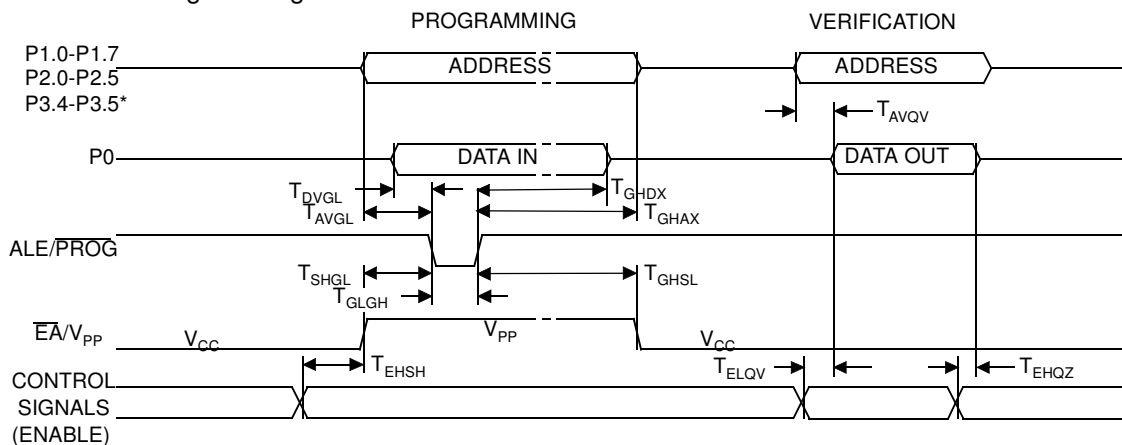
$T_A = 21^\circ\text{C}$ to 27°C ; $V_{SS} = 0\text{V}$; $V_{CC} = 5\text{V} \pm 10\%$ while programming. V_{CC} = operating range while

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13	V
I_{PP}	Programming Supply Current		75	mA
$1/T_{CLCL}$	Oscillator Frequency	4	6	MHz
T_{AVGL}	Address Setup to $\overline{\text{PROG}}$ Low	$48 T_{CLCL}$		
T_{GHAX}	Address Hold after $\overline{\text{PROG}}$	$48 T_{CLCL}$		
T_{DVGL}	Data Setup to $\overline{\text{PROG}}$ Low	$48 T_{CLCL}$		
T_{GHDX}	Data Hold after $\overline{\text{PROG}}$	$48 T_{CLCL}$		
T_{EHS}	(Enable) High to V_{PP}	$48 T_{CLCL}$		
T_{SHGL}	V_{PP} Setup to $\overline{\text{PROG}}$ Low	10		μs
T_{GHSL}	V_{PP} Hold after $\overline{\text{PROG}}$	10		μs
T_{GLGH}	$\overline{\text{PROG}}$ Width	90	110	μs
T_{AVQV}	Address to Valid Data		$48 T_{CLCL}$	
T_{ELQV}	ENABLE Low to Data Valid		$48 T_{CLCL}$	
T_{EHQZ}	Data Float after ENABLE	0	$48 T_{CLCL}$	

verifying

11.5.10 EPROM Programming and Verification Waveforms

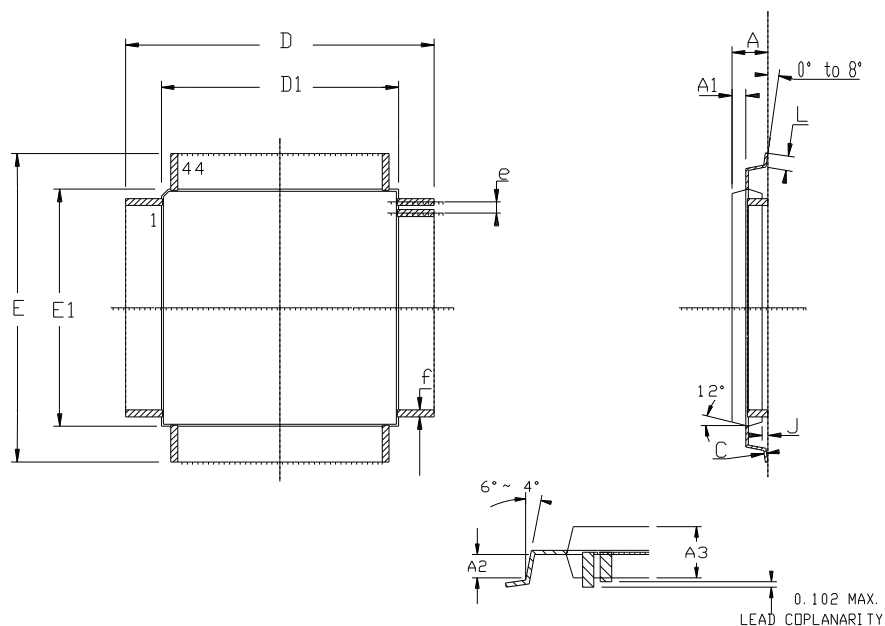
Figure 11-10. EPROM Programming and Verification Waveforms



* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

Part Number	Memory size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS83C51RB2-MCA	OBSOLETE					
TS83C51RB2-MCB						
TS83C51RB2-MCE						
TS83C51RB2-MIA						
TS83C51RB2-MIB						
TS83C51RB2-MIE						
TS83C51RB2-LCA						
TS83C51RB2-LCB						
TS83C51RB2-LCE						
TS83C51RB2-LIA						
TS83C51RB2-LIB						
TS83C51RB2-LIE						
TS83C51RB2-VCA						
TS83C51RB2-VCB						
TS83C51RB2-VCE						
TS83C51RB2-VIA						
TS83C51RB2-VIB						
TS83C51RB2-VIE						
AT83C51RB2-3CSUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PDIL40	Stick
AT83C51RB2-SLSUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PLCC44	Stick
AT83C51RB2-RLTUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	VQFP44	Tray
AT83C51RB2-3CSUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PDIL40	Stick
AT83C51RB2-SLSUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PLCC44	Stick
AT83C51RB2-RLTUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	VQFP44	Tray

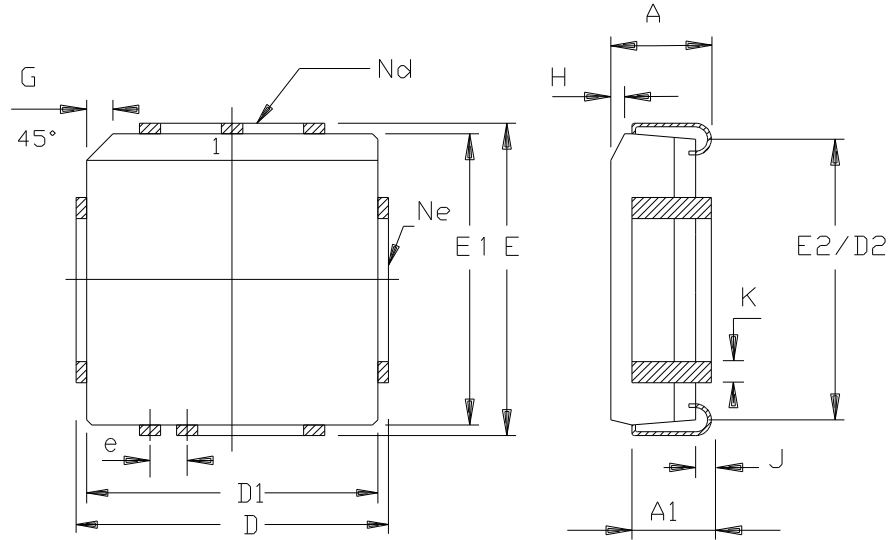
13.3 VQFP44



	MM		INCH	
	Min	Max	Min	Max
A	-	1.60	-	.063
A1	0.64 REF		.025 REF	
A2	0.64 REF		.025 REF	
A3	1.35	1.45	.053	.057
D	11.90	12.10	.468	.476
D1	9.90	10.10	.390	.398
E	11.90	12.10	.468	.476
E1	9.90	10.10	.390	.398
J	0.05	-	.002	-
L	0.45	0.75	.018	.030
e	0.80 BSC		.0315 BSC	
f	0.35 BSC		.014 BSC	

13.5 PLCC68

68 PINS PLCC



	MM		INCH	
A	4. 20	5. 08	. 165	. 200
A1	2. 29	3. 30	. 090	. 130
D	25. 02	25. 27	. 985	. 995
D1	24. 13	24. 33	. 950	. 958
D2	22. 61	23. 62	. 890	. 930
E	25. 02	25. 27	. 985	. 995
E1	24. 13	24. 33	. 950	. 958
E2	22. 61	23. 62	. 890	. 930
e	1. 27	BSC	. 050	BSC
G	1. 07	1. 22	. 042	. 048
H	1. 07	1. 42	. 042	. 056
J	0. 51	-	. 020	-
K	0. 33	0. 53	. 013	. 021
Nd	17		17	
Ne	17		17	
PKG STD		00		

14. Datasheet Revision History

14.1 Changes from 4188E to 4188F

1. Removed TS80C51RD2 and AT80C51RD2 from “Ordering Information” on page 73.
2. Removed non-green part numbers from ordering information.