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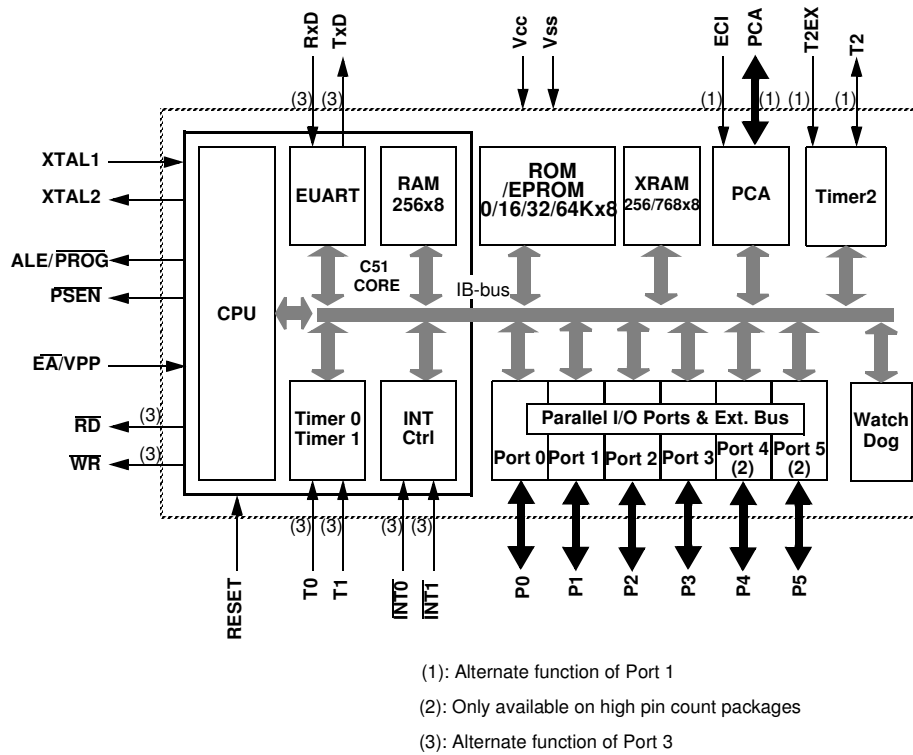
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/at87c51rd2-slsun">https://www.e-xfl.com/product-detail/microchip-technology/at87c51rd2-slsun</a>

### 3. Block Diagram

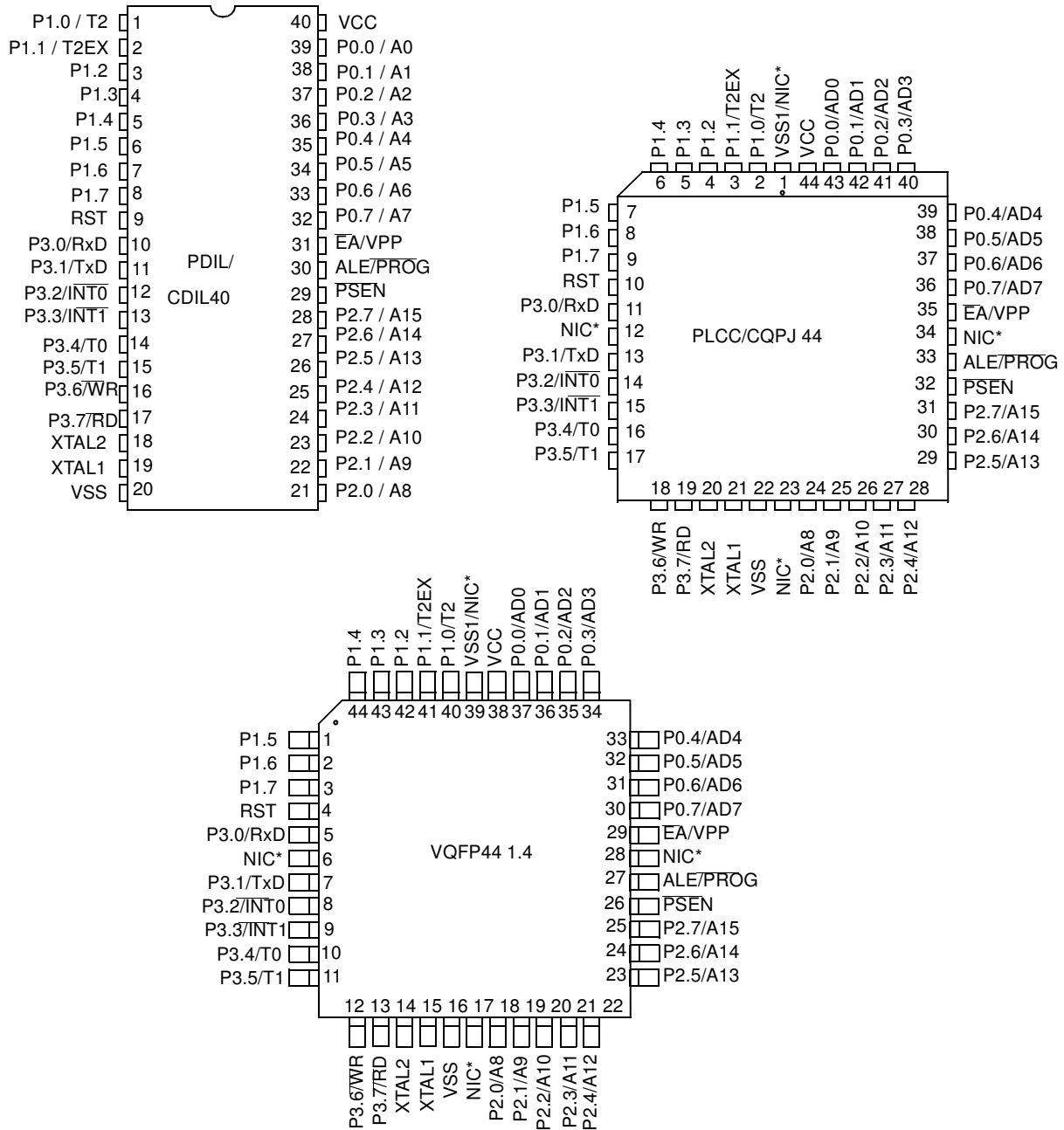


**Table 4-1.** All SFRs with their address and their reset value

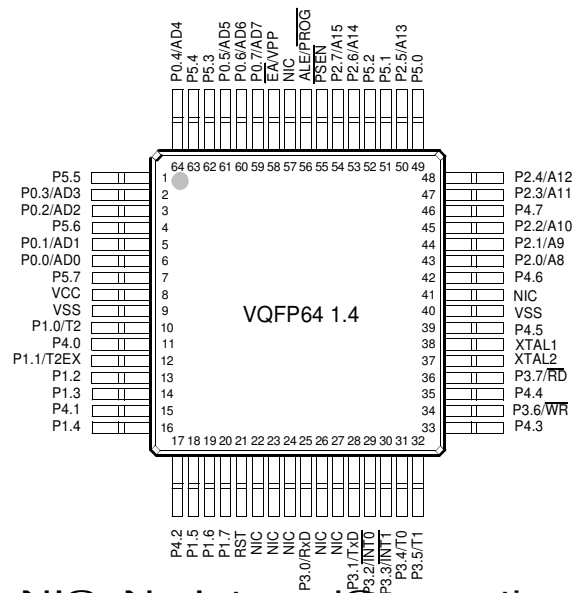
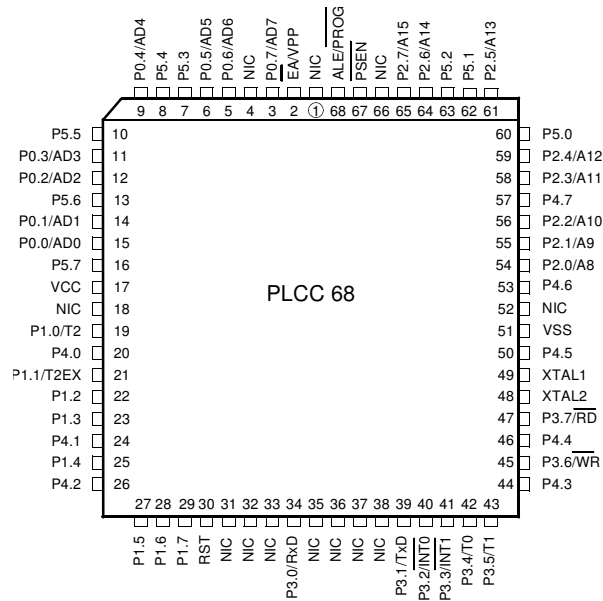
	Bit addressable	Non Bit addressable							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h		CH 0000 0000	CCAP0H XXXX XXXX	CCAP1H XXXX XXXX	CCAPL2H XXXX XXXX	CCAPL3H XXXX XXXX	CCAPL4H XXXX XXXX		FFh
F0h	B 0000 0000								F7h
E8h	P5 bit addressable 1111 1111	CL 0000 0000	CCAP0L XXXX XXXX	CCAP1L XXXX XXXX	CCAPL2L XXXX XXXX	CCAPL3L XXXX XXXX	CCAPL4L XXXX XXXX		EFh
E0h	ACC 0000 0000								E7h
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		DFh
D0h	PSW 0000 0000								D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0h	P4 bit addressable 1111 1111							P5 byte addressable 1111 1111	C7h
B8h	IP X000 000	SADEN 0000 0000							BFh
B0h	P3 1111 1111							IPH X000 0000	B7h
A8h	IE 0000 0000	SADDR 0000 0000							AFh
A0h	P2 1111 1111		AUXR1 XXXX0XX0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXXXXXX00	CKCON XXXX XXX0	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

reserved

## 5. Pin Configuration



\*NIC: No Internal Connection



NIC: No Internal Connection

Mnemonic	Pin Number			Type	Name And Function
	DIL	LCC	VQFP 1.4		
V <sub>SS</sub>	20	22	16	I	<b>Ground:</b> 0V reference
V <sub>SS1</sub>		1	39	I	Optional Ground: <b>Contact the Sales Office for ground connection.</b>
V <sub>CC</sub>	40	44	38	I	<b>Power Supply:</b> This is the power supply voltage for normal, idle and power-down operation
P0.0-P0.7	39-32	43-36	37-30	I/O	<b>Port 0:</b> Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to V <sub>CC</sub> or V <sub>SS</sub> in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes.
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	<b>Port 1:</b> Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification. Alternate functions for Port 1 include:
	1	2	40	I/O	<b>T2 (P1.0):</b> Timer/Counter 2 external count input/Clockout
	2	3	41	I	<b>T2EX (P1.1):</b> Timer/Counter 2 Reload/Capture/Direction Control
	3	4	42	I	<b>ECI (P1.2):</b> External Clock for the PCA
	4	5	43	I/O	<b>CEX0 (P1.3):</b> Capture/Compare External I/O for PCA module 0
	5	6	44	I/O	<b>CEX1 (P1.4):</b> Capture/Compare External I/O for PCA module 1
	6	7	45	I/O	<b>CEX0 (P1.5):</b> Capture/Compare External I/O for PCA module 2
	7	8	46	I/O	<b>CEX0 (P1.6):</b> Capture/Compare External I/O for PCA module 3
	8	9	47	I/O	<b>CEX0 (P1.7):</b> Capture/Compare External I/O for PCA module 4
P2.0-P2.7	21-28	24-31	18-25	I/O	<b>Port 2:</b> Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR. Some Port 2 pins (P2.0 to P2.5) receive the high order address bits during EPROM programming and verification:
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	<b>Port 3:</b> Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Some Port 3 pins (P3.4 to P3.5) receive the high order address bits during EPROM programming and verification. Port 3 also serves the special features of the 80C51 family, as listed below.
	10	11	5	I	<b>RXD (P3.0):</b> Serial input port
	11	13	7	O	<b>TXD (P3.1):</b> Serial output port

## 6. Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.

### ASSEMBLY LANGUAGE

```
; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2  AUXR1 EQU 0A2H
;
0000 909000MOV DPTR,#SOURCE ; address of SOURCE
0003 05A2 INC AUXR1 ; switch data pointers
0005 90A000 MOV DPTR,#DEST ; address of DEST
0008 LOOP:
0008 05A2 INC AUXR1 ; switch data pointers
000A E0 MOVX A,@DPTR ; get a byte from SOURCE
000B A3 INC DPTR ; increment SOURCE address
000C 05A2 INC AUXR1 ; switch data pointers
000E F0 MOVX @DPTR,A ; write the byte to DEST
000F A3 INC DPTR ; increment DEST address
0010 70F6JNZ LOOP ; check for 0 terminator
0012 05A2 INC AUXR1 ; (optional) restore DPS
```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

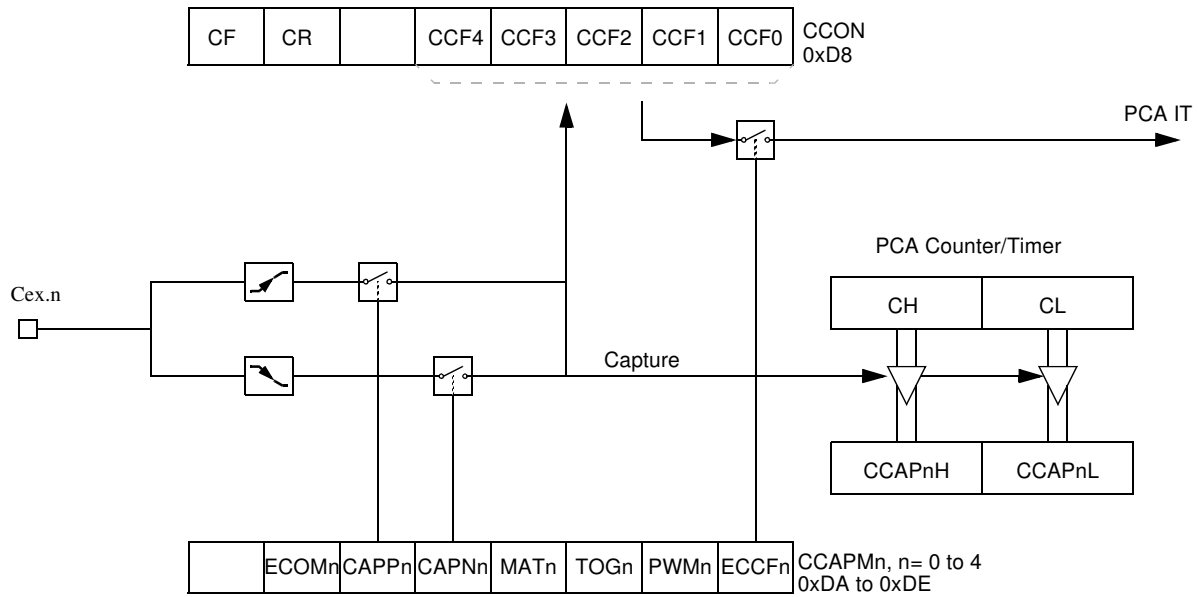
Bit Number	Bit Mnemonic	Description
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
3	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
2	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
1	T2OE	<b>Timer 2 Output Enable bit</b> Clear to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.
0	DCEN	<b>Down Counter Enable bit</b> Clear to disable timer 2 as up/down counter. Set to enable timer 2 as up/down counter.

Reset Value = XXXX XX00b

Not bit addressable



**Figure 6-6. PCA Capture Mode**



### 6.3.2 16-bit Software Timer/ Compare Mode

The PCA modules can be used as software timers by setting both the **ECOM** and **MAT** bits in the modules **CCAPMn** register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the **CCFn** (**CCON** SFR) and the **ECCFn** (**CCAPMn** SFR) bits for the module are both set (See Figure 6-7).

Bit Number	Bit Mnemonic	Description												
7	FE	<b>Framing Error bit (SMOD0=1)</b> Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit												
	SM0	<b>Serial port Mode bit 0</b> Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit												
6	SM1	<b>Serial port Mode bit 1</b> <u>SM0 SM1 Mode Description Baud Rate</u> <table> <tr> <td>0</td><td>0</td><td>0Shift Register <math>F_{XTAL}/12</math> (/6 in X2 mode)</td></tr> <tr> <td>0</td><td>1</td><td>18-bit UARTVariable</td></tr> <tr> <td>1</td><td>0</td><td>29-bit UART <math>F_{XTAL}/64</math> or <math>F_{XTAL}/32</math> (/32, /16 in X2 mode)</td></tr> <tr> <td>1</td><td>1</td><td>39-bit UARTVariable</td></tr> </table>	0	0	0Shift Register $F_{XTAL}/12$ (/6 in X2 mode)	0	1	18-bit UARTVariable	1	0	29-bit UART $F_{XTAL}/64$ or $F_{XTAL}/32$ (/32, /16 in X2 mode)	1	1	39-bit UARTVariable
0	0	0Shift Register $F_{XTAL}/12$ (/6 in X2 mode)												
0	1	18-bit UARTVariable												
1	0	29-bit UART $F_{XTAL}/64$ or $F_{XTAL}/32$ (/32, /16 in X2 mode)												
1	1	39-bit UARTVariable												
5	SM2	<b>Serial port Mode 2 bit / Multiprocessor Communication Enable bit</b> Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.												
4	REN	<b>Reception Enable bit</b> Clear to disable serial reception. Set to enable serial reception.												
3	TB8	Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3 Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.												
2	RB8	<b>Receiver Bit 8 / Ninth bit received in modes 2 and 3</b> Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.												
1	TI	<b>Transmit Interrupt flag</b> Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.												
0	RI	<b>Receive Interrupt flag</b> Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 6-11. and Figure 6-12. in the other modes.												

Reset Value = 0000 0000b

Bit addressable

**Table 6-15.** PCON Register  
PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

Bit Number	Bit Mnemonic	Description																																				
7	T4	<b>Reserved</b> Do not try to set or clear this bit.																																				
6	T3																																					
5	T2																																					
4	T1																																					
3	T0																																					
2	S2	WDT Time-out select bit 2																																				
1	S1	WDT Time-out select bit 1																																				
0	S0	WDT Time-out select bit 0																																				
		<table><tr><td><u>S2</u></td><td><u>S1</u></td><td><u>S0</u></td><td><u>Selected Time-out</u></td></tr><tr><td>0</td><td>0</td><td>0</td><td><math>0(2^{14} - 1)</math> machine cycles, 16.3 ms @ 12 MHz</td></tr><tr><td>0</td><td>0</td><td>1</td><td><math>1(2^{15} - 1)</math> machine cycles, 32.7 ms @ 12 MHz</td></tr><tr><td>0</td><td>1</td><td>0</td><td><math>0(2^{16} - 1)</math> machine cycles, 65.5 ms @ 12 MHz</td></tr><tr><td>0</td><td>1</td><td>1</td><td><math>1(2^{17} - 1)</math> machine cycles, 131 ms @ 12 MHz</td></tr><tr><td>1</td><td>0</td><td>0</td><td><math>0(2^{18} - 1)</math> machine cycles, 262 ms @ 12 MHz</td></tr><tr><td>1</td><td>0</td><td>1</td><td><math>1(2^{19} - 1)</math> machine cycles, 542 ms @ 12 MHz</td></tr><tr><td>1</td><td>1</td><td>0</td><td><math>0(2^{20} - 1)</math> machine cycles, 1.05 s @ 12 MHz</td></tr><tr><td>1</td><td>1</td><td>1</td><td><math>1(2^{21} - 1)</math> machine cycles, 2.09 s @ 12 MHz</td></tr></table>	<u>S2</u>	<u>S1</u>	<u>S0</u>	<u>Selected Time-out</u>	0	0	0	$0(2^{14} - 1)$ machine cycles, 16.3 ms @ 12 MHz	0	0	1	$1(2^{15} - 1)$ machine cycles, 32.7 ms @ 12 MHz	0	1	0	$0(2^{16} - 1)$ machine cycles, 65.5 ms @ 12 MHz	0	1	1	$1(2^{17} - 1)$ machine cycles, 131 ms @ 12 MHz	1	0	0	$0(2^{18} - 1)$ machine cycles, 262 ms @ 12 MHz	1	0	1	$1(2^{19} - 1)$ machine cycles, 542 ms @ 12 MHz	1	1	0	$0(2^{20} - 1)$ machine cycles, 1.05 s @ 12 MHz	1	1	1	$1(2^{21} - 1)$ machine cycles, 2.09 s @ 12 MHz
<u>S2</u>	<u>S1</u>	<u>S0</u>	<u>Selected Time-out</u>																																			
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1	1	1	$1(2^{21} - 1)$ machine cycles, 2.09 s @ 12 MHz																																			

Reset value XXXX X000

### 6.8.2 WDT during Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode the user does not need to service the WDT. There are 2 methods of exiting Power-down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally should whenever the TS80C51Rx2 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service routine.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is best to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the TS80C51Rx2 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

## 7.1 Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

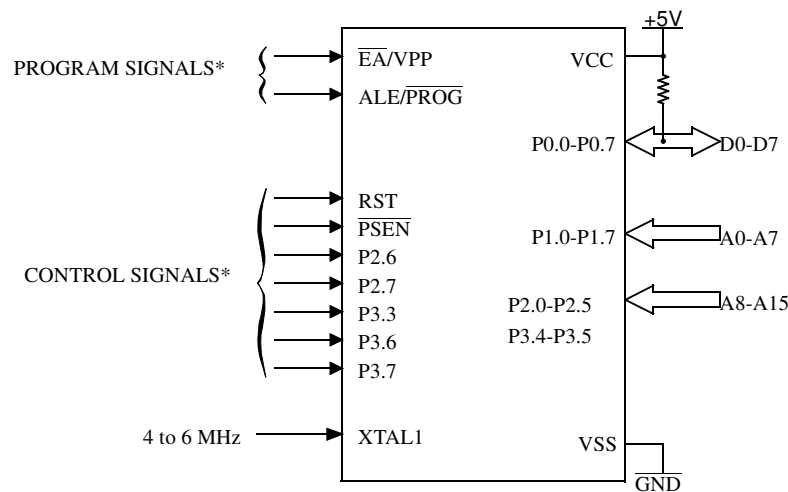
**Table 7-2.** AUXR Register  
AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	EXTRAM	AO
Bit Number	Bit Mnemonic	Description					
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
3	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
2	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
1	EXTRAM	<b>EXTRAM bit</b> See Table 6-1.					
0	AO	<b>ALE Output bit</b> Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.					

Reset Value = XXXX XX00b

Not bit addressable

**Figure 9-1.** Set-Up Modes Configuration



\* See Table 31, for proper value on these inputs

### 9.3.3 Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS87C51RB2/RC2/RD2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise  $\overline{EA}/VPP$  from VCC to VPP (typical 12.75V).
- Step 5: Pulse ALE/ $\overline{PROG}$  once.
- Step 6: Lower  $\overline{EA}/VPP$  from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See [Figure 9-2](#)).

### 9.3.4 Verify algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C51RB2/RC2/RD2.

P 2.7 is used to enable data output.

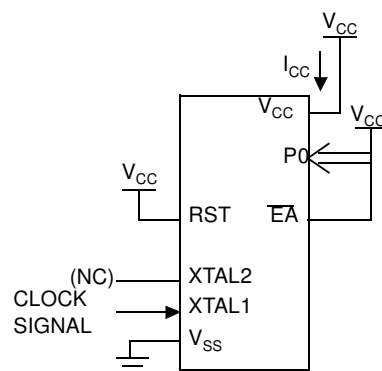
To verify the TS87C51RB2/RC2/RD2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See [Figure 9-2](#)).

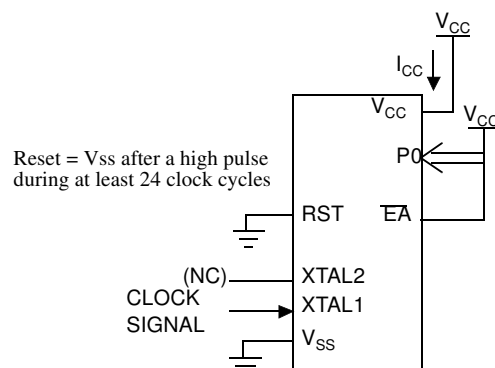
4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the  $V_{OL}$ s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi  $V_{OL}$  peak 0.6V. A Schmitt Trigger use is not necessary.
5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
6. Under steady state (non-transient) conditions,  $I_{OL}$  must be externally limited as follows:  
 Maximum  $I_{OL}$  per port pin: 10 mA  
 Maximum  $I_{OL}$  per 8-bit port:  
 Port 0: 26 mA  
 Ports 1, 2, 3 and 4 and 5 when available: 15 mA  
 Maximum total  $I_{OL}$  for all output pins: 71 mA  
 If  $I_{OL}$  exceeds the test condition,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
7. For other values, please contact your sales office.
8. Operating  $I_{CC}$  is measured with all output pins disconnected; XTAL1 driven with  $T_{CLCH}$ ,  $T_{CHCL} = 5$  ns (see Figure 11-5.),  $V_{IL} = V_{SS} + 0.5$  V,  $V_{IH} = V_{CC} - 0.5$  V; XTAL2 N.C.;  $\overline{EA} = \text{Port 0} = V_{CC}$ ; RST =  $V_{SS}$ . The internal ROM runs the code 80 FE (label: SJMP label).  $I_{CC}$  would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.

**Figure 11-1.**  $I_{CC}$  Test Condition, under reset



All other pins are disconnected.

**Figure 11-2.** Operating  $I_{CC}$  Test Condition



All other pins are disconnected.

$T_A = 0$  to  $+70^{\circ}\text{C}$  (commercial temperature range);  $V_{SS} = 0$  V;  $2.7$  V  $< V_{CC} < 5.5$  V; -L range.  
 $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  (industrial temperature range);  $V_{SS} = 0$  V;  $2.7$  V  $< V_{CC} < 5.5$  V; -L range.

Table 11-3. gives the maximum applicable load capacitance for Port 0, Port 1, 2 and 3, and ALE and PSEN signals. Timings will be guaranteed if these capacitances are respected. Higher capacitance values can be used, but timings will then be degraded.

**Table 11-3.** Load Capacitance versus speed range, in pF

	-M	-V	-L
Port 0	100	50	100
Port 1, 2, 3	80	50	80
ALE / PSEN	100	30	100

Table 11-5., Table 39. and Table 42. give the description of each AC symbols.

Table 11-6., Table 11-8. and Table 11-10. give for each range the AC parameter.

Table 11-7., Table 11-9. and Table 11-11. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

**Table 11-4.** Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20	40	30	30	20
T (ns)	25	50	25	33.3	33.3	50

Example:

$T_{LLIV}$  in X2 mode for a -V part at 20 MHz ( $T = 1/20^{\text{E6}} = 50$  ns):

$$x = 22 \text{ (Table 11-7.)}$$

$$T = 50\text{ns}$$

$$T_{LLIV} = 2T - x = 2 \times 50 - 22 = 78\text{ns}$$

## 11.5.2 External Program Memory Characteristics

**Table 11-5.** Symbol Description

Symbol	Parameter
T	Oscillator clock period
T <sub>LHLL</sub>	ALE pulse width
T <sub>AVLL</sub>	Address Valid to ALE
T <sub>LLAX</sub>	Address Hold After ALE
T <sub>LLIV</sub>	ALE to Valid Instruction In
T <sub>LLPL</sub>	ALE to $\overline{\text{PSEN}}$
T <sub>PLPH</sub>	$\overline{\text{PSEN}}$ Pulse Width
T <sub>PLIV</sub>	$\overline{\text{PSEN}}$ to Valid Instruction In
T <sub>PXIX</sub>	Input Instruction Hold After $\overline{\text{PSEN}}$
T <sub>PXIZ</sub>	Input Instruction Float After $\overline{\text{PSEN}}$
T <sub>PXAV</sub>	$\overline{\text{PSEN}}$ to Address Valid
T <sub>AVIV</sub>	Address to Valid Instruction In
T <sub>PLAZ</sub>	$\overline{\text{PSEN}}$ Low to Address Float

**Table 11-6.** AC Parameters for Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T	25		33		25		50		33		ns
T <sub>LHLL</sub>	40		25		42		35		52		ns
T <sub>AVLL</sub>	10		4		12		5		13		ns
T <sub>LLAX</sub>	10		4		12		5		13		ns
T <sub>LLIV</sub>		70		45		78		65		98	ns
T <sub>LLPL</sub>	15		9		17		10		18		ns
T <sub>PLPH</sub>	55		35		60		50		75		ns
T <sub>PLIV</sub>		35		25		50		30		55	ns
T <sub>PXIX</sub>	0		0		0		0		0		ns
T <sub>PXIZ</sub>		18		12		20		10		18	ns
T <sub>AVIV</sub>		85		53		95		80		122	ns
T <sub>PLAZ</sub>		10		10		10		10		10	ns

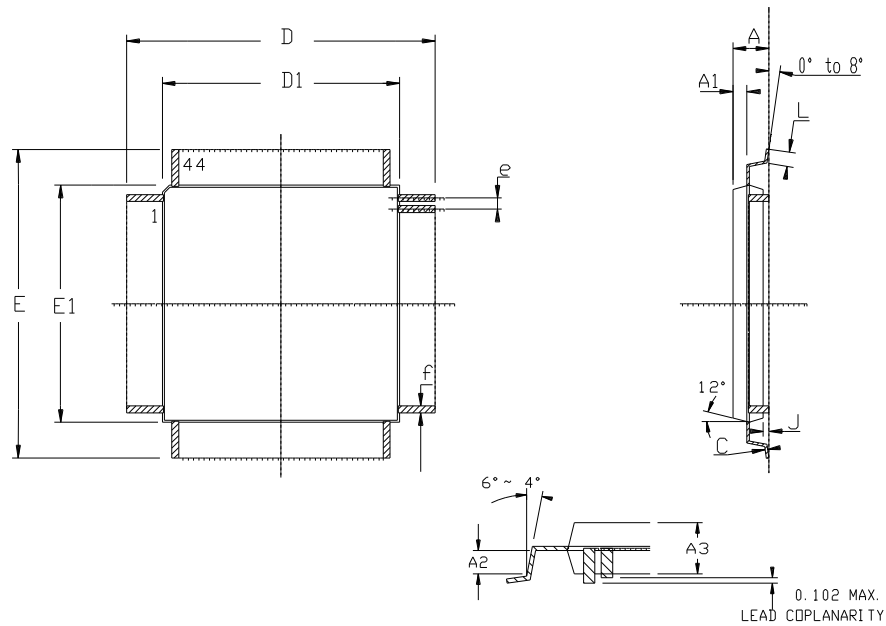


Part Number	Memory size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT80C51RA2-3CSCV	OBSOLETE					
AT80C51RA2-SLSCV						
AT80C51RA2-RLTCV						
AT80C51RA2-3CSIV						
AT80C51RA2-SLSIV						
AT80C51RA2-RLSIV						
TS80C51RD2-MCA	Not recommended use AT87C51RD2					
TS80C51RD2-MCB	Not recommended use AT87C51RD2					
TS80C51RD2-MCE	Not recommended use AT87C51RD2					
TS80C51RD2-MIA	Not recommended use AT87C51RD2					
TS80C51RD2-MIB	Not recommended use AT87C51RD2					
TS80C51RD2-MIE	Not recommended use AT87C51RD2					
TS80C51RD2-LCA	Not recommended use AT87C51RD2					
TS80C51RD2-LCB	Not recommended use AT87C51RD2					
TS80C51RD2-LCE	Not recommended use AT87C51RD2					
TS80C51RD2-LIA	Not recommended use AT87C51RD2					
TS80C51RD2-LIB	Not recommended use AT87C51RD2					
TS80C51RD2-LIE	Not recommended use AT87C51RD2					
TS80C51RD2-VCA	Not recommended use AT87C51RD2					
TS80C51RD2-VCB	Not recommended use AT87C51RD2					
TS80C51RD2-VCE	Not recommended use AT87C51RD2					
TS80C51RD2-VIA	Not recommended use AT87C51RD2					
TS80C51RD2-VIB	Not recommended use AT87C51RD2					
TS80C51RD2-VIE	Not recommended use AT87C51RD2					
AT80C51RD2-3CSUM	Not recommended use AT87C51RD2					
AT80C51RD2-SLSUM	Not recommended use AT87C51RD2					
AT80C51RD2-RLTUM	Not recommended use AT87C51RD2					
AT80C51RD2-3CSUL	Not recommended use AT87C51RD2					
AT80C51RD2-SLSUL	Not recommended use AT87C51RD2					
AT80C51RD2-RLTUL	Not recommended use AT87C51RD2					

Part Number	Memory size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS87C51RC2-MCA	OBSOLETE					
TS87C51RC2-MCB						
TS87C51RC2-MCE						
TS87C51RC2-MIA						
TS87C51RC2-MIB						
TS87C51RC2-MIE						
TS87C51RC2-LCA						
TS87C51RC2-LCB						
TS87C51RC2-LCE						
TS87C51RC2-LIA						
TS87C51RC2-LIB						
TS87C51RC2-LIE						
TS87C51RC2-VCA						
TS87C51RC2-VCB						
TS87C51RC2-VCE						
TS87C51RC2-VIA						
TS87C51RC2-VIB						
TS87C51RC2-VIE						
AT87C51RC2-3CSUM	OTP 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PDIL40	Stick
AT87C51RC2-SLSUM	OTP 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PLCC44	Stick
AT87C51RC2-RLTUM	OTP 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	VQFP44	Tray
AT87C51RC2-3CSUL	OTP 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PDIL40	Stick
AT87C51RC2-SLSUL	OTP 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PLCC44	Stick
AT87C51RC2-RLTUL	OTP 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	VQFP44	Tray

Part Number	Memory size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS87C51RD2-MCA	OBSOLETE					
TS87C51RD2-MCB						
TS87C51RD2-MCE						
TS87C51RD2-MIA						
TS87C51RD2-MIB						
TS87C51RD2-MIE						
TS87C51RD2-LCA						
TS87C51RD2-LCB						
TS87C51RD2-LCE						
TS87C51RD2-LIA						
TS87C51RD2-LIB						
TS87C51RD2-LIE						
TS87C51RD2-VCA						
TS87C51RD2-VCB						
TS87C51RD2-VCE						
TS87C51RD2-VCL						
TS87C51RD2-VIA						
TS87C51RD2-VIB						
TS87C51RD2-VIE						
AT87C51RD2-3CSUM	OTP 64k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PDIL40	Stick
AT87C51RD2-SLSUM	OTP 64k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PLCC44	Stick
AT87C51RD2-RLTUM	OTP 64k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	VQFP44	Tray
AT87C51RD2-3CSUL	OTP 64k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PDIL40	Stick
AT87C51RD2-SLSUL	OTP 64k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PLCC44	Stick
AT87C51RD2-RLTUL	OTP 64k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	VQFP44	Tray

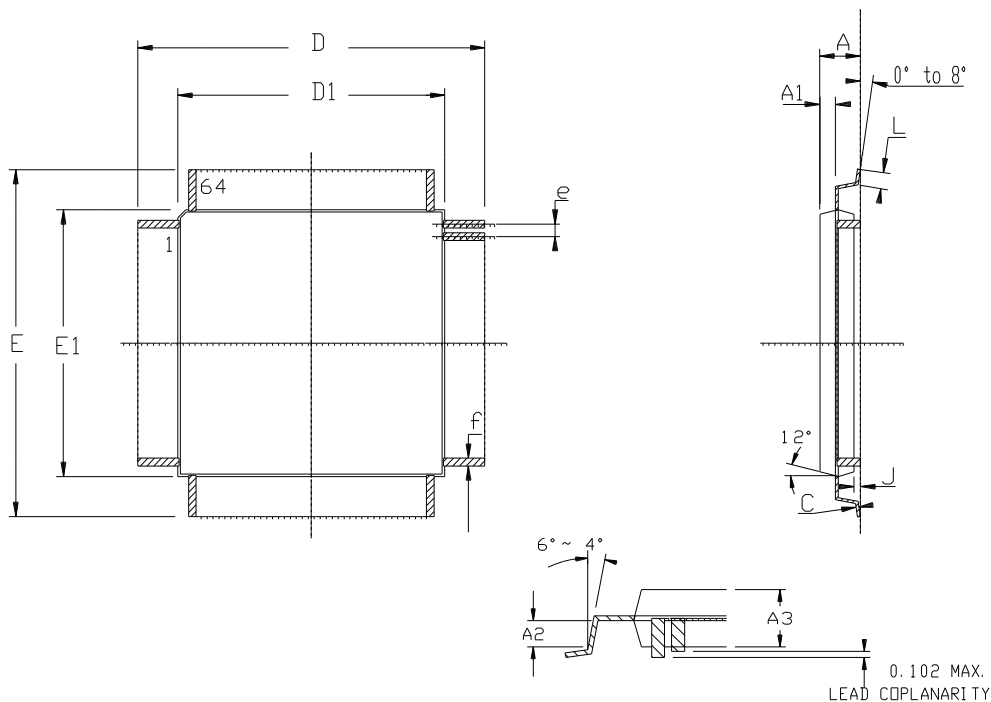
### 13.3 VQFP44



	MM		INCH	
	Min	Max	Min	Max
A	-	1.60	-	.063
A1	0.64 REF		.025 REF	
A2	0.64 REF		.025 REF	
A3	1.35	1.45	.053	.057
D	11.90	12.10	.468	.476
D1	9.90	10.10	.390	.398
E	11.90	12.10	.468	.476
E1	9.90	10.10	.390	.398
J	0.05	-	.002	-
L	0.45	0.75	.018	.030
e	0.80 BSC		.0315 BSC	
f	0.35 BSC		.014 BSC	

## 13.4 VQFP64

### SQUARE GULL WING (1.4 mm)



	MM		INCH	
	Min	Max	Min	Max
A	-	1.60	-	.063
A1	0.64 REF		.025 REF	
A2	0.64 REF		.025 REF	
A3	1.35	1.45	.053	.057
D	11.75	12.25	.463	.483
D1	9.90	10.10	.390	.398
E	11.75	12.25	.463	.483
E1	9.90	10.10	.390	.398
J	0.05	-	.002	-
L	0.45	0.75	.018	.030
e	0.50 BSC		.0197 BSC	
f	0.25 BSC		.010 BSC	