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Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMIess
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts80c51ra2-lia

Email: info@E-XFL.COM

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	Bit addressable	Non Bit address	Non Bit addressable							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F		
F8h		CH 0000 0000	CCAP0H XXXX XXXX	CCAP1H XXXX XXXX	CCAPL2H XXXX XXXX	CCAPL3H XXXX XXXX	CCAPL4H XXXX XXXX		FFh	
F0h	B 0000 0000								F7h	
E8h	P5 bit addressable 1111 1111	CL 0000 0000	CCAP0L XXXX XXXX	CCAP1L XXXX XXXX	CCAPL2L XXXX XXXX	CCAPL3L XXXX XXXX	CCAPL4L XXXX XXXX		EFh	
E0h	ACC 0000 0000								E7h	
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		DFh	
D0h	PSW 0000 0000								D7h	
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh	
C0h	P4 bit addressable 1111 1111							P5 byte addressable 1111 1111	C7h	
B8h	IP X000 000	SADEN 0000 0000							BFh	
B0h	P3 1111 1111							IPH X000 0000	B7h	
A8h	IE 0000 0000	SADDR 0000 0000							AFh	
A0h	P2 1111 1111		AUXR1 XXXX0XX0				WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h	
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh	
90h	P1 1111 1111								97h	
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXXXX00	CKCON XXXX XXX0	8Fh	
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h	
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F		

 Table 4-1.
 All SFRs with their address and their reset value

reserved











The X2 bit in the CKCON register (Table 5-2) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

Note: In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers, PCA...) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.



7	6	5	4	3	2	1	0		
-	-	-	-	-	-	-	X2		
Bit Number	Bit Mnemonic	Description	escription						
7	-	Reserved The value re	Reserved The value read from this bit is indeterminate. Do not set this bit.						
6	-	Reserved The value re	Reserved The value read from this bit is indeterminate. Do not set this bit.						
5	-	Reserved The value re	Reserved The value read from this bit is indeterminate. Do not set this bit.						





6. Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.

ASSEMBLY LANGUAGE

; Block move using dual data pointers ; Destroys DPTR0, DPTR1, A and PSW ; note: DPS exits opposite of entry state ; unless an extra INC AUXR1 is added 00A2 AUXR1 EQU 0A2H ; 0000 909000MOV DPTR, #SOURCE ; address of SOURCE 0003 05A2 INC AUXR1 ; switch data pointers 0005 90A000 MOV DPTR, #DEST ; address of DEST 0008 LOOP: 0008 05A2 INC AUXR1 ; switch data pointers 000A EO MOVX A, @DPTR ; get a byte from SOURCE 000B A3 INC DPTR ; increment SOURCE address 000C 05A2 INC AUXR1 ; switch data pointers 000E FO MOVX @DPTR, A ; write the byte to DEST 000F A3 INC DPTR ; increment DEST address 0010 70F6JNZ LOOP ; check for 0 terminator 0012 05A2 INC AUXR1 ; (optional) restore DPS

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

6.2 Timer 2

The timer 2 in the TS80C51RX2 is compatible with the timer 2 in the 80C52. It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 6-2) and T2MOD register (See Table 6-3). Timer 2 operation is similar to Timer 0 and Timer 1. C/T2 selects $F_{OSC}/12$ (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and $CP/\overline{RL2}$ (T2CON), as described in the Atmel 8-bit Microcontroller Hardware description.

Refer to the Atmel 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C51RX2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

6.2.1 Auto-reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 6-2. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.





Figure 6-2. Auto-reload Mode Up/Down Counter (DCEN = 1)



6.2.2 Programmable Clock-Output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 6-3) . The input clock increments TL2 at frequency $F_{OSC}/2$. The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers:

$$Clock - OutFrequency = \frac{F_{osc}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz $(F_{OSC}/2^{16})$ to 4 MHz $(F_{OSC}/4)$. The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear C/T2 bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.
- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.

Figure 6-4. PCA Timer/Counter



Table 6-4. CMOD: PCA Counter Mode Register

CMOD Address 0D9H		CIDL	WDTE	-	-	-	CPS1	CPS0	ECF	
	Re	eset value	0	0	Х	х	х	0	0	0
Symbol	Functio	n								
CIDL	Counter Idle control: CIDL = 0 programs the PCA Counter to continue functioning during idle Mode. CIDL = 1 programs it to be gated off during idle.									
WDTE	Watchdo enables	og Timer E it.	Enable: WDTE	E = 0 disab	les Watch	dog Timei	r function (on PCA M	odule 4. W	/DTE = 1
-	Not impl	lemented,	reserved for	future use	. (1)					
CPS1	PCA Co	unt Pulse	Select bit 1.							
CPS0	PCA Co	unt Pulse	Select bit 0.							
	CPS1	CPS0	Selected PC	A input. ⁽²⁾						
	0	0	Internal clock	k f _{osc} /12(0	Or f _{osc} /6 in	X2 Mode).			
	0	1	Internal clock	k f _{osc} /4(O	r f _{osc} /2 in X	X2 Mode).				
	1 0 Timer 0 Overflow									
	1 1 External clock at ECI/P1.2 pin (max rate = f _{osc} / 8)									
ECF	PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function of CF.									

1. User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

2. $f_{osc} = oscillator frequency$

The CMOD SFR includes three additional bits associated with the PCA (See Figure 6-4 and Table 6-4).



Figure 6-5. PCA Interrupt System



PCA Modules: each one of the five compare/capture modules has six possible functions. It can perform:

- 16-bit Capture, positive-edge triggered,
- 16-bit Capture, negative-edge triggered,
- 16-bit Capture, both positive and negative-edge triggered,
- 16-bit Software Timer,
- 16-bit High Speed Output,
- 8-bit Pulse Width Modulator.

In addition, module 4 can be used as a Watchdog Timer.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (See Table 6-6). The registers contain the bits that control the mode that each module will operate in.

- The ECCF bit (CCAPMn.0 where n=0, 1, 2, 3, or 4 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module.
- PWM (CCAPMn.1) enables the pulse width modulation mode.
- The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register.
- The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.
- The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition.



There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output (See Table 6-8 & Table 6-9)

 Table 6-8.
 CCAPnH: PCA Modules Capture/Compare Registers High

	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

 Table 6-9.
 CCAPnL: PCA Modules Capture/Compare Registers Low

CCAPnL Address n = 0 - 4	
11 = 0 +	

CCAP0L=0EAH	
CCAP1L=0EBH	
CCAP2L=0ECH	
CCAP3L=0EDH	
CCAP4L=0EEH	

	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

Table 6-10.CH: PCA Counter High

CH Address 0F9H

Н									
		7	6	5	4	3	2	1	0
	Reset value	0	0	0	0	0	0	0	0

Table 6-11. CL: PCA Counter Low

CL

Address 0E9H

	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0

6.3.1 PCA Capture Mode

To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated (Refer to Figure 6-6).



Figure 6-9. PCA PWM Mode



6.3.5 PCA Watchdog Timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed. Figure 6-7 shows a diagram of how the watchdog works. The user preloads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

- 1. Periodically change the compare value so it will never match the PCA timer,
- 2. periodically change the PCA timer value so it will never match the compare values, or
- 3. Disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for all modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

This watchdog timer won't generate a reset out on the reset pin.





6.4 TS80C51Rx2 Serial I/O Port

The serial I/O port in the TS80C51Rx2 is compatible with the serial I/O port in the 80C52.

It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

Serial I/O port includes the following enhancements:

- Framing error detection
- · Automatic address recognition

6.4.1 Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 6-10).





When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 6-14.) bit is set.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 6-11 and Figure 6-12).







```
Slave C:SADDR1111 0010b

<u>SADEN1111 1101b</u>

Given1111 00X1b
```

The SADEN byte is selected so that each slave may be addressed separately.

For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. 1111 0000b).

For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).

To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

6.4.4 Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

SADDR0101 0110b SADEN1111 1100b Broadcast =SADDR OR SADEN1111 111Xb

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

```
Slave A:SADDR1111 0001b

<u>SADEN1111 1010b</u>

Broadcast1111 1X11b,

Slave B:SADDR1111 0011b

<u>SADEN1111 1001b</u>

Broadcast1111 1X11B,

Slave C:SADDR=1111 0010b

<u>SADEN1111 1101b</u>

Broadcast1111 1111b
```

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.

6.4.5 Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

Table 6-16.	Priority Level Bit Values
-------------	---------------------------

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Table 6-17. IE Register

IE - Interrupt Enable Register (A8h)

7	6		5	4	3	2	1	0		
EA	EC	I	ET2	ES	ET1	EX1	ET0	EX0		
Bit Number	Bit Mnem	nonic	Descrip	otion						
7	EA		Enable Clear to Set to e If EA=1, clearing	Enable All interrupt bit Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by clearing its own interrupt enable bit.						
6	EC		PCA int Clear to	disable . Set to	bit o enable.					
5	ET2		Timer 2 Clear to Set to e	Timer 2 overflow interrupt Enable bit Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.						
4	ES		Serial p Clear to Set to e	Serial port Enable bit Clear to disable serial port interrupt. Set to enable serial port interrupt.						
3	ET1		Timer 1 Clear to Set to e	Timer 1 overflow interrupt Enable bit Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.						
2	EX1		Externa Clear to Set to e	External interrupt 1 Enable bit Clear to disable external interrupt 1. Set to enable external interrupt 1.						
1	ETO		Timer 0 Clear to Set to e	Timer 0 overflow interrupt Enable bit Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.						
0	EX0		Externa Clear to Set to e	External interrupt 0 Enable bit Clear to disable external interrupt 0. Set to enable external interrupt 0.						

Reset Value = 0000 0000b

Bit addressable



IPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0		
-	РРСН	PT2H	PSH	PT1H	PX1H	РТОН	PX0H		
Bit Number	Bit Mnemonic	Descrip	Description						
7	-	Reserv The value	Reserved The value read from this bit is indeterminate. Do not set this bit.						
6	РРСН	PCA int <u>PPCHP</u> 0 1 1	errupt priority b <u>PC Priorit</u> 0 Lowest 1 0 1 Highest	it high. <u>y Level</u>					
5	PT2H	Timer 2 <u>PT2H P</u> 0 0 1 1	overflow intern T <u>2</u> <u>Priority</u> 0 Lowest 1 0 1 Highest	upt Priority High Level	n bit				
4	PSH	Serial p <u>PSH</u> 0 0 1 1	ort Priority High <u>PS Priority</u> 0Lowest 1 0 1Highest	n bit <u>Level</u>					
3	PT1H	Timer 1 <u>PT1HP</u> 0 0 1 1	overflow intern <u>T1Priority Leve</u> 0Lowest 1 0 1Highest	upt Priority High I	n bit				
2	PX1H	Externa <u>PX1HP</u> 0 0 1 1	l interrupt 1 Prio X <u>1Priority Leve</u> 0Lowest 1 0 1Highest	ority High bit I					
1	РТОН	Timer 0 <u>PT0HP</u> 0 0 1 1	overflow intern T <u>0</u> <u>Priority</u> 0 Lowest 1 0 1 Highest	upt Priority High Level	n bit				
0	РХОН	Externa <u>PX0HP2</u> 0 0 1 1	l interrupt 0 Prio <u>X0 Priority</u> 0 Lowest 1 0 1 Highest	ority High bit <u>Level</u>					

Reset Value = X000 0000b

Not bit addressable



8. TS83C51RB2/RC2/RD2 ROM

8.1 ROM Structure

The TS83C51RB2/RC2/RD2 ROM memory is divided in three different arrays:

- the code array:16/32/64 Kbytes.
- the encryption array:64 bytes.
- the signature array:4 bytes.

8.2 ROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

8.2.1 8.2.1 Encryption Array

Within the ROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

8.2.2 Program Lock Bits

The lock bits when programmed according to Table 8-1. will provide different level of protection for the on-chip code and data.

Program Lock Bits				
Security level	LB1	LB2	LB3	Protection Description
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	Ρ	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, \overline{EA} is sampled and latched on reset.
3	U	Ρ	U	Same as level 1+ Verify disable. This security level is only available for 51RDX2 devices.

Table 8-1.	Program Lock bits

U: unprogrammed P: programmed

8.2.3 Signature bytes

The TS83C51RB2/RC2/RD2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 8.3.





8.2.4 Verify Algorithm

Refer to Section "Verify algorithm".

Table 11-1.	DC Parameters in Standard Voltage
-------------	-----------------------------------

Symbol	Parameter	Min	Тур	Мах	Unit	Test Conditions
V _{oh}	Output High Voltage, ports 1, 2, 3, 4, 5	V _{CC} - 0.3 V _{CC} - 0.7 V _{CC} - 1.5			V V V	I _{OH} = -10 μA I _{OH} = -30 μA I _{OH} = -60 μA V _{CC} = 5 V ± 10%
V _{OH1}	Output High Voltage, port 0	V _{CC} - 0.3 V _{CC} - 0.7 V _{CC} - 1.5			V V V	$I_{OH} = -200 \ \mu A$ $I_{OH} = -3.2 \ m A$ $I_{OH} = -7.0 \ m A$ $V_{CC} = 5 \ V \pm 10\%$
V _{OH2}	Output High Voltage,ALE, PSEN	V _{CC} - 0.3 V _{CC} - 0.7 V _{CC} - 1.5			> > >	$I_{OH} = -100 \ \mu A$ $I_{OH} = -1.6 \ m A$ $I_{OH} = -3.5 \ m A$ $V_{CC} = 5 \ V \pm 10\%$
R _{RST}	RST Pulldown Resistor	50	90 ⁽⁵⁾	200	kΩ	
I _{IL}	Logical 0 Input Current ports 1, 2, 3, 4, 5			-50	μA	Vin = 0.45 V
ILI	Input Leakage Current			±10	μA	0.45 V < Vin < V _{CC}
I _{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3, 4, 5			-650	μΑ	Vin = 2.0 V
C _{IO}	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz TA = 25°C
I _{PD}	Power-down Current		20 ⁽⁵⁾	50	μA	$2.0 \text{ V} < \text{V}_{\text{CC}} < 5.5 \text{ V}^{(3)}$
I _{CC} under RESET	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			1 + 0.4 Freq (MHz) @12MHz 5.8 @16MHz 7.4	mA	V _{CC} = 5.5 V ⁽¹⁾
I _{cc} operating	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			3 + 0.6 Freq (MHz) @12MHz 10.2 @16MHz 12.6	mA	V _{CC} = 5.5 V ⁽⁸⁾
l _{cc} idle	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			0.25+0.3 Freq (MHz) @12MHz 3.9 @16MHz 5.1	mA	V _{CC} = 5.5 V ⁽²⁾





11.5.9 EPROM Programming and Verification Characteristics

TA = 21°C to 27°C; V_{SS} = 0V; V_{CC} = 5V \pm 10% while programming. V_{CC} = operating range while

Symbol	Parameter	Min	Мах	Units
V _{PP}	Programming Supply Voltage	12.5	13	V
I _{PP}	Programming Supply Current		75	mA
1/T _{CLCL}	Oscillator Frquency	4	6	MHz
T _{AVGL}	Address Setup to PROG Low	48 T _{CLCL}		
T _{GHAX}	Adress Hold after PROG	48 T _{CLCL}		
T _{DVGL}	Data Setup to PROG Low	48 T _{CLCL}		
T _{GHDX}	Data Hold after PROG	48 T _{CLCL}		
T _{EHSH}	(Enable) High to V _{PP}	48 T _{CLCL}		
T _{SHGL}	V _{PP} Setup to PROG Low	10		μs
T _{GHSL}	V _{PP} Hold after PROG	10		μs
T _{GLGH}	PROG Width	90	110	μs
T _{AVQV}	Address to Valid Data		48 T _{CLCL}	
T _{ELQV}	ENABLE Low to Data Valid		48 T _{CLCL}	
T _{EHQZ}	Data Float after ENABLE	0	48 T _{CLCL}	

verifying

11.5.10 EPROM Programming and Verification Waveforms



Figure 11-10. EPROM Programming and Verification Waveforms

* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5



Part Number	Memory size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS83C51RB2-MCA			•	•		
TS83C51RB2-MCB						
TS83C51RB2-MCE						
TS83C51RB2-MIA						
TS83C51RB2-MIB						
TS83C51RB2-MIE						
TS83C51RB2-LCA						
TS83C51RB2-LCB						
TS83C51RB2-LCE				TE		
TS83C51RB2-LIA			OBSOLL			
TS83C51RB2-LIB						
TS83C51RB2-LIE						
TS83C51RB2-VCA						
TS83C51RB2-VCB						
TS83C51RB2-VCE						
TS83C51RB2-VIA						
TS83C51RB2-VIB						
TS83C51RB2-VIE						
AT83C51RB2-3CSUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PDIL40	Stick
AT83C51RB2-SLSUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PLCC44	Stick
AT83C51RB2-RLTUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	VQFP44	Tray
AT83C51RB2-3CSUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PDIL40	Stick
AT83C51RB2-SLSUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PLCC44	Stick
AT83C51RB2-RLTUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	VQFP44	Tray

Part Number	Memory size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS83C51RC2-MCA						
TS83C51RC2-MCB						
TS83C51RC2-MCE						
TS83C51RC2-MIA						
TS83C51RC2-MIB						
TS83C51RC2-MIE						
TS83C51RC2-LCA						
TS83C51RC2-LCB						
TS83C51RC2-LCE				TE		
TS83C51RC2-LIA			OBSOLL			
TS83C51RC2-LIB						
TS83C51RC2-LIE						
TS83C51RC2-VCA						
TS83C51RC2-VCB						
TS83C51RC2-VCE						
TS83C51RC2-VIA						
TS83C51RC2-VIB						
TS83C51RC2-VIE						
AT83C51RC2-3CSUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PDIL40	Stick
AT83C51RC2-SLSUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	PLCC44	Stick
AT83C51RC2-RLTUM	ROM 32k Bytes	5V	Industrial & Green	40 MHz (20 MHz X2)	VQFP44	Tray
AT83C51RC2-3CSUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PDIL40	Stick
AT83C51RC2-SLSUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	PLCC44	Stick
AT83C51RC2-RLTUL	ROM 32k Bytes	3-5V	Industrial & Green	30 MHz (20 MHz X2)	VQFP44	Tray





13.4 VQFP64

SQUARE GULL WING (1.4 mm)

