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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x8b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87lpc779fdh-529

5. Pinning information

5.1 Pinning

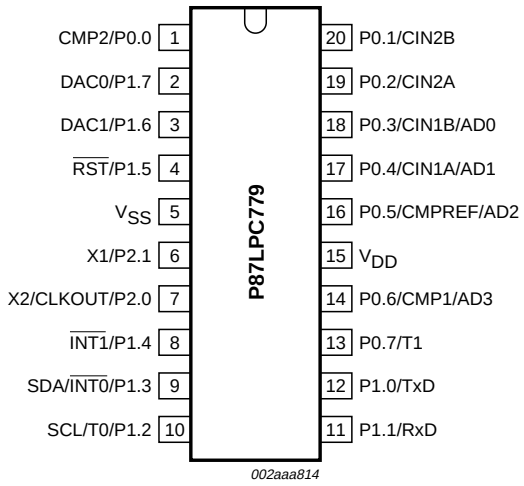


Fig 3. 20 pin DIP and SO configuration.

5.2 Pin description

Table 2: Pin description

Symbol	Pin	Type	Description
P0.0 - P0.7	1, 20-16, 14, 13	I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. Port 0 latches are configured in the quasi-bidirectional mode and have either ones or zeros written to them during reset, as determined by the PRHI bit in the UCFG1 configuration byte. The operation of port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.9 “I/O ports” and Table 55 “DC electrical characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. Port 0 also provides various special functions as described below:
P0.0	1	O	**CMP2 —** Comparator 2 output.
P0.1	20	I	**CIN2B —** Comparator 2 positive input B.
P0.2	19	I	**CIN2A —** Comparator 2 positive input A.
P0.3	18	I	**CIN1B —** Comparator 1 positive input B.
		I	**AD0 —** A/D channel 0 input.
P0.4	17	I	**CIN1A —** Comparator 1 positive input A.
		I	**AD1 —** A/D channel 1 input.
P0.5	16	I	**CMPREF —** Comparator reference (negative) input.
		I	**AD2 —** A/D channel 2 input.
P0.6	14	O	**CMP1 —** Comparator 1 output.
		I	**AD3 —** A/D channel 3 input.
P0.7	13	I/O	**T1 —** Timer/counter 1 external count input or overflow output.

6. Logic symbol

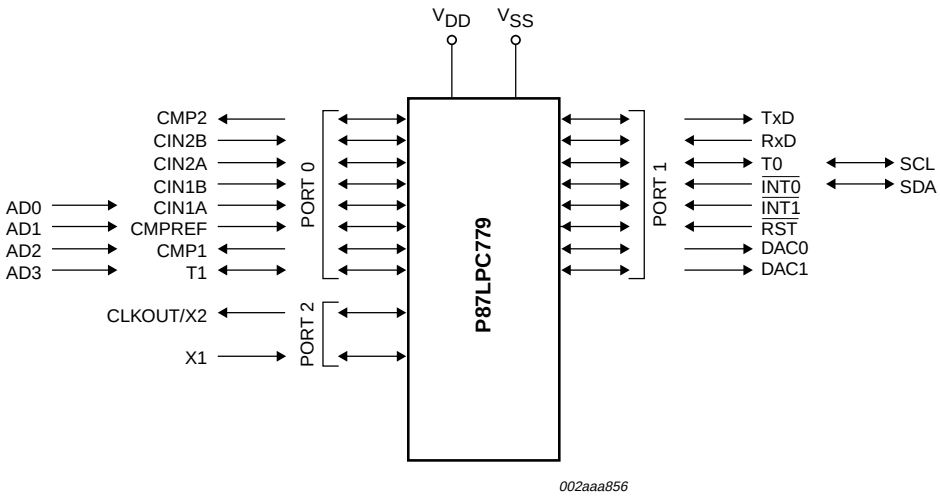


Fig 4. Logic symbol.

Table 5: ADCON - A/D control register (address C0h) bit description *...continued*

Bit	Symbol	Description
4	ADCI	A/D conversion complete/interrupt flag. This flag is set when an A/D conversion is completed. This bit will cause a hardware interrupt if enabled and of sufficient priority. Must be cleared by software.
3	ADCS	A/D start. Setting this bit by software starts the conversion of the selected A/D input. ADCS remains set while the A/D conversion is in progress and is cleared automatically upon completion. While ADCS or ADCI are one, new start commands are ignored. See Table 6.
2	RCCLK	When RCCLK = 0, the CPU clock is used as the A/D clock. When RCCLK = 1, the internal RC oscillator is used as the A/D clock. This bit is writable while ADCS and ADCI are 0.
1, 0	AADR1, 0	Along with AADR0, selects the A/D channel to be converted. These bits can only be written while ADCS and ADCI are 0. See Table 7.

Table 6: ADCON - ADCI, ADCS A/D status

ADCI, ADCS	A/D status
0 0	A/D not busy, a conversion can be started
0 1	A/D busy, the start of a new conversion is blocked.
1 0	An A/D conversion is complete. ADCI must be cleared prior to starting a new conversion.
1 1	An A/D conversion is complete. ADCI must be cleared prior to starting a new conversion. This state exists for one machine cycle as an A/D conversion is completed.

Table 7: ADCON - AADR1, AADR0 A/D input selection

AADR1, AADR0	A/D input selected
0 0	AD0 (P0.3)
0 1	AD1 (P0.4)

8.4 A/D timing

The A/D may be clocked in one of two ways. The default is to use the CPU clock as the A/D clock source. When used in this manner, the A/D completes a conversion in 31 machine cycles. The A/D may be operated up to the maximum CPU clock rate of 20 MHz, giving a conversion time of 9.3 µs. The formula for calculating A/D conversion time when the CPU clock runs the A/D is: 186 µs / CPU clock rate (in MHz). To obtain accurate A/D conversion results, the CPU clock must be at least 1 MHz.

The A/D may also be clocked by the on-chip RC oscillator, even if the RC oscillator is not used as the CPU clock. This is accomplished by setting the RCCLK bit in ADCON. This arrangement has several advantages. First, the A/D conversion time is faster at lower CPU clock rates. Also, the CPU may be run at speeds below 1 MHz without affecting A/D accuracy. Finally, the Power-down mode may be used to completely shut down the CPU and its oscillator, along with other peripheral functions, in order to obtain the best possible A/D accuracy.

```
ADRead:
 orl  ADCON,A      ; Add in the new channel number.
 setb ADCS         ; Start A/D conversion.
ADChk:
 jnb  ADCI,ADChk   ; Wait for ADCI to be set.
 mov  A,DAC0       ; Get A/D result.
 clr  ADCI         ; Clear the A/D completion flag.
 anl  ADCON,#0fch  ; Clear the A/D channel number.
 ret
```

8.5 Digital to Analog Converter (DAC) outputs

The P87LPC779 provides a two channel, 8-bit DAC function. DAC0 is also part of the A/D Converter and is should not be enabled while the A/D is active. The DAC outputs function down to a V_{DD} of 3.0 V. Digital outputs must be disabled on the DAC output pins while the corresponding DAC is enabled, as described in Section 8.2 “Analog functions” on page 12.

The DACs use the power supply as the references: V_{DD} as the upper reference and VSS as the lower reference. The DAC output is generated by a tap from a resistor ladder and is not buffered. The maximum resistance to V_{DD} or V_{SS} from a DAC output is 10 kΩ. Care must be taken with the loading of the DAC outputs in order to avoid distortion of the output voltage. DAC accuracy is affected by noise generated on-chip and elsewhere in the application. Since the P87LPC779 power pins are used for the DAC references, the power supply also affects the accuracy of the DAC outputs.

The ideal DAC output may be calculated as follows:

$$\text{Result} = (\text{DAC value} + 0.5) \times \frac{V_{DD} - V_{SS}}{256} \quad (2)$$

where DAC Value is the contents of the relevant DAC register: DAC0 or DAC1.

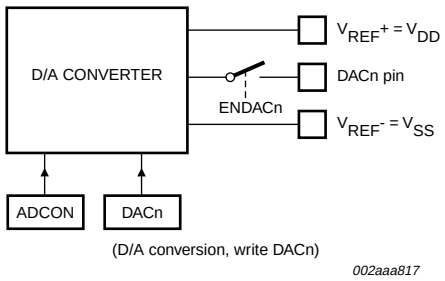


Fig 6. DAC block diagram.

8.6 Analog comparators

Two analog comparators are provided on the P87LPC779. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logic 1 (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable pins) is greater than the

negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.

8.6.1 Comparator configuration

Each comparator has a control register, CMP1 for comparator 1 and CMP2 for comparator 2. The control registers are identical and are shown in Tables 9 and 10.

The overall connections to both comparators are shown in Figure 7. There are eight possible configurations for each comparator, as determined by the control bits in the corresponding CMPn register: CPn, CNn, and OEn. These configurations are shown in Figure 8. The comparators function down to a V_{DD} of 3.0 V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 μs. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

Table 9: CMPn - Comparator control registers CMP1 and CMP2 (address ACh for CMP1, ADh for CMP2) bit allocation

Not bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	CEn	CPn	CNn	OEn	COn	CMFn

Table 10: CMPn - Comparator control registers CMP1 and CMP2 (address ACh for CMP1, ADh for CMP2) bit description

Bit	Symbol	Description
7, 6	-	Reserved for future use. Should not be set to ‘1’ by user programs.
5	CEn	Comparator enable. When set by software, the corresponding comparator function is enabled. Comparator output is stable 10 μs after CEn is first set.
4	CPn	Comparator positive input select. When ‘0’, CINnA is selected as the positive comparator input. When ‘1’, CINnB is selected as the positive comparator input.
3	CNn	Comparator negative input select. When ‘0’, the comparator reference pin CMPREF is selected as the negative comparator input. When ‘1’, the internal comparator reference Vref is selected as the negative comparator input.
2	OEn	Output enable. When ‘1’, the comparator output is connected to the CMPn pin if the comparator is enabled (CEn = 1). This output is asynchronous to the CPU clock.
1	COn	Comparator output, synchronized to the CPU clock to allow reading by software. Cleared when the comparator is disabled (CEn = 0).
0	CMFn	Comparator interrupt flag. This bit is set by hardware whenever the comparator output COn changes state. This bit will cause a hardware interrupt if enabled and of sufficient priority. Cleared by software and when the comparator is disabled (CEn = 0).

8.6.3 Comparator interrupt

Each comparator has an interrupt flag CMFn contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The interrupt will be generated when the corresponding enable bit ECn in the IEN1 register is set and the interrupt system is enabled via the EA bit in the IEN0 register.

8.6.4 Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated. The comparators will continue to function in the power reduction mode. If a comparator interrupt is enabled, a change of the comparator output state will generate an interrupt and wake up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the oscillator stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue.

8.6.5 Comparator configuration example

The code shown below is an example of initializing one comparator. Comparator 1 is configured to use the CIN1A and CMPREF inputs, outputs the comparator result to the CMP1 pin, and generates an interrupt when the comparator output changes.

```
CmpInit: b
  mov   PT0AD,#30h    ; Disable digital inputs on pins that are used
                      ;   for analog functions: CIN1A, CMPREF.
  anl   P0M2,#0cfh    ; Disable digital outputs on pins that are used
  orl   P0M1,#30h     ;   for analog functions: CIN1A, CMPREF.
  mov   CMP1,#24h     ; Turn on comparator 1 and set up for:
                      ;   - Positive input on CIN1A.
                      ;   - Negative input from CMPREF pin.
                      ;   - Output to CMP1 pin enabled.
  call  delay10us     ; The comparator has to start up for at
                      ;   least 10 microseconds before use.
  anl   CMP1,#0feh    ; Clear comparator 1 interrupt flag.
  setb  EC1           ; Enable the comparator 1 interrupt. The
                      ;   priority is left at the current value.
  setb  EA            ; Enable the interrupt system (if needed).
  ret                 ; Return to caller.
```

The interrupt routine used for the comparator must clear the interrupt flag (CMF1 in this case) before returning.

8.7 I²C-bus serial interface

The I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Bidirectional data transfer between masters and slaves.
- Serial addressing of slaves (no added wiring).

8.7.4 Writing I2CON

Typically, for each bit in an I²C-bus message, a service routine waits for ATN = 1. Based on DRDY, ARL, STR, and STP, and on the current bit position in the message, it may then write I2CON with one or more of the following bits, or it may read or write the I2DAT register.

CXA — Writing a '1' to 'Clear Xmit Active' clears the Transmit Active state. (Reading the I2DAT register also does this.)

8.7.5 Regarding Transmit Active

Transmit Active is set by writing the I2DAT register, or by writing I2CON with XSTR = 1 or XSTP = 1. The I²C-bus interface will only drive the SDA line low when Transmit Active is set, and the ARL bit will only be set to '1' when Transmit Active is set. Transmit Active is cleared by reading the I2DAT register, or by writing I2CON with CXA = 1. Transmit Active is automatically cleared when ARL is '1'.

IDLE — Writing '1' to 'IDLE' causes a slave's I²C-bus hardware to ignore the I²C-bus until the next start condition (but if MASTRQ is '1', then a stop condition will cause this device to become a master).

CDR — Writing a '1' to 'Clear Data Ready' clears DRDY. (Reading or writing the I2DAT register also does this.)

CARL — Writing a '1' to 'Clear Arbitration Loss' clears the ARL bit.

CSTR — Writing a '1' to 'Clear STaRt' clears the STR bit.

CSTP — Writing a '1' to 'Clear SToP' clears the STP bit. Note that if one or more of DRDY, ARL, STR, or STP is '1', the low time of SCL is stretched until the service routine responds by clearing them.

XSTR — Writing '1's to 'Xmit repeated STaRt' and CDR tells the I²C-bus hardware to send a repeated start condition. This should only be at a master. Note that XSTR need not and should not be used to send an 'initial' (non-repeated) start; it is sent automatically by the I²C-bus hardware. Writing XSTR = '1' includes the effect of writing I2DAT with XDAT = '1'; it sets Transmit Active and releases SDA to HIGH during the SCL low time. After SCL goes HIGH, the I²C-bus hardware waits for the suitable minimum time and then drives SDA low to make the start condition.

XSTP — Writing 1s to 'Xmit SToP' and CDR tells the I²C-bus hardware to send a stop condition. This should only be done at a master. If there are no more messages to initiate, the service routine should clear the MASTRQ bit in I2CFG to '0' before writing XSTP with '1'. Writing XSTP = '1' includes the effect of writing I2DAT with XDAT = '0'; it sets Transmit Active and drives SDA low during the SCL low time. After SCL goes HIGH, the I²C-bus hardware waits for the suitable minimum time and then releases SDA to HIGH to make the stop condition.

Table 13: I2DAT - I²C-bus data register (address D9H) bit allocation

Not bit addressable; Reset value: xxH

Bit	7	6	5	4	3	2	1	0
Symbol (R)	RDAT	-	-	-	-	-	-	-
Symbol (W)	XDAT	-	-	-	-	-	-	-

Table 19: Summary of interrupts...*continued*

Description	Interrupt Flag Bit(s)	Vector Address	Interrupt Enable Bit(s)	Interrupt Priority	Arbitration Ranking	Power-down Wake-up
A/D Converter	ADCI	005Bh	EAD (IEN1.4)	IP1H.4, IP1.4	6	Yes
Comparator 1 interrupt	CMF1	0063h	EC1 (IEN1.5)	IP1H.5, IP1.5	9	Yes
Timer I interrupt	-	0073h	ETI (IEN1.7)	IP1H.7, IP1.7	13 (lowest)	No

8.8.1 External interrupt inputs

The P87LPC779 has two individual interrupt inputs as well as the Keyboard Interrupt function. The latter is described separately elsewhere in this section. The two interrupt inputs are identical to those present on the standard 80C51 microcontroller.

The external sources can be programmed to be level-activated or transition-activated by setting or clearing bit IT1 or IT0 in Register TCON. If ITn = 0, external interrupt n is triggered by a detected low at the $\overline{\text{INTn}}$ pin. If ITn = 1, external interrupt n is edge triggered. In this mode if successive samples of the $\overline{\text{INTn}}$ pin show a high in one cycle and a low in the next cycle, interrupt request flag IEn in TCON is set, causing an interrupt request.

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least 6 CPU Clocks to ensure proper sampling. If the external interrupt is transition-activated, the external source has to hold the request pin high for at least one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the transition is seen and that interrupt request flag IEn is set. IEn is automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source must hold the request active until the requested interrupt is actually generated. If the external interrupt is still asserted when the interrupt service routine is completed another interrupt will be generated. It is not necessary to clear the interrupt flag IEn when the interrupt is level sensitive, it simply tracks the input pin level.

If an external interrupt is enabled when the P87LPC779 is put into Power-down or Idle mode, the interrupt will cause the processor to wake up and resume operation. Refer to Section 8.12 “Power reduction modes” on page 38 for details.

8.9.4 Keyboard interrupt (KBI)

The Keyboard Interrupt function is intended primarily to allow a single interrupt to be generated when any key is pressed on a keyboard or keypad connected to specific pins of the P87LPC779, as shown in Figure 13. This interrupt may be used to wake up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery powered systems that need to carefully manage power consumption yet also need to be convenient to use.

The P87LPC779 allows any or all pins of port 0 to be enabled to cause this interrupt. Port pins are enabled by the setting of bits in the KBI register, as shown in Tables 23 and 24. The Keyboard Interrupt Flag (KBF) in the AUXR1 register is set when any enabled pin is pulled LOW while the KBI interrupt function is active. An interrupt will be generated if it has been enabled. Note that the KBF bit must be cleared by software.

Due to human time scales and the mechanical delay associated with keyswitch closures, the KBI feature will typically allow the interrupt service routine to poll port 0 in order to determine which key was pressed, even if the processor has to wake up from Power-down mode. Refer to Section 8.12 “Power reduction modes” on page 38 for details.

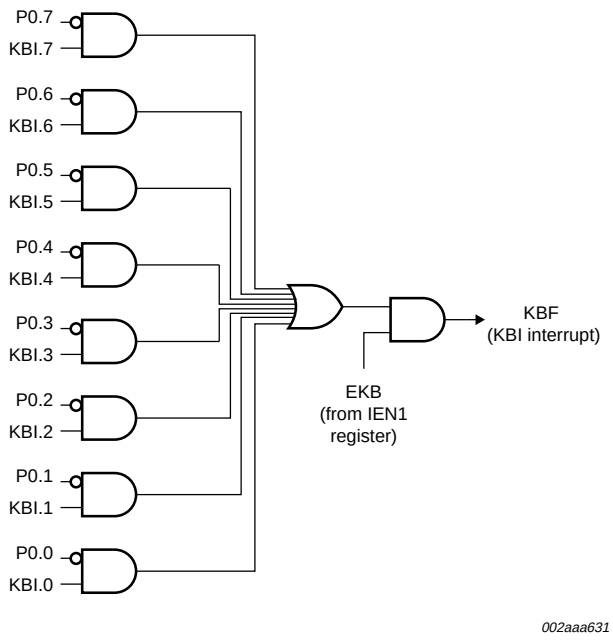


Fig 13. Keyboard interrupt.

Table 23: KBI - Keyboard interrupt register (address 86H) bit allocation

Not bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0

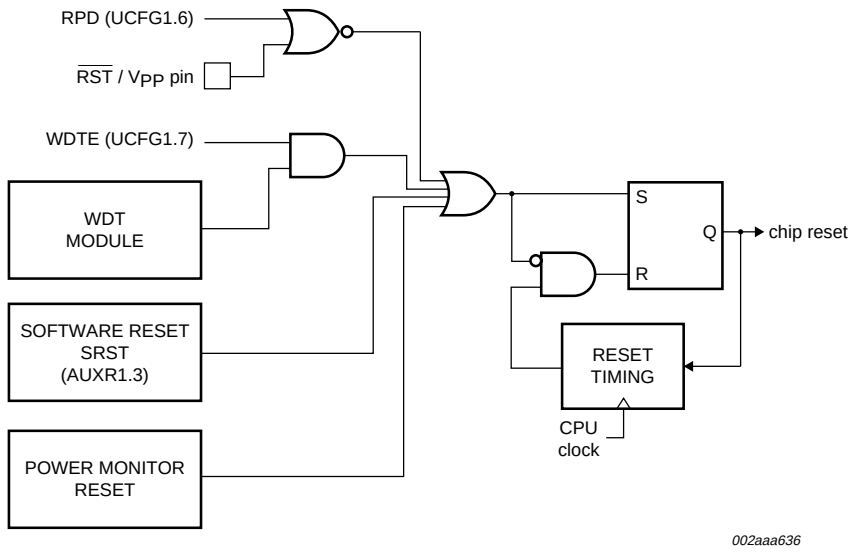


Fig 18. Block diagram showing reset sources.

8.14 Timer/counters

The P87LPC779 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer0 and Timer1. Both can be configured to operate either as timers or event counters (see Tables 31 and 32). An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the 'Timer' function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of 6 CPU clock periods, the count rate is $\frac{1}{6}$ of the CPU clock frequency. Refer to Section 8.1 "Enhanced CPU" on page 12 for a description of the CPU clock.

In the 'Counter' function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle. When the samples of the pin state show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (12 CPU clocks) to recognize a 1-to-0 transition, the maximum count rate is $\frac{1}{6}$ of the CPU clock frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

The 'Timer' or 'Counter' function is selected by control bits C/T in the Special Function Register TMOD. In addition to the 'Timer' or 'Counter' selection, Timer0 and Timer1 have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different. The four operating modes are described in the following text.

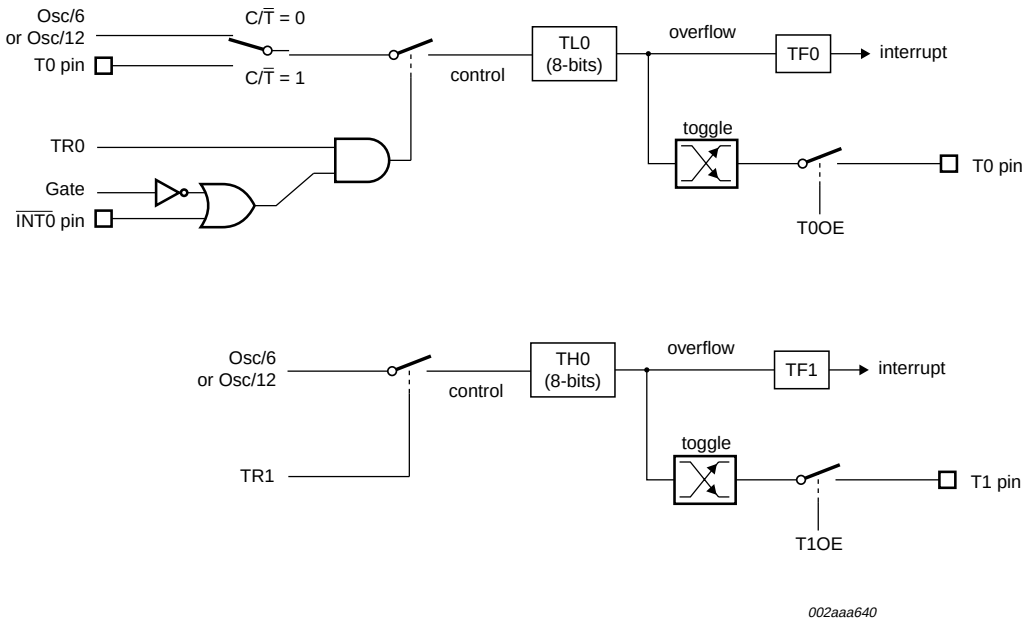


Fig 22. Timer/counter 0 Mode 3 (two 8-bit counters).

8.14.5 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. This function is enabled by control bits ENT0 and ENT1 in the P2M1 register, and apply to Timer0 and Timer1 respectively. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

8.15 UART

The P87LPC779 includes an enhanced 80C51 UART. The baud rate source for the UART is Timer1 for modes 1 and 3, while the rate is fixed in modes 0 and 2. Because CPU clocking is different on the P87LPC779 than on the standard 80C51, baud rate calculation is somewhat different. Enhancements over the standard 80C51 UART include Framing Error detection and automatic address recognition.

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the SBUF register. However, if the first byte still hasn't been read by the time reception of the second byte is complete, the first byte will be lost. The serial port receive and transmit registers are both accessed through Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port can be operated in 4 modes.

Table 37: SCON - Serial port control register (address 98H) bit description

Bit	Symbol	Description
7	FE	Framing Error. This bit is set by the UART receiver when an invalid stop bit is detected. Must be cleared by software. The SMOD0 bit in the PCON register must be '1' for this bit to be accessible. See SM0 bit below.
	SM0	With SM1, defines the serial port mode. The SMOD0 bit in the PCON register must be '0' for this bit to be accessible. See FE bit above.
6	SM1	With SM0, defines the serial port mode (see Table 38 below).
5	SM2	Enables the multiprocessor communication feature in Modes 2 and 3. In Mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In Mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit was not received. In Mode 0, SM2 should be 0.
4	REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
3	TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
2	RB8	In Modes 2 and 3, is the 9th data bit that was received. In Mode 1, it SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
1	TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
0	RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Table 38: SM0, SM1 serial port mode

SM0, SM1	UART mode	Baud rate
0 0	0: shift register	CPU clock/6
0 1	1: 8-bit UART	variable (see text)
1 0	2: 9-bit UART	CPU clock/32 or CPU clock/16
1 1	3: 9-bit UART	variable (see text)

8.15.6 Baud rates

The baud rate in Mode 0 is fixed: Mode 0 Baud Rate = CPU clock/6. The baud rate in Mode 2 depends on the value of bit SMOD1 in Special Function Register PCON. If SMOD1 = 0 (which is the value on reset), the baud rate is $1/32$ of the CPU clock frequency. If SMOD1 = 1, the baud rate is $1/16$ of the CPU clock frequency.

$$\text{Mode 2 baud rate} = \frac{1 + SMOD1}{32} \times \text{CPU clock frequency} \quad (4)$$

Table 40: Baud rates, timer values, and CPU clock frequencies for SMOD1 = 1*...continued*

Timer Value	Baud Rate						
	2400	4800	9600	19.2 k	38.4 k	57.6 k	115.2 k
–15	3.4560	6.9120	13.8240	-	-	-	-
–16	* 3.6864	* 7.3728	* 14.7456	-	-	-	-
–17	3.9168	7.8336	15.6672	-	-	-	-
–18	4.1472	8.2944	16.5888	-	-	-	-
–19	4.3776	8.7552	17.5104	-	-	-	-
–20	4.6080	9.2160	* 18.4320	-	-	-	-
–21	4.8384	9.6768	19.3536	-	-	-	-

[1] Tables 39 and 40 apply to UART modes 1 and 3 (variable rate modes), and show CPU clock rates in MHz for standard baud rates from 2400 to 115.2 kbaud.

[2] Table 39 shows timer settings and CPU clock rates with the SMOD1 bit in the PCON register = 0 (the default after reset), while Table 40 reflects the SMOD1 bit = 1.

[3] The tables show all potential CPU clock frequencies up to 20 MHz that may be used for baud rates from 9600 baud to 115.2 kbaud. Other CPU clock frequencies that would give only lower baud rates are not shown.

[4] Table entries marked with an asterisk (*) indicate standard crystal and ceramic resonator frequencies that may be obtained from many sources without special ordering.

8.15.8 More about UART Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at $\frac{1}{6}$ the CPU clock frequency. Figure 23 shows a simplified functional diagram of the serial port in Mode 0, and associated timing.

Transmission is initiated by any instruction that uses SBUF as a destination register. The ‘write to SBUF’ signal at S6P2 also loads a ‘1’ into the 9th position of the transmit shift register and tells the TX Control block to commence a transmission. The internal timing is such that one full machine cycle will elapse between ‘write to SBUF’ and activation of SEND.

SEND enables the output of the shift register to the alternate output function line of P3.0 and also enable SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK is low during S3, S4, and S5 of every machine cycle, and high during S6, S1, and S2. At S6P2 of every machine cycle in which SEND is active, the contents of the transmit shift are shifted to the right one position.

As data bits shift out to the right, zeros come in from the left. When the MSB of the data byte is at the output position of the shift register, then the ‘1’ that was initially loaded into the 9th position, is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control block to do one last shift and then deactivate SEND and set T1. Both of these actions occur at S1P1 of the 10th machine cycle after ‘write to SBUF.’ Reception is initiated by the condition REN = 1 and R1 = 0. At S6P2 of the next machine cycle, the RX Control unit writes the bits 11111110 t o the receive shift register, and in the next clock phase activates RECEIVE.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are 'don't care'. The SADEN mask can be logically ANDed with the SADDR to create the 'Given' address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Table 41: Slave 0/1 examples

Example 1			Example 2		
Slave 0	SADDR =	1100 0000	Slave 1	SADDR =	1100 0000
	SADEN =	1111 1101		SADEN =	1111 1110
	Given =	1100 00X0		Given =	1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a '0' in bit 0 and it ignores bit 1. Slave 1 requires a '0' in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a '0' in bit 1. A unique address for slave 1 would be 1100 0001 since a '1' in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Table 42: Slave 0/1/2 examples

Example 1			Example 2			Example 3		
Slave 0	SADDR =	1100 0000	Slave 1	SADDR =	1110 0000	Slave 2	SADDR =	1110 0000
	SADEN =	1111 1001		SADEN =	1111 1010		SADEN =	1111 1100
	Given =	1100 0XX0		Given =	1110 0X0X		Given =	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2. The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal. Upon reset SADDR and SADEN are loaded with 0s. This produces a given address of all 'don't cares' as well as a Broadcast address of all 'don't cares'. This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard UART drivers which do not make use of this feature.

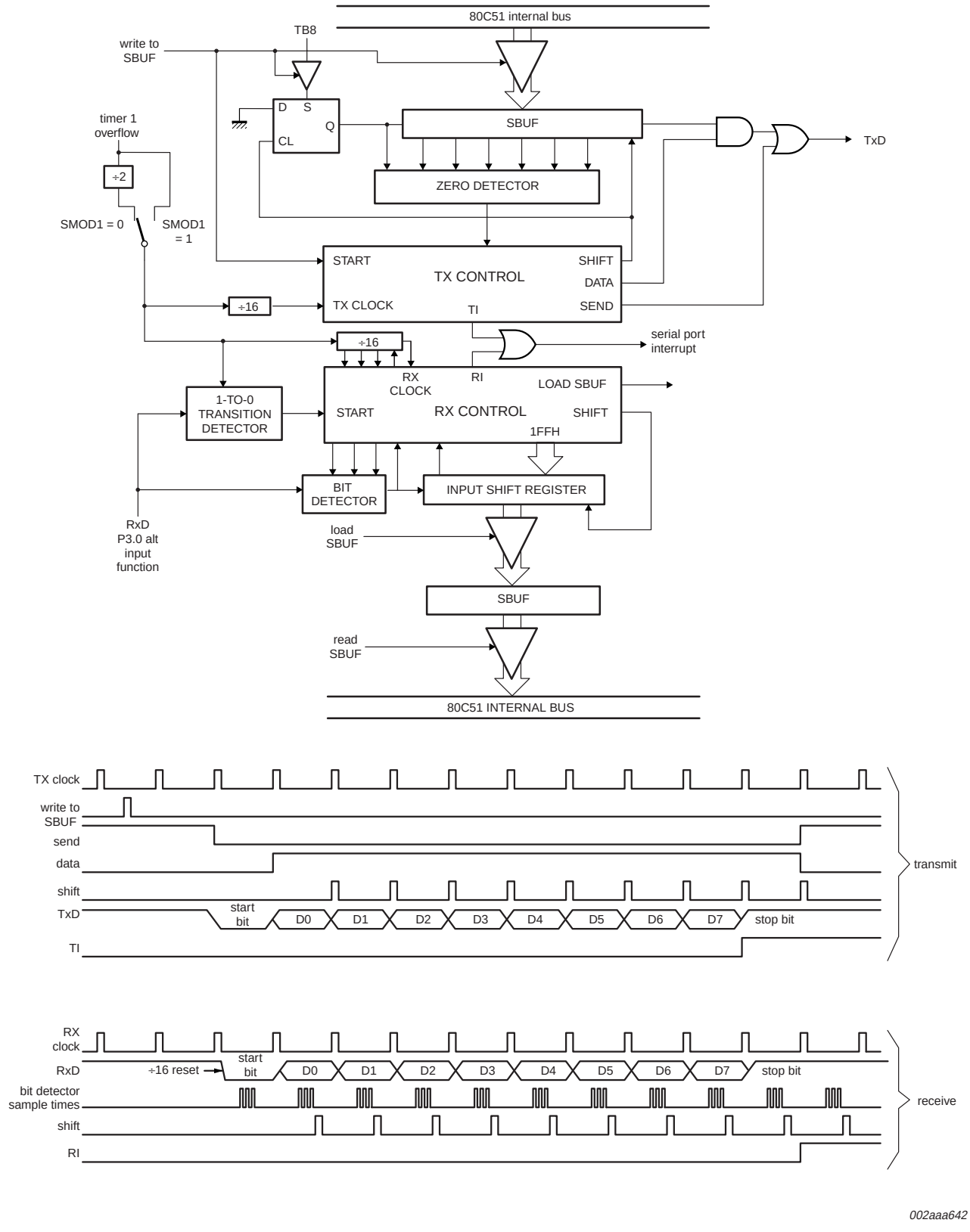


Fig 24. Serial port mode 1.

8.16 Watchdog timer

When enabled via the WDTE configuration bit, the Watchdog timer is operated from an independent, fully on-chip oscillator in order to provide the greatest possible dependability. When the Watchdog feature is enabled, the timer must be fed regularly by software in order to prevent it from resetting the CPU, and it **cannot** be turned off. When disabled as a Watchdog timer (via the WDTE bit in the UCFG1 configuration register), it may be used as an interval timer and may generate an interrupt. The Watchdog timer is shown in Figure 27.

The Watchdog timeout time is selectable from one of eight values, nominal times range from 16 milliseconds to 2.1 seconds. The frequency tolerance of the independent Watchdog RC oscillator is ±37 %. The timeout selections and other control bits are shown in Tables 43 and 44. When the Watchdog function is enabled, the WDCON register may be written **once** during chip initialization in order to set the Watchdog timeout time. The recommended method of initializing the WDCON register is to first feed the Watchdog, then write to WDCON to configure the WDS2-0 bits. Using this method, the Watchdog initialization may be done any time within 10 milliseconds after start-up without a Watchdog overflow occurring before the initialization can be completed.

Since the Watchdog timer oscillator is fully on-chip and independent of any external oscillator circuit used by the CPU, it intrinsically serves as an oscillator fail detection function. If the Watchdog feature is enabled and the CPU oscillator fails for any reason, the Watchdog timer will time out and reset the CPU.

When the Watchdog function is enabled, the timer is deactivated temporarily when a chip reset occurs from another source, such as a Power-on reset, brownout reset, or external reset.

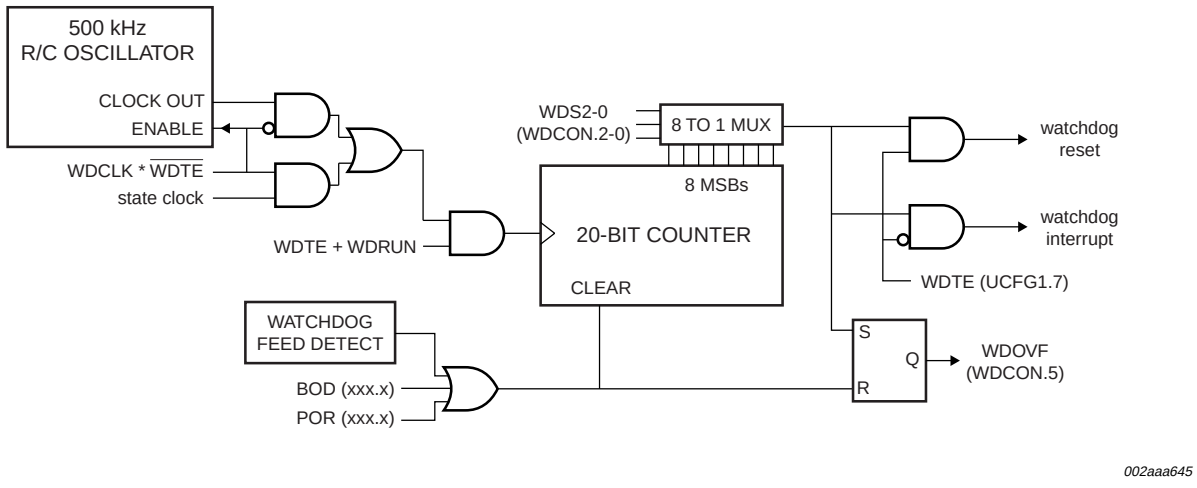


Fig 27. Block diagram of the Watchdog timer.

A special user data area is also available for access via the MOVC instruction at addresses FCE0h through FCFFh. This ‘customer code’ space is programmed in the same manner as the main code EPROM and may be used to store a serial number, manufacturing date, or other application information.

8.18.1 System configuration bytes

A number of user configurable features of the P87LPC779 must be defined at power up and therefore cannot be set by the program after start of execution. Those features are configured through the use of two EPROM bytes that are programmed in the same manner as the EPROM program space. The contents of the two configuration bytes, UCFG1 and UCFG2, are shown in Tables 48, 49, 51 and 52. The values of these bytes may be read by the program through the use of the MOVX instruction at the addresses shown in the tables.

Table 48: UCFG1 - EPROM system configuration byte 1 register (address FD00H) bit allocation

Unprogrammed value: FFH

Bit	7	6	5	4	3	2	1	0
Symbol	WDTE	RPD	PRHI	BOV	CLKR	FOSC2	FOSC1	FOSC0

Table 49: UCFG1 - EPROM system configuration byte 1 register (address FD00H) bit description

Bit	Symbol	Description
7	WDTE	Watchdog timer enable. When programmed (0), disables the Watchdog timer. The timer may still be used to generate an interrupt.
6	RPD	Reset pin disable. When programmed (0), disables the reset function of pin P1.5, allowing it to be used as an input only port pin.
5	PRHI	Port reset high. When ‘1’, ports reset to a high state. When ‘0’, ports reset to a low state.
4	BOV	Brownout voltage select. When ‘1’, the brownout detect voltage is 2.5 V. When ‘0’, the brownout detect voltage is 3.8 V. This is described in Section 8.11 “Power monitoring functions” on page 37.
3	CLKR	Clock rate select. When ‘0’, the CPU clock rate is divided by 2. This results in machine cycles taking 12 CPU clocks to complete as in the standard 80C51. For full backward compatibility, this division applies to peripheral timing as well.
2 to 0	FOSC[2:0]	CPU oscillator type select. See Section 8.10 “Oscillator” on page 34 for additional information. Combinations other than those shown below should not be used. They are reserved for future use.

Table 50: FOSC2-FOSC0 oscillator configuration

FOSC2-FOSC0	Oscillator configuration
1 1 1	External clock input on X1 (default setting for an unprogrammed part).
0 1 1	Internal RC oscillator, 6 MHz.

Table 55: DC electrical characteristics *...continued*

V_{DD} = 2.7 V to 5.5 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for extended industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{BOLOW}	brownout trip voltage with BOV = 1[11]		2.35	-	2.69	V
V_{BOHI}	brownout trip voltage with BOV = 0[12]		3.45	3.8	3.99	V
V_{REF}	bandgap reference voltage		1.11	1.26	1.41	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 5 V.

[2] Ports in quasi-bidirectional mode with weak pull-up (applies to all port pins with pull-ups). Does not apply to open-drain pins.

[3] Ports in PUSH-PULL mode. Does not apply to open drain pins.

[4] In all output modes except high impedance mode.

[5] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from '1' to '0'. This current is highest when V_{IN} is approximately 2 V.

[6] Measured with port in high-impedance mode. Parameter is guaranteed, but not tested at cold temperature.

[7] Measured with port in quasi-bidirectional mode.

[8] Under steady state (non-transient conditions, I_{OL} must be externally limited as follows.

a) Maximum I_{OL} per port pin: 20 mA

b) Maximum I_{OL} for all outputs: 80 mA

c) Maximum I_{OL} for all outputs: 5 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

[9] Pin capacitance is characterized but not tested.

[10] The I_{DD}, I_{ID}, and I_{PD} specifications are measured using an external clock with the following functions disabled: comparators, brownout detect, and Watchdog timer. For V_{DD} = 3 V, LPEP = 1. Refer to the appropriate figure on the following pages for additional current drawn by each of these functions.

[11] Devices initially operating at V_{DD} = 2.7 V or above and f_{osc} = 10 MHz or less are guaranteed to continue to execute instructions correctly at the brownout trip point. Initial power-on operation below V_{DD} = 2.7 V is not guaranteed.

[12] Devices initially operating at V_{DD} = 4.0 V or above and f_{osc} = 20 MHz or less are guaranteed to continue to execute instructions correctly at the brownout trip point. Initial power-on operation below V_{DD} = 4.0 V and f_{osc} > 10 MHz is not guaranteed

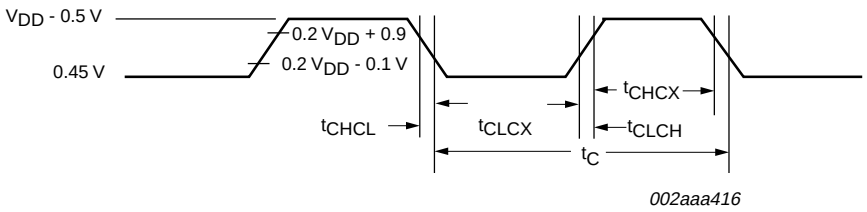


Fig 30. External clock timing.

12. Comparator electrical characteristics

Table 58: Comparator electrical characteristics

V_{DD} = 2.7 V to 5.5 V unless otherwise specified.
T_{amb} = –40 °C to +85 °C for extended industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IO}	Offset voltage comparator inputs[1]		-	-	±10	mV
V_{CR}	Common mode range comparator inputs		0	-	V_{DD} – 0.3	V
CMRR	Common mode rejection ratio[1]		-	-	–50	dB
	Response time		-	250	500	ns
	Comparator enable to output valid		-	-	10	µs
I_{IL}	Input leakage current, comparator	$0 < V_{IN} < V_{DD}$	-	-	±10	µA

[1] This parameter is characterized, but not tested in production.

13. D/A electrical characteristics

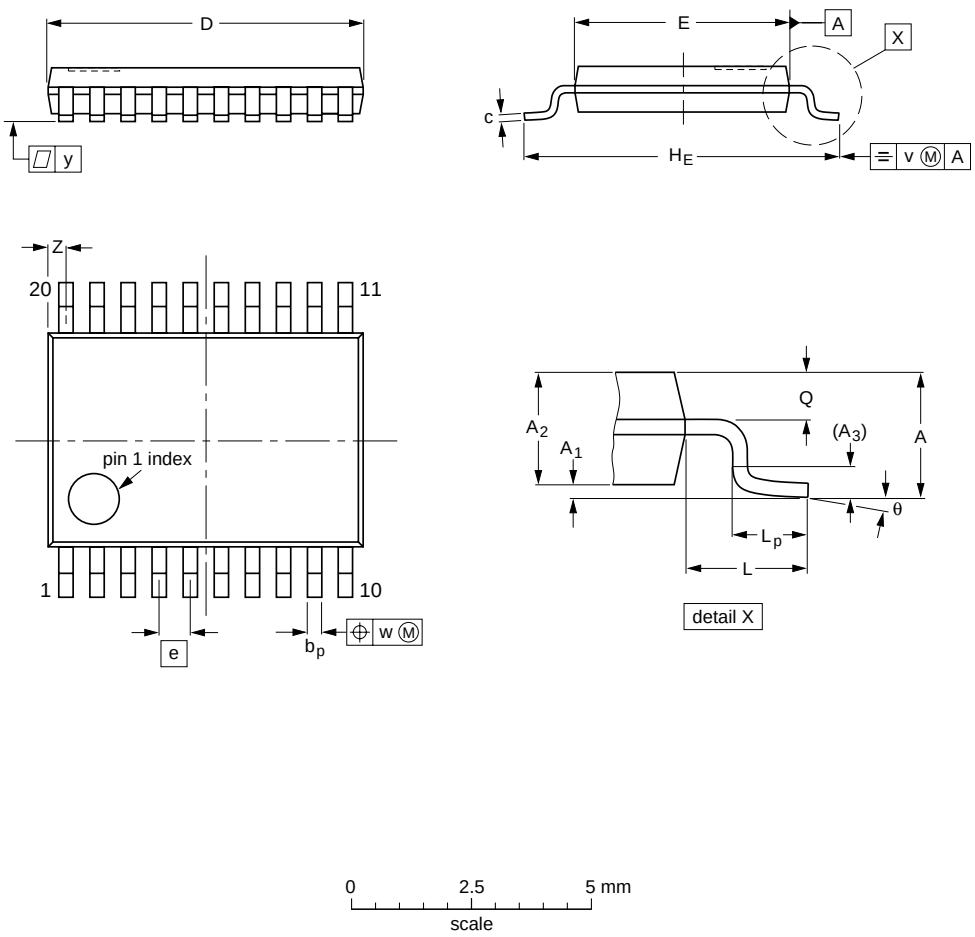
Table 59: D/A electrical characteristics

V_{DD} = 2.7 V to 5.5 V unless otherwise specified.
T_{amb} = –40 °C to +85 °C for extended industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog output						
V_{OA}	output voltage	no resistive load	V_{SS}	-	V_{DD}	V
		R_L = 100 k	$0.975 \times V_{DD}$	-	V_{DD}	V
		R_L = 10 k	$0.9 \times V_{DD}$	-	V_{DD}	V
$t_{DACrise}$	rise time 10 % to 90 % V_{DD}	no load	-	100	-	ns
		C_L = 100 pF	-	500	-	ns
$t_{DACfall}$	fall time 90 % to 10 % V_{DD}	no load	-	80	-	ns
		C_L = 100 pF	-	500	-	ns

14. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 31. SOT360-1.