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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	350MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	255-BBGA, FCBGA
Supplier Device Package	255-FCPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc745cpx350le

2 Features

This section summarizes features of the MPC755 implementation of the PowerPC architecture. Major features of the MPC755 are as follows:

- Branch processing unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving two speculations)
  - Up to one speculative stream in execution, one additional speculative stream in fetch
  - 512-entry branch history table (BHT) for dynamic prediction
  - 64-entry, four-way set-associative branch target instruction cache (BTIC) for eliminating branch delay slots
- Dispatch unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point)
  - Serialization control (predispatch, postdispatch, execution serialization)
- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - Six-entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization, and all instruction flow changes
- Fixed point units (FXUs) that share 32 GPRs for integer operands
  - Fixed Point Unit 1 (FXU1)—multiply, divide, shift, rotate, arithmetic, logical
  - Fixed Point Unit 2 (FXU2)—shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Floating-point unit and a 32-entry FPR file
  - Support for IEEE standard 754 single- and double-precision floating-point arithmetic
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Single-entry reservation station
  - Supports non-IEEE mode for time-critical operations
  - Three-cycle latency, one-cycle throughput, single-precision multiply-add

  - Three-cycle latency, one-cycle throughput, double-precision add
  - Four-cycle latency, two-cycle throughput, double-precision multiply-add
- System unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions
- Load/store unit
  - One-cycle load or store cache access (byte, half-word, word, double word)
  - Effective address generation
  - Hits under misses (one outstanding miss)
  - Single-cycle unaligned access within double-word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations
  - Store gathering
  - Cache and TLB instructions
  - Big- and little-endian byte addressing supported
- Level 1 cache structure
  - 32K, 32-byte line, eight-way set-associative instruction cache (iL1)
  - 32K, 32-byte line, eight-way set-associative data cache (dL1)
  - Cache locking for both instruction and data caches, selectable by group of ways
  - Single-cycle cache access
  - Pseudo least-recently-used (PLRU) replacement
  - Copy-back or write-through data cache (on a page per page basis)
  - MEI data cache coherency maintained in hardware
  - Nonblocking instruction and data cache (one outstanding miss under hits)
  - No snooping of instruction cache
- Level 2 (L2) cache interface (not implemented on MPC745)
  - Internal L2 cache controller and tags; external data SRAMs
  - 256K, 512K, and 1 Mbyte two-way set-associative L2 cache support
  - Copy-back or write-through data cache (on a page basis, or for all L2)
  - Instruction-only mode and data-only mode
  - 64-byte (256K/512K) or 128-byte (1M) sectored line size
  - Supports flow through (register-buffer) synchronous BurstRAMs, pipelined (register-register) synchronous BurstRAMs (3-1-1-1 or strobeless 4-1-1-1) and pipelined (register-register) late write synchronous BurstRAMs
  - L2 configurable to cache, private memory, or split cache/private memory
  - Core-to-L2 frequency divisors of ÷1, ÷1.5, ÷2, ÷2.5, and ÷3 supported
  - 64-bit data bus

Table 4. Package Thermal Characteristics [6]

Characteristic	Symbol	Value			Unit	Notes
		MPC755 CBGA	MPC755 PBGA	MPC745 PBGA		
Junction-to-ambient thermal resistance, natural convection	$R_{\theta JA}$	24	31	34	°C/W	1, 2
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JMA}$	17	25	26	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	18	25	27	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	14	21	22	°C/W	1, 3
Junction-to-board thermal resistance	$R_{\theta JB}$	8	17	17	°C/W	4
Junction-to-case thermal resistance	$R_{\theta JC}$	<0.1	<0.1	<0.1	°C/W	5

Notes:

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.
6. Refer to Section 8.8, "Thermal Management Information," for more details about thermal management.

The MPC755 incorporates a thermal management assist unit (TAU) composed of a thermal sensor, digital-to-analog converter, comparator, control logic, and dedicated special-purpose registers (SPRs). See the *MPC750 RISC Microprocessor Family User's Manual* for more information on the use of this feature. Specifications for the thermal sensor portion of the TAU are found in Table 5.

Table 5. Thermal Sensor Specifications

At recommended operating conditions (see Table 3)

Characteristic	Min	Max	Unit	Notes
Temperature range	0	127	°C	1
Comparator settling time	20	—	µs	2, 3
Resolution	4	—	°C	3
Accuracy	–12	+12	°C	3

Notes:

1. The temperature is the junction temperature of the die. The thermal assist unit's raw output does not indicate an absolute temperature, but must be interpreted by software to derive the absolute junction temperature. For information about the use and calibration of the TAU, see Freescale Application Note AN1800/D, *Programming the Thermal Assist Unit in the MPC750 Microprocessor.*
2. The comparator settling time value must be converted into the number of CPU clocks that need to be written into the THRM3 SPR.
3. Guaranteed by design and characterization.

Table 6 provides the DC electrical characteristics for the MPC755.

Table 6. DC Electrical Specifications

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage [1]	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs except SYSCLK)	2.5	V_{IH}	1.6	(L2)OV_{DD} + 0.3	V	2, 3
	3.3	V_{IH}	2.0	(L2)OV_{DD} + 0.3	V	2, 3
Input low voltage (all inputs except SYSCLK)	2.5	V_{IL}	–0.3	0.6	V	2
	3.3	V_{IL}	–0.3	0.8	V	
SYSCLK input high voltage	2.5	KV_{IH}	1.8	OV_{DD} + 0.3	V	
	3.3	KV_{IH}	2.4	OV_{DD} + 0.3	V	
SYSCLK input low voltage	2.5	KV_{IL}	–0.3	0.4	V	
	3.3	KV_{IL}	–0.3	0.4	V	
Input leakage current, V_{in} = L2OV_{DD}/OV_{DD}		I_{in}	—	10	µA	2, 3
High-Z (off-state) leakage current, V_{in} = L2OV_{DD}/OV_{DD}		I_{TSI}	—	10	µA	2, 3, 5
Output high voltage, I_{OH} = –6 mA	2.5	V_{OH}	1.7	—	V	
	3.3	V_{OH}	2.4	—	V	
Output low voltage, I_{OL} = 6 mA	2.5	V_{OL}	—	0.45	V	
	3.3	V_{OL}	—	0.4	V	

Table 6. DC Electrical Specifications (continued)

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage [1]	Symbol	Min	Max	Unit	Notes
Capacitance, V_{in} = 0 V, f = 1 MHz		C_{in}	—	5.0	pF	3, 4

Notes:

1. Nominal voltages; see Table 3 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD} while $L2OV_{DD}$ is the reference for the L2 bus signals.
3. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK) and IEEE 1149.1 boundary scan (JTAG) signals.
4. Capacitance is periodically sampled rather than 100% tested.
5. The leakage is measured for nominal OV_{DD} and V_{DD}, or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or –5%).

Table 7 provides the power consumption for the MPC755.

Table 7. Power Consumption for MPC755

	Processor (CPU) Frequency			Unit	Notes
	300 MHz	350 MHz	400 MHz		
Full-Power Mode					
Typical	3.1	3.6	5.4	W	1, 3, 4
Maximum	4.5	6.0	8.0	W	1, 2
Doze Mode					
Maximum	1.8	2.0	2.3	W	1, 2, 4
Nap Mode					
Maximum	1.0	1.0	1.0	W	1, 2, 4
Sleep Mode					
Maximum	550	550	550	mW	1, 2, 4
Sleep Mode (PLL and DLL Disabled)					
Maximum	510	510	510	mW	1, 2

Notes:

1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O supply power (OV_{DD} and $L2OV_{DD}$) or PLL/DLL supply power (AV_{DD} and $L2AV_{DD}$). OV_{DD} and $L2OV_{DD}$ power is system dependent, but is typically <10% of V_{DD} power. Worst case power consumption for AV_{DD} = 15 mW and $L2AV_{DD}$ = 15 mW.
2. Maximum power is measured at nominal V_{DD} (see Table 3) while running an entirely cache-resident, contrived sequence of instructions which keep the execution units maximally busy.
3. Typical power is an average value measured at the nominal recommended V_{DD} (see Table 3) and 65°C in a system while running a typical code sequence.
4. Not 100% tested. Characterized and periodically sampled.

4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC755. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section 4.2.1, "Clock AC Specifications," and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:3] signals. Parts are sold by maximum processor core frequency; see Section 10, "Ordering Information."

4.2.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications as defined in Figure 3.

Table 8. Clock AC Timing Specifications

At recommended operating conditions (see Table 3)

Characteristic	Symbol	Maximum Processor Core Frequency						Unit	Notes
		300 MHz		350 MHz		400 MHz			
		Min	Max	Min	Max	Min	Max		
Processor frequency	f_{core}	200	300	200	350	200	400	MHz	1
VCO frequency	f_{VCO}	400	600	400	700	400	800	MHz	1
SYSCLK frequency	f_{SYSCLK}	25	100	25	100	25	100	MHz	1
SYSCLK cycle time	t_{SYSCLK}	10	40	10	40	10	40	ns	
SYSCLK rise and fall time	t_{KR}, t_{KF}	—	2.0	—	2.0	—	2.0	ns	2
	t_{KR}, t_{KF}	—	1.4	—	1.4	—	1.4	ns	2
SYSCLK duty cycle measured at $OV_{DD}/2$	t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	%	3
SYSCLK jitter		—	±150	—	±150	—	±150	ps	3, 4
Internal PLL relock time		—	100	—	100	—	100	μs	3, 5

Notes:

1. **Caution:** The SYSCLK frequency and PLL_CFG[0:3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:3] signal description in Section 8.1, "PLL Configuration," for valid PLL_CFG[0:3] settings.
2. Rise and fall times measurements are now specified in terms of slew rates, rather than time to account for selectable I/O bus interface levels. The minimum slew rate of 1 V/ns is equivalent to a 2 ns maximum rise/fall time measured at 0.4 and 2.4 V (OV_{DD} = 3.3 V) or a rise/fall time of 1 ns measured at 0.4 and 1.8 V (OV_{DD} = 2.5 V).
3. Timing is guaranteed by design and characterization.
4. This represents total input jitter—short term and long term combined—and is guaranteed by design.
5. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 4 provides the mode select input timing diagram for the MPC755.

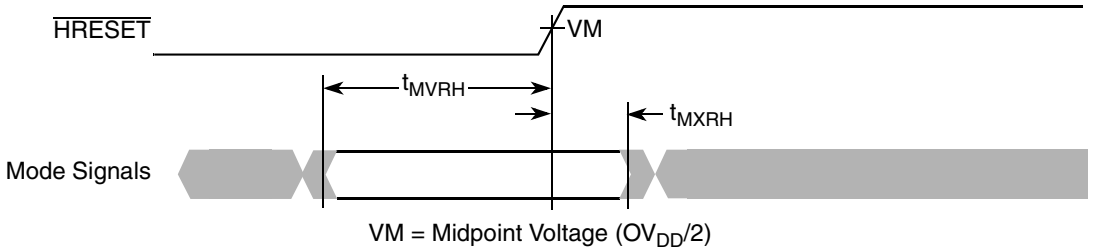


Figure 4. Mode Input Timing Diagram

Figure 5 provides the AC test load for the MPC755.

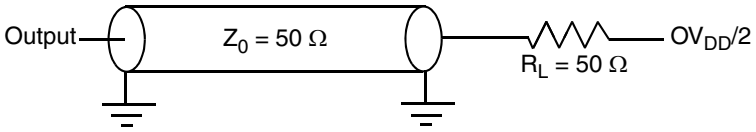


Figure 5. AC Test Load

Table 10. Processor Bus AC Timing Specifications [1]

At recommended operating conditions (see Table 3)

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
Setup times: All inputs	t_{IVKH}	2.5	—	ns	
Input hold times: $\overline{\text{TLBISYNC}}$, $\overline{\text{MCP}}$, $\overline{\text{SMI}}$	t_{IXKH}	0.6	—	ns	6
Input hold times: All inputs, except $\overline{\text{TLBISYNC}}$, $\overline{\text{MCP}}$, $\overline{\text{SMI}}$	t_{IXKH}	0.2	—	ns	6
Valid times: All outputs	t_{KHOV}	—	4.1	ns	
Output hold times: All outputs	t_{KHOX}	1.0	—	ns	
SYSCLK to output enable	t_{KHOE}	0.5	—	ns	2
SYSCLK to output high impedance (all except $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$)	t_{KHOZ}	—	6.0	ns	2
SYSCLK to $\overline{\text{ABB}}$, $\overline{\text{DBB}}$ high impedance after precharge	t_{KHABPZ}	—	1.0	t_{sysclk}	2, 3, 4
Maximum delay to $\overline{\text{ARTRY}}$ precharge	t_{KHARP}	—	1	t_{sysclk}	2, 3, 5
SYSCLK to $\overline{\text{ARTRY}}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{sysclk}	2, 3, 5

Notes:

1. Revisions prior to Rev. 2.8 (Rev. E) were limited in performance and did not conform to this specification. For more information, refer to Section 10.2, "Part Numbers Not Fully Addressed by This Document."
2. Guaranteed by design and characterization.
3. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. Per the 60x bus protocol, $\overline{\text{TS}}$, $\overline{\text{ABB}}$, and $\overline{\text{DBB}}$ are driven only by the currently active bus master. They are asserted low, then precharged high before returning to high-Z as shown in Figure 6. The nominal precharge width for $\overline{\text{TS}}$, $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ is $0.5 \times t_{sysclk}$, that is, less than the minimum t_{sysclk} period, to ensure that another master asserting $\overline{\text{TS}}$, $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
5. Per the 60x bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue since any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{sysclk}; that is, it should be high-Z as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z and precharge behavior is guaranteed by design.
6. $\overline{\text{MCP}}$ and $\overline{\text{SRESET}}$ must be held asserted for a minimum of two bus clock cycles; $\overline{\text{INT}}$ and $\overline{\text{SMI}}$ should be held asserted until the exception is taken; $\overline{\text{CKSTP\_IN}}$ must be held asserted until the system has been reset. See the *MPC750 RISC Microprocessor Family User's Manual* for more information.

Figure 9 shows the L2 bus output timing diagrams for the MPC755.

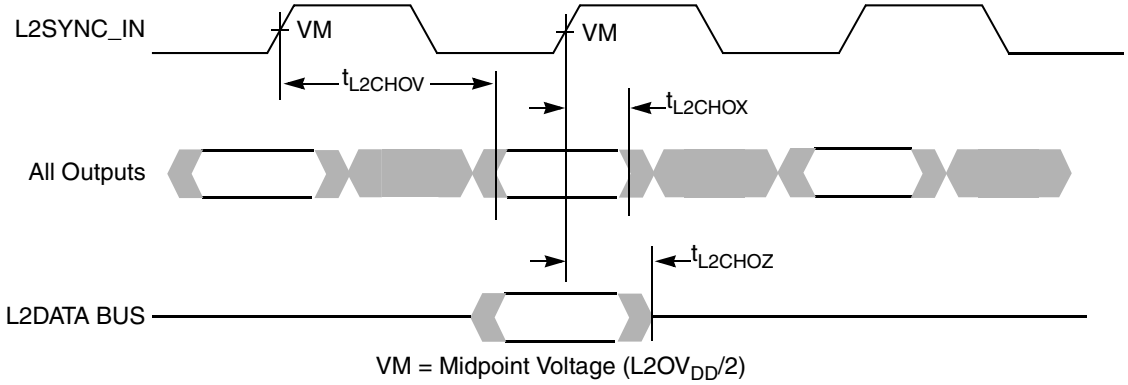


Figure 9. L2 Bus Output Timing Diagrams

Figure 10 provides the AC test load for L2 interface of the MPC755.

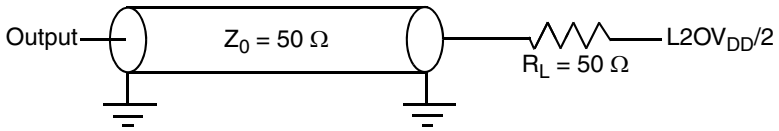


Figure 10. AC Test Load for the L2 Interface

Figure 15 provides the test access port timing diagram.

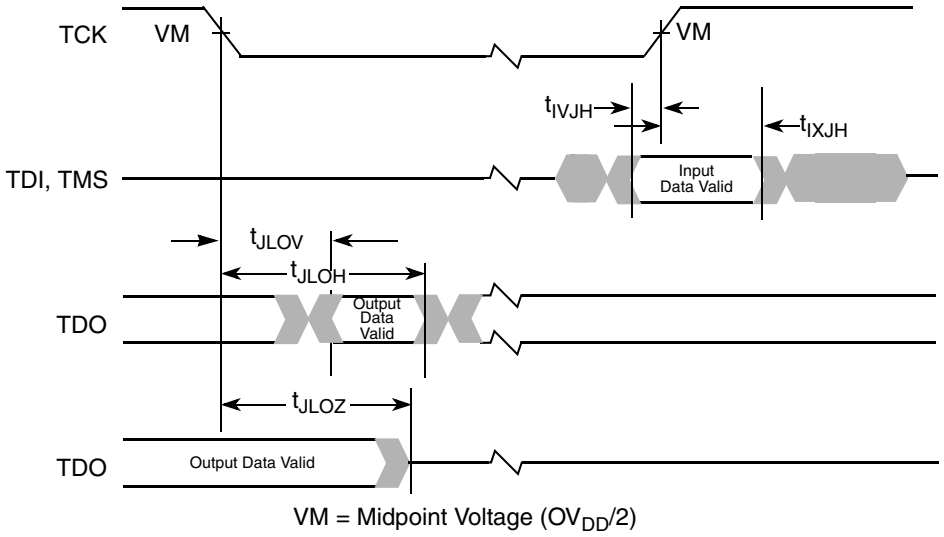


Figure 15. Test Access Port Timing Diagram

6 Pinout Listings

Table 14 provides the pinout listing for the MPC745, 255 PBGA package.

Table 14. Pinout Listing for the MPC745, 255 PBGA Package

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
A[0:31]	C16, E4, D13, F2, D14, G1, D15, E2, D16, D4, E13, G2, E15, H1, E16, H2, F13, J1, F14, J2, F15, H3, F16, F4, G13, K1, G15, K2, H16, M1, J15, P1	High	I/O	OV_{DD}	
$\overline{\text{AACK}}$	L2	Low	Input	OV_{DD}	
$\overline{\text{ABB}}$	K4	Low	I/O	OV_{DD}	
AP[0:3]	C1, B4, B3, B2	High	I/O	OV_{DD}	
$\overline{\text{ARTRY}}$	J4	Low	I/O	OV_{DD}	
AV_{DD}	A10	—	—	2.0 V	
$\overline{\text{BG}}$	L1	Low	Input	OV_{DD}	
$\overline{\text{BR}}$	B6	Low	Output	OV_{DD}	
BVSEL	B1	High	Input	OV_{DD}	3, 4, 5
$\overline{\text{CI}}$	E1	Low	Output	OV_{DD}	
$\overline{\text{CKSTP\_IN}}$	D8	Low	Input	OV_{DD}	
$\overline{\text{CKSTP\_OUT}}$	A6	Low	Output	OV_{DD}	
CLK_OUT	D7	—	Output	OV_{DD}	
$\overline{\text{DBB}}$	J14	Low	I/O	OV_{DD}	
$\overline{\text{DBG}}$	N1	Low	Input	OV_{DD}	
$\overline{\text{DBDIS}}$	H15	Low	Input	OV_{DD}	
$\overline{\text{DBWO}}$	G4	Low	Input	OV_{DD}	
DH[0:31]	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P9, N9, T10, R9, T9, P8, N8, R8, T8, N7, R7, T7, P6, N6, R6, T6, R5, N5, T5, T4	High	I/O	OV_{DD}	
DL[0:31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P3, N3, N4, R3, T1, T2, P4, T3, R4	High	I/O	OV_{DD}	
DP[0:7]	M2, L3, N2, L4, R1, P2, M4, R2	High	I/O	OV_{DD}	
$\overline{\text{DRTRY}}$	G16	Low	Input	OV_{DD}	
$\overline{\text{GBL}}$	F1	Low	I/O	OV_{DD}	
GND	C5, C12, E3, E6, E8, E9, E11, E14, F5, F7, F10, F12, G6, G8, G9, G11, H5, H7, H10, H12, J5, J7, J10, J12, K6, K8, K9, K11, L5, L7, L10, L12, M3, M6, M8, M9, M11, M14, P5, P12	—	—	GND	
$\overline{\text{HRESET}}$	A7	Low	Input	OV_{DD}	

Table 14. Pinout Listing for the MPC745, 255 PBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
$\overline{\text{INT}}$	B15	Low	Input	OV_{DD}	
L1_TSTCLK	D11	High	Input	—	2
L2_TSTCLK	D12	High	Input	—	2
$\overline{\text{LSSD\_MODE}}$	B10	Low	Input	—	2
$\overline{\text{MCP}}$	C13	Low	Input	OV_{DD}	
NC (No Connect)	B7, B8, C3, C6, C8, D5, D6, H4, J16, A4, A5, A2, A3, B5	—	—	—	
OV_{DD}	C7, E5, E7, E10, E12, G3, G5, G12, G14, K3, K5, K12, K14, M5, M7, M10, M12, P7, P10	—	—	2.5 V/3.3 V	
PLL_CFG[0:3]	A8, B9, A9, D9	High	Input	OV_{DD}	
$\overline{\text{QACK}}$	D3	Low	Input	OV_{DD}	
$\overline{\text{QREQ}}$	J3	Low	Output	OV_{DD}	
$\overline{\text{RSRV}}$	D1	Low	Output	OV_{DD}	
$\overline{\text{SMI}}$	A16	Low	Input	OV_{DD}	
$\overline{\text{SRESET}}$	B14	Low	Input	OV_{DD}	
SYSCLK	C9	—	Input	OV_{DD}	
$\overline{\text{TA}}$	H14	Low	Input	OV_{DD}	
TBEN	C2	High	Input	OV_{DD}	
$\overline{\text{TBST}}$	A14	Low	I/O	OV_{DD}	
TCK	C11	High	Input	OV_{DD}	
TDI	A11	High	Input	OV_{DD}	5
TDO	A12	High	Output	OV_{DD}	
$\overline{\text{TEA}}$	H13	Low	Input	OV_{DD}	
$\overline{\text{TLBISYNC}}$	C4	Low	Input	OV_{DD}	
TMS	B11	High	Input	OV_{DD}	5
$\overline{\text{TRST}}$	C10	Low	Input	OV_{DD}	5
$\overline{\text{TS}}$	J13	Low	I/O	OV_{DD}	
TSIZ[0:2]	A13, D10, B12	High	Output	OV_{DD}	
TT[0:4]	B13, A15, B16, C14, C15	High	I/O	OV_{DD}	
$\overline{\text{WT}}$	D2	Low	Output	OV_{DD}	
V_{DD}	F6, F8, F9, F11, G7, G10, H6, H8, H9, H11, J6, J8, J9, J11, K7, K10, L6, L8, L9, L11	—	—	2.0 V	

Table 14. Pinout Listing for the MPC745, 255 PBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
VOLTDET	F3	High	Output	—	6

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals; and V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL pin configuration of Table 2 and the voltage supplied. For actual recommended value of V_{in} or supply voltages, see Table 3.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. This pin must be pulled up to OV_{DD} for proper operation of the processor interface. To allow for future I/O voltage changes, provide the option to connect BVSEL independently to either OV_{DD} or GND.
4. Uses 1 of 15 existing no connects in the MPC740, 255 BGA package.
5. Internal pull-up on die.
6. Internally tied to GND in the MPC745, 255 BGA package to indicate to the power supply that a low-voltage processor is present. This signal is not a power supply input.

   Caution: This differs from the MPC755, 360 BGA package.

Table 15 provides the pinout listing for the MPC755, 360 PBGA and CBGA packages.

Table 15. Pinout Listing for the MPC755, 360 BGA Package

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
A[0:31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O	OV_{DD}	
$\overline{\text{AACK}}$	N3	Low	Input	OV_{DD}	
$\overline{\text{ABB}}$	L7	Low	I/O	OV_{DD}	
AP[0:3]	C4, C5, C6, C7	High	I/O	OV_{DD}	
$\overline{\text{ARTRY}}$	L6	Low	I/O	OV_{DD}	
AV_{DD}	A8	—	—	2.0 V	
$\overline{\text{BG}}$	H1	Low	Input	OV_{DD}	
$\overline{\text{BR}}$	E7	Low	Output	OV_{DD}	
BVSEL	W1	High	Input	OV_{DD}	3, 5, 6
$\overline{\text{CI}}$	C2	Low	Output	OV_{DD}	
$\overline{\text{CKSTP\_IN}}$	B8	Low	Input	OV_{DD}	
$\overline{\text{CKSTP\_OUT}}$	D7	Low	Output	OV_{DD}	
CLK_OUT	E3	—	Output	OV_{DD}	
$\overline{\text{DBB}}$	K5	Low	I/O	OV_{DD}	
$\overline{\text{DBDIS}}$	G1	Low	Input	OV_{DD}	
$\overline{\text{DBG}}$	K1	Low	Input	OV_{DD}	
$\overline{\text{DBWO}}$	D1	Low	Input	OV_{DD}	

Table 15. Pinout Listing for the MPC755, 360 BGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
VOLTDET	K13	High	Output	$L2OV_{DD}$	8

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L2 cache controls ($\overline{L2CE}$, $\overline{L2WE}$, and L2ZZ); $L2OV_{DD}$ supplies power to the L2 cache interface (L2ADDR[0:16], L2DATA[0:63], L2DP[0:7], and L2SYNC_OUT) and the L2 control signals; and V_{DD} supplies power to the processor core and the PLL and DLL (after filtering to become AV_{DD} and $L2AV_{DD}$, respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL/L2VSEL pin configurations of Table 2 and the voltage supplied. For actual recommended value of V_{in} or supply voltages, see Table 3.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. This pin must be pulled up to OV_{DD} for proper operation of the processor interface. To allow for future I/O voltage changes, provide the option to connect BVSEL independently to either OV_{DD} or GND.
4. These pins are reserved for potential future use as additional L2 address pins.
5. Uses one of nine existing no connects in the MPC750, 360 BGA package.
6. Internal pull-up on die.
7. This pin must be pulled up to $L2OV_{DD}$ for proper operation of the processor interface. To allow for future I/O voltage changes, provide the option to connect L2VSEL independently to either $L2OV_{DD}$ or GND.
8. Internally tied to $L2OV_{DD}$ in the MPC755, 360 BGA package to indicate the power present at the L2 cache interface. This signal is not a power supply input.

   Caution: This differs from the MPC745, 255 BGA package.

7 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC745, 255 PBGA package, as well as the MPC755, 360 CBGA and PBGA packages. While both the MPC755 plastic and ceramic packages are described here, both packages are not guaranteed to be available at the same time. All new designs should allow for either ceramic or plastic BGA packages for this device. For more information on designing a common footprint for both plastic and ceramic package types, see the *Freescale Flip-Chip Plastic Ball Grid Array Presentation*. The MPC755 was initially sampled in a CBGA package, but production units are currently provided in both a CBGA and a PBGA package. Because of the better long-term device-to-board interconnect reliability of the PBGA package, Freescale recommends use of a PBGA package except where circumstances dictate use of a CBGA package.

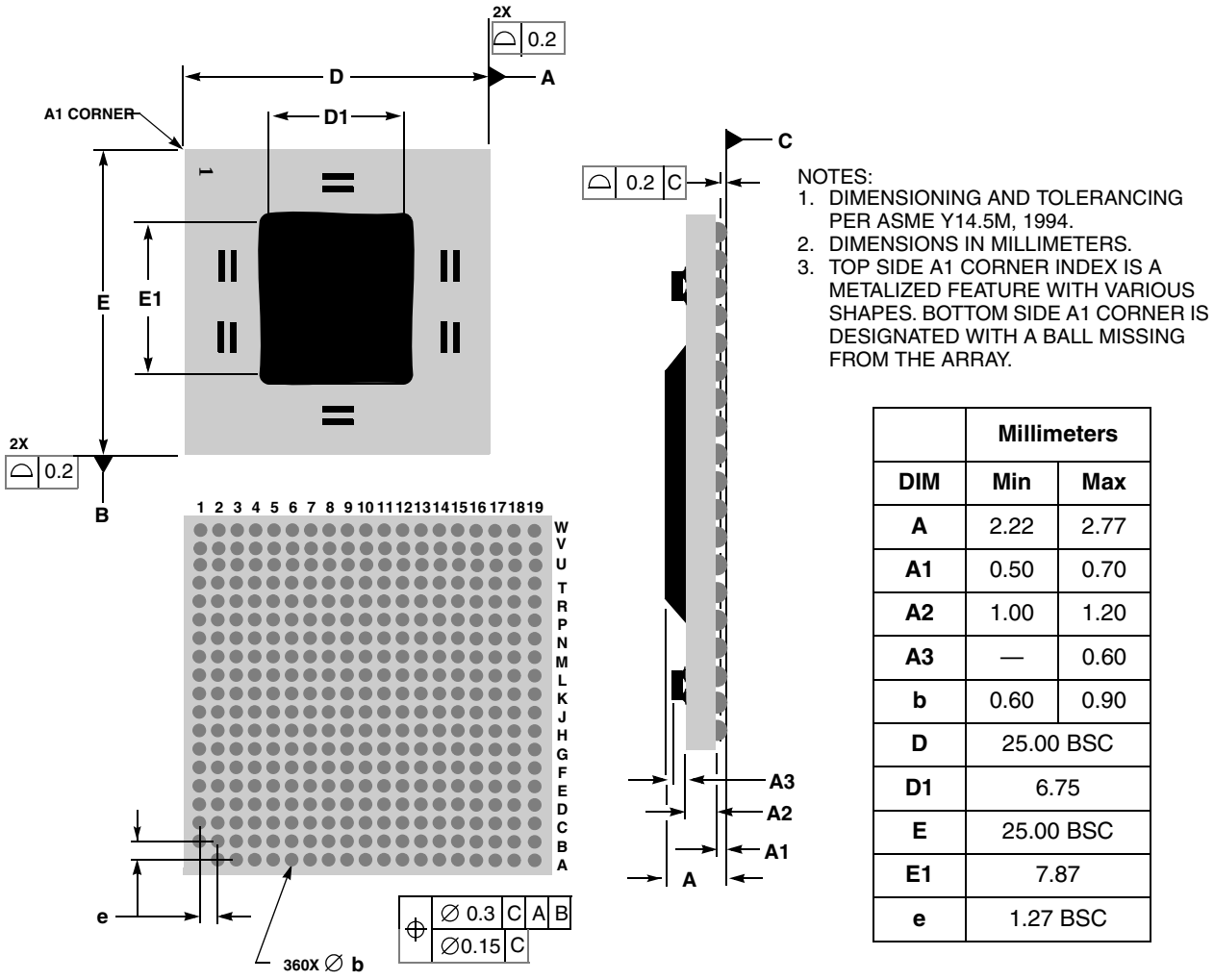
7.5 Package Parameters for the MPC755 PBGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead plastic ball grid array (PBGA).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.22 mm
Maximum module height	2.77 mm
Ball diameter	0.75 mm (29.5 mil)

7.6 Mechanical Dimensions for the MPC755

Figure 20 provides the mechanical dimensions and bottom surface nomenclature for the MPC755, 360 PBGA package.



	Millimeters	
DIM	Min	Max
A	2.22	2.77
A1	0.50	0.70
A2	1.00	1.20
A3	—	0.60
b	0.60	0.90
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	

Figure 20. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC755, 360 PBGA Package

8 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC755.

8.1 PLL Configuration

The MPC755 PLL is configured by the PLL_CFG[0:3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. These must be chosen such that they comply with Table 8. Table 16 shows the valid configurations of these signals and an example illustrating the core and VCO frequencies resulting from various PLL configurations and example bus frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the 400-MHz column in Table 8.

Table 16. MPC755 Microprocessor PLL Configuration Example for 400 MHz Parts

PLL_CFG [0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus 33 MHz	Bus 50 MHz	Bus 66 MHz	Bus 75 MHz	Bus 80 MHz	Bus 100 MHz
0100	2x	2x	—	—	—	—	—	200 (400)
1000	3x	2x	—	—	200 (400)	225 (450)	240 (480)	300 (600)
1110	3.5x	2x	—	—	233 (466)	263 (525)	280 (560)	350 (700)
1010	4x	2x	—	200 (400)	266 (533)	300 (600)	320 (640)	400 (800)
0111	4.5x	2x	—	225 (450)	300 (600)	338 (675)	360 (720)	—
1011	5x	2x	—	250 (500)	333 (666)	375 (750)	400 (800)	—
1001	5.5x	2x	—	275 (550)	366 (733)	—	—	—
1101	6x	2x	200 (400)	300 (600)	400 (800)	—	—	—
0101	6.5x	2x	216 (433)	325 (650)	—	—	—	—
0010	7x	2x	233 (466)	350 (700)	—	—	—	—
0001	7.5x	2x	250 (500)	375 (750)	—	—	—	—
1100	8x	2x	266 (533)	400 (800)	—	—	—	—
0110	10x	2x	333 (666)	—	—	—	—	—

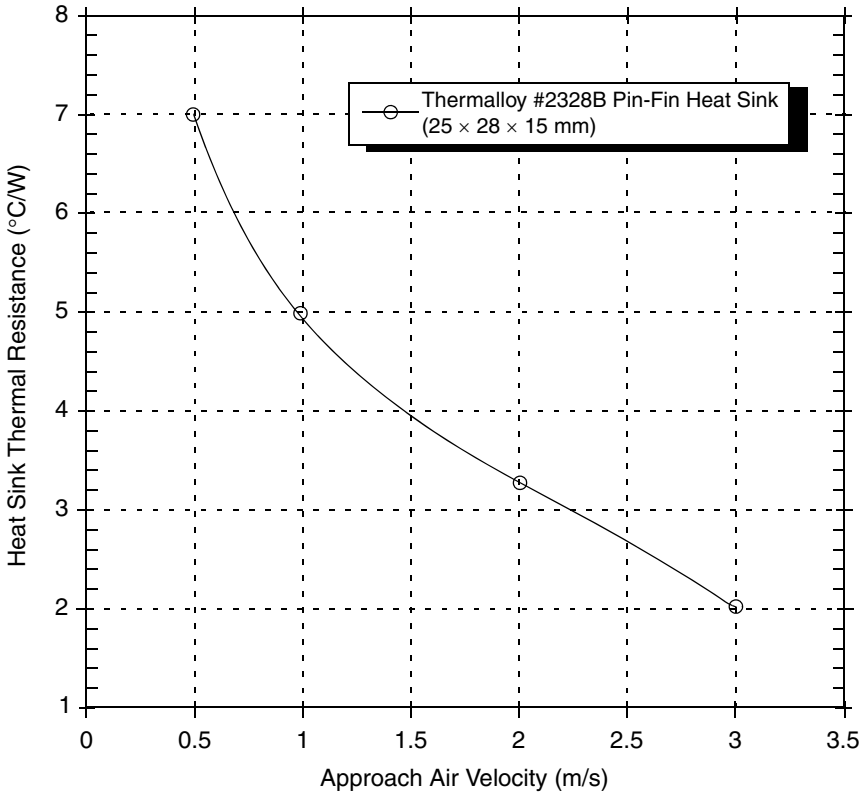


Figure 28. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs.

10 Ordering Information

Ordering information for the devices fully covered by this specification document is provided in Section 10.1, “Part Numbers Fully Addressed by This Document.” Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number. Section 10.2, “Part Numbers Not Fully Addressed by This Document,” lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specifications addendum.

10.1 Part Numbers Fully Addressed by This Document

Table 20 provides the Freescale part numbering nomenclature for the MPC755 and MPC745 devices fully addressed by this document.

Table 20. Part Numbering Nomenclature

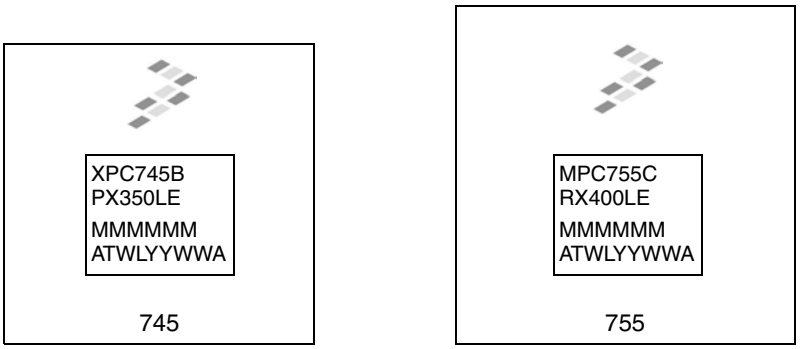
MPC	*xxx*	*x*	*xx*	*nnn*	*x*	*x*
Product Code	**Part Identifier**	**Process Descriptor**	**Package [1]**	**Processor Frequency**	**Application Modifier**	**Revision Level**
XPC[2]	755 745	B = HiP4DP	PX = PBGA RX = CBGA	300 350	L: 2.0 V ± 100 mV 0° to 105°C	E: 2.8; PVR = 0008 3203
	755	C = HiP4DP		400		
MPC	755	B = HiP4DP		300 350		
		C = HiP4DP		350 400		
	745	B = HiP4DP	PX = PBGA	300 350		
	745	C = HiP4DP	PX = PBGA VT = PBGAPb-free BGA	350		
	755 745	B = HiP4DP	VT = PBGAPb-free BGA	300 350		
	755	C = HiP4DP		350 400		

Notes:

1. See Section 7, “Package Description,” for more information on available package types.
2. The X prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These are from a limited production volume of prototypes manufactured, tested, and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes

10.3 Part Marking

Parts are marked as the example shown in Figure 29.



Notes:

MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 29. Part Marking for BGA Device

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