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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 350MHz |
| Co-Processors/DSP | - |
| RAM Controllers | - |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 255-BBGA, FCBGA |
| Supplier Device Package | 255-FCPBGA (21x21) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc745cvt350le |

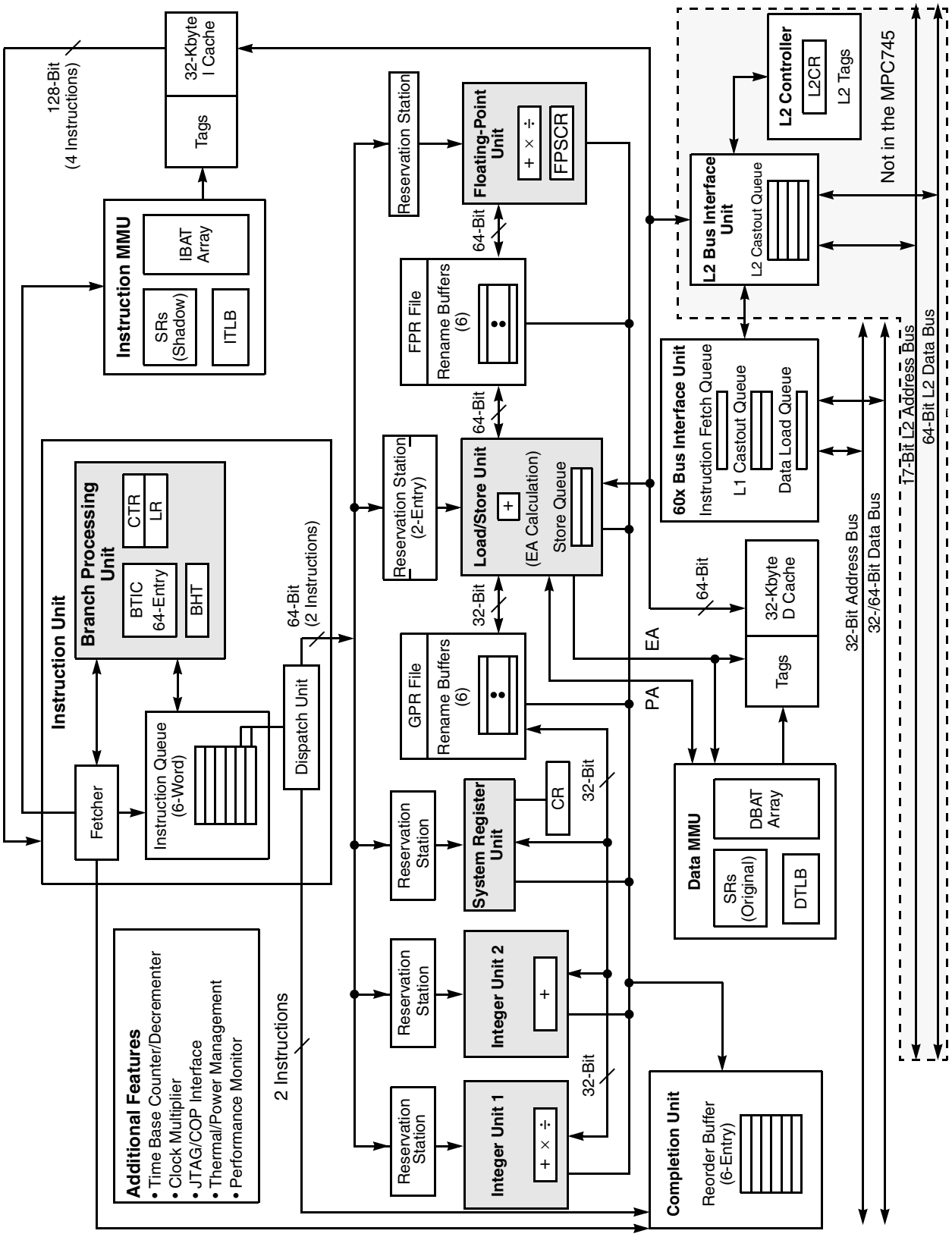



**Figure 1. MPC755 Block Diagram**

| | |
|---|---|
| Packages | MPC745: Surface mount 255 plastic ball grid array (PBGA)<br>MPC755: Surface mount 360 ceramic ball grid array (CBGA)<br>Surface mount 360 plastic ball grid array (PBGA) |
| Core power supply | 2.0 V ± 100 mV DC (nominal; some parts support core voltages down to 1.8 V; see Table 3 for recommended operating conditions) |
| I/O power supply | 2.5 V ± 100 mV DC or<br>3.3 V ± 165 mV DC (input thresholds are configuration pin selectable) |

# 4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC755.

## 4.1 DC Electrical Characteristics

Table 1 through Table 7 describe the MPC755 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

**Table 1. Absolute Maximum Ratings[1]**

| Characteristic | | Symbol | Maximum Value | Unit | Notes |
|---|---|---|---|---|---|
| Core supply voltage | | $V_{DD}$ | –0.3 to 2.5 | V | 4 |
| PLL supply voltage | | $AV_{DD}$ | –0.3 to 2.5 | V | 4 |
| L2 DLL supply voltage | | $L2AV_{DD}$ | –0.3 to 2.5 | V | 4 |
| Processor bus supply voltage | | $OV_{DD}$ | –0.3 to 3.6 | V | 3 |
| L2 bus supply voltage | | $L2OV_{DD}$ | –0.3 to 3.6 | V | 3 |
| Input voltage | Processor bus | $V_{in}$ | –0.3 to $OV_{DD}$ + 0.3 V | V | 2, 5 |
| | L2 bus | $V_{in}$ | –0.3 to $L2OV_{DD}$ + 0.3 V | V | 2, 5 |
| | JTAG signals | $V_{in}$ | –0.3 to 3.6 | V | |
| Storage temperature range | | $T_{stg}$ | –55 to 150 | °C | |

**Notes:**

1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** $V_{in}$ must not exceed $OV_{DD}$ or $L2OV_{DD}$ by more than 0.3 V at any time including during power-on reset.
3. **Caution:** $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 1.6 V during normal operation. During power-on reset and power-down sequences, $L2OV_{DD}/OV_{DD}$ may exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by up to 3.3 V for up to 20 ms, or by 2.5 V for up to 40 ms. Excursions beyond 3.3 V or 40 ms are not supported.
4. **Caution:** $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4 V during normal operation. During power-on reset and power-down sequences, $V_{DD}/AV_{DD}/L2AV_{DD}$ may exceed $L2OV_{DD}/OV_{DD}$ by up to 1.0 V for up to 20 ms, or by 0.7 V for up to 40 ms. Excursions beyond 1.0 V or 40 ms are not supported.
5. This is a DC specifications only. $V_{in}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

Table 3 provides the recommended operating conditions for the MPC755.

**Table 3. Recommended Operating Conditions [1]**

| Characteristic | | Symbol | Recommended Value | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | 300 MHz, 350 MHz | | 400 MHz | | | |
| | | | Min | Max | Min | Max | | |
| Core supply voltage | | $V_{DD}$ | 1.80 | 2.10 | 1.90 | 2.10 | V | 3 |
| PLL supply voltage | | $AV_{DD}$ | 1.80 | 2.10 | 1.90 | 2.10 | V | 3 |
| L2 DLL supply voltage | | $L2AV_{DD}$ | 1.80 | 2.10 | 1.90 | 2.10 | V | 3 |
| Processor bus supply voltage | BVSEL = 1 | $OV_{DD}$ | 2.375 | 2.625 | 2.375 | 2.625 | V | 2, 4 |
| | | | 3.135 | 3.465 | 3.135 | 3.465 | | 5 |
| L2 bus supply voltage | L2VSEL = 1 | $L2OV_{DD}$ | 2.375 | 2.625 | 2.375 | 2.625 | V | 2, 4 |
| | | | 3.135 | 3.465 | 3.135 | 3.465 | | 5 |
| Input voltage | Processor bus | $V_{in}$ | GND | $OV_{DD}$ | GND | $OV_{DD}$ | V | |
| | L2 bus | $V_{in}$ | GND | $L2OV_{DD}$ | GND | $L2OV_{DD}$ | V | |
| | JTAG signals | $V_{in}$ | GND | $OV_{DD}$ | GND | $OV_{DD}$ | V | |
| Die-junction temperature | | $T_j$ | 0 | 105 | 0 | 105 | °C | |

**Notes:**

1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. Revisions prior to Rev. 2.8 (Rev. E) offered different I/O voltage support. For more information, refer to Section 10.2, “Part Numbers Not Fully Addressed by This Document.”
3. 2.0 V nominal.
4. 2.5 V nominal.
5. 3.3 V nominal.

Table 4 provides the package thermal characteristics for the MPC755 and MPC745. The MPC755 was initially sampled in a CBGA package, but production units are currently provided in both a CBGA and a PBGA package. Because of the better long-term device-to-board interconnect reliability of the PBGA package, Freescale recommends use of a PBGA package except where circumstances dictate use of a CBGA package. The MPC745 is offered in a PBGA package only.

**Table 4. Package Thermal Characteristics [6]**

| Characteristic | Symbol | Value | | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | MPC755 CBGA | MPC755 PBGA | MPC745 PBGA | | |
| Junction-to-ambient thermal resistance, natural convection | $R_{\theta JA}$ | 24 | 31 | 34 | °C/W | 1, 2 |
| Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board | $R_{\theta JMA}$ | 17 | 25 | 26 | °C/W | 1, 3 |
| Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board | $R_{\theta JMA}$ | 18 | 25 | 27 | °C/W | 1, 3 |
| Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board | $R_{\theta JMA}$ | 14 | 21 | 22 | °C/W | 1, 3 |
| Junction-to-board thermal resistance | $R_{\theta JB}$ | 8 | 17 | 17 | °C/W | 4 |
| Junction-to-case thermal resistance | $R_{\theta JC}$ | <0.1 | <0.1 | <0.1 | °C/W | 5 |

**Notes:**

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.
6. Refer to Section 8.8, "Thermal Management Information," for more details about thermal management.

The MPC755 incorporates a thermal management assist unit (TAU) composed of a thermal sensor, digital-to-analog converter, comparator, control logic, and dedicated special-purpose registers (SPRs). See the *MPC750 RISC Microprocessor Family User's Manual* for more information on the use of this feature. Specifications for the thermal sensor portion of the TAU are found in Table 5.

**Table 6. DC Electrical Specifications (continued)**

At recommended operating conditions (see Table 3)

| Characteristic | Nominal Bus Voltage [1] | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Capacitance, $V_{in}$ = 0 V, f = 1 MHz | | $C_{in}$ | — | 5.0 | pF | 3, 4 |

**Notes:**

1. Nominal voltages; see Table 3 for recommended operating conditions.
2. For processor bus signals, the reference is $OV_{DD}$ while $L2OV_{DD}$ is the reference for the L2 bus signals.
3. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK) and IEEE 1149.1 boundary scan (JTAG) signals.
4. Capacitance is periodically sampled rather than 100% tested.
5. The leakage is measured for nominal $OV_{DD}$ and $V_{DD}$, or both $OV_{DD}$ and $V_{DD}$ must vary in the same direction (for example, both $OV_{DD}$ and $V_{DD}$ vary by either +5% or –5%).

Table 7 provides the power consumption for the MPC755.

**Table 7. Power Consumption for MPC755**

| | Processor (CPU) Frequency | | | Unit | Notes |
|---|---|---|---|---|---|
| | 300 MHz | 350 MHz | 400 MHz | | |
| **Full-Power Mode** | | | | | |
| Typical | 3.1 | 3.6 | 5.4 | W | 1, 3, 4 |
| Maximum | 4.5 | 6.0 | 8.0 | W | 1, 2 |
| **Doze Mode** | | | | | |
| Maximum | 1.8 | 2.0 | 2.3 | W | 1, 2, 4 |
| **Nap Mode** | | | | | |
| Maximum | 1.0 | 1.0 | 1.0 | W | 1, 2, 4 |
| **Sleep Mode** | | | | | |
| Maximum | 550 | 550 | 550 | mW | 1, 2, 4 |
| **Sleep Mode (PLL and DLL Disabled)** | | | | | |
| Maximum | 510 | 510 | 510 | mW | 1, 2 |

**Notes:**

1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O supply power ($OV_{DD}$ and $L2OV_{DD}$) or PLL/DLL supply power ($AV_{DD}$ and $L2AV_{DD}$). $OV_{DD}$ and $L2OV_{DD}$ power is system dependent, but is typically <10% of $V_{DD}$ power. Worst case power consumption for $AV_{DD}$ = 15 mW and $L2AV_{DD}$ = 15 mW.
2. Maximum power is measured at nominal $V_{DD}$ (see Table 3) while running an entirely cache-resident, contrived sequence of instructions which keep the execution units maximally busy.
3. Typical power is an average value measured at the nominal recommended $V_{DD}$ (see Table 3) and 65°C in a system while running a typical code sequence.
4. Not 100% tested. Characterized and periodically sampled.

## 4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC755. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section 4.2.1, "Clock AC Specifications," and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:3] signals. Parts are sold by maximum processor core frequency; see Section 10, "Ordering Information."

### 4.2.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications as defined in Figure 3.

**Table 8. Clock AC Timing Specifications**

At recommended operating conditions (see Table 3)

| Characteristic | Symbol | Maximum Processor Core Frequency | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | 300 MHz | | 350 MHz | | 400 MHz | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| Processor frequency | $f_{core}$ | 200 | 300 | 200 | 350 | 200 | 400 | MHz | 1 |
| VCO frequency | $f_{VCO}$ | 400 | 600 | 400 | 700 | 400 | 800 | MHz | 1 |
| SYSCLK frequency | $f_{SYSCLK}$ | 25 | 100 | 25 | 100 | 25 | 100 | MHz | 1 |
| SYSCLK cycle time | $t_{SYSCLK}$ | 10 | 40 | 10 | 40 | 10 | 40 | ns | |
| SYSCLK rise and fall time | $t_{KR}$, $t_{KF}$ | — | 2.0 | — | 2.0 | — | 2.0 | ns | 2 |
| | $t_{KR}$, $t_{KF}$ | — | 1.4 | — | 1.4 | — | 1.4 | ns | 2 |
| SYSCLK duty cycle measured at $OV_{DD}/2$ | $t_{KHKL}/t_{SYSCLK}$ | 40 | 60 | 40 | 60 | 40 | 60 | % | 3 |
| SYSCLK jitter | | — | ±150 | — | ±150 | — | ±150 | ps | 3, 4 |
| Internal PLL relock time | | — | 100 | — | 100 | — | 100 | μs | 3, 5 |

**Notes:**

1. **Caution:** The SYSCLK frequency and PLL_CFG[0:3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:3] signal description in Section 8.1, "PLL Configuration," for valid PLL_CFG[0:3] settings.
2. Rise and fall times measurements are now specified in terms of slew rates, rather than time to account for selectable I/O bus interface levels. The minimum slew rate of 1 V/ns is equivalent to a 2 ns maximum rise/fall time measured at 0.4 and 2.4 V ($OV_{DD}$ = 3.3 V) or a rise/fall time of 1 ns measured at 0.4 and 1.8 V ($OV_{DD}$ = 2.5 V).
3. Timing is guaranteed by design and characterization.
4. This represents total input jitter—short term and long term combined—and is guaranteed by design.
5. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable $V_{DD}$ and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 3 provides the SYSCLK input timing diagram.

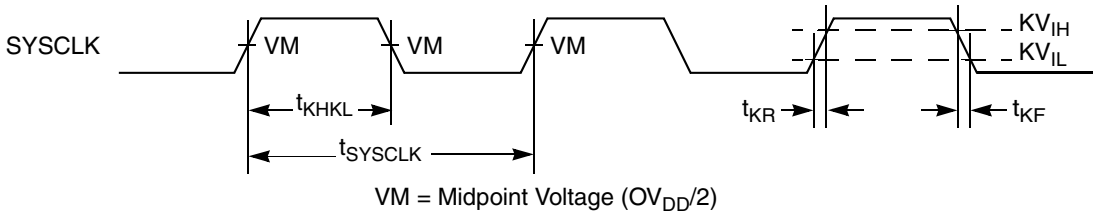



**Figure 3. SYSCLK Input Timing Diagram**

## 4.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC755 as defined in Figure 4 and Figure 6. Timing specifications for the L2 bus are provided in Section 4.2.3, "L2 Clock AC Specifications."

**Table 9. Processor Bus Mode Selection AC Timing Specifications [1]**

At recommended operating conditions (see Table 3)

| Parameter | Symbol [2] | All Speed Grades | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Mode select input setup to $\overline{\text{HRESET}}$ | $t_{MVRH}$ | 8 | — | $t_{sysclk}$ | 3, 4, 5, 6, 7 |
| $\overline{\text{HRESET}}$ to mode select input hold | $t_{MXRH}$ | 0 | — | ns | 3, 4, 6, 7, 8 |

**Notes:**

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 5). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{IVKH}$ symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And $t_{KHOV}$ symbolizes the time from SYSCLK (K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH)—note the position of the reference and its state for inputs—and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 4).
4. This specification is for configuration mode select only. Also note that the $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
5. $t_{sysclk}$ is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
6. Mode select signals are BVSEL, L2VSEL, PLL_CFG[0:3], and $\overline{\text{TLBISYNC}}$.
7. Guaranteed by design and characterization.
8. Bus mode select pins must remain stable during operation. Changing the logic states of BVSEL or L2VSEL during operation will cause the bus mode voltage selection to change. Changing the logic states of the PLL_CFG pins during operation will cause the PLL division ratio selection to change. Both of these conditions are considered outside the specification and are not supported. Once $\overline{\text{HRESET}}$ is negated the states of the bus mode selection pins must remain stable.

## Table 10. Processor Bus AC Timing Specifications [1]

At recommended operating conditions (see Table 3)

| Parameter | Symbol | All Speed Grades | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Setup times: All inputs | $t_{IVKH}$ | 2.5 | — | ns | |
| Input hold times: $\overline{\text{TLBISYNC}}$, $\overline{\text{MCP}}$, $\overline{\text{SMI}}$ | $t_{IXKH}$ | 0.6 | — | ns | 6 |
| Input hold times: All inputs, except $\overline{\text{TLBISYNC}}$, $\overline{\text{MCP}}$, $\overline{\text{SMI}}$ | $t_{IXKH}$ | 0.2 | — | ns | 6 |
| Valid times: All outputs | $t_{KHOV}$ | — | 4.1 | ns | |
| Output hold times: All outputs | $t_{KHOX}$ | 1.0 | — | ns | |
| SYSCLK to output enable | $t_{KHOE}$ | 0.5 | — | ns | 2 |
| SYSCLK to output high impedance (all except $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$) | $t_{KHOZ}$ | — | 6.0 | ns | 2 |
| SYSCLK to $\overline{\text{ABB}}$, $\overline{\text{DBB}}$ high impedance after precharge | $t_{KHABPZ}$ | — | 1.0 | $t_{sysclk}$ | 2, 3, 4 |
| Maximum delay to $\overline{\text{ARTRY}}$ precharge | $t_{KHARP}$ | — | 1 | $t_{sysclk}$ | 2, 3, 5 |
| SYSCLK to $\overline{\text{ARTRY}}$ high impedance after precharge | $t_{KHARPZ}$ | — | 2 | $t_{sysclk}$ | 2, 3, 5 |

**Notes:**

1. Revisions prior to Rev. 2.8 (Rev. E) were limited in performance and did not conform to this specification. For more information, refer to Section 10.2, "Part Numbers Not Fully Addressed by This Document."
2. Guaranteed by design and characterization.
3. $t_{sysclk}$ is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. Per the 60x bus protocol, $\overline{\text{TS}}$, $\overline{\text{ABB}}$, and $\overline{\text{DBB}}$ are driven only by the currently active bus master. They are asserted low, then precharged high before returning to high-Z as shown in Figure 6. The nominal precharge width for $\overline{\text{TS}}$, $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ is $0.5 \times t_{sysclk}$, that is, less than the minimum $t_{sysclk}$ period, to ensure that another master asserting $\overline{\text{TS}}$, $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
5. Per the 60x bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue since any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 $t_{sysclk}$; that is, it should be high-Z as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z and precharge behavior is guaranteed by design.
6. $\overline{\text{MCP}}$ and $\overline{\text{SRESET}}$ must be held asserted for a minimum of two bus clock cycles; $\overline{\text{INT}}$ and $\overline{\text{SMI}}$ should be held asserted until the exception is taken; $\overline{\text{CKSTP\_IN}}$ must be held asserted until the system has been reset. See the *MPC750 RISC Microprocessor Family User's Manual* for more information.

SRAM. Note that revisions of the MPC755 prior to Rev. 2.8 (Rev. E) were limited in performance, and were typically limited to 175 MHz with similarly-rated SRAM. For more information, see Section 10.2, “Part Numbers Not Fully Addressed by This Document.”

Freescale is similarly limited by system constraints and cannot perform tests of the L2 interface on a socketed part on a functional tester at the maximum frequencies of Table 11. Therefore, functional operation and AC timing information are tested at core-to-L2 divisors of 2 or greater. Functionality of core-to-L2 divisors of 1 or 1.5 is verified at less than maximum rated frequencies.

L2 input and output signals are latched or enabled, respectively, by the internal L2CLK (which is SYSCLK multiplied up to the core frequency and divided down to the L2CLK frequency). In other words, the AC timings of Table 12 and Table 13 are entirely independent of L2SYNC_IN. In a closed loop system, where L2SYNC_IN is driven through the board trace by L2SYNC_OUT, L2SYNC_IN only controls the output phase of L2CLK_OUTA and L2CLK_OUTB which are used to latch or enable data at the SRAMs. However, since in a closed loop system L2SYNC_IN is held in phase alignment with the internal L2CLK, the signals of Table 12 and Table 13 are referenced to this signal rather than the not-externally-visible internal L2CLK. During manufacturing test, these times are actually measured relative to SYSCLK.

The L2SYNC_OUT signal is intended to be routed halfway out to the SRAMs and then returned to the L2SYNC_IN input of the MPC755 to synchronize L2CLK_OUT at the SRAM with the processor’s internal clock. L2CLK_OUT at the SRAM can be offset forward or backward in time by shortening or lengthening the routing of L2SYNC_OUT to L2SYNC_IN. See Freescale Application Note AN1794/D, *Backside L2 Timing Analysis for PCB Design Engineers*.

The L2CLK_OUTA and L2CLK_OUTB signals should not have more than two loads.

**Table 12. L2 Bus Interface AC Timing Specifications (continued)**

At recommended operating conditions (see Table 3)

| Parameter | Symbol | All Speed Grades | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| L2SYNC_IN to high impedance:<br>All outputs when L2CR[14–15] = 00<br>All outputs when L2CR[14–15] = 01<br>All outputs when L2CR[14–15] = 10<br>All outputs when L2CR[14–15] = 11 | $t_{L2CHOZ}$ | <br>—<br>—<br>—<br>— | <br>2.4<br>2.6<br>2.8<br>3.0 | ns | 3, 5 |

**Notes:**

1. Rise and fall times for the L2SYNC_IN input are measured from 20% to 80% of $L2OV_{DD}$.
2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC_IN (see Figure 8). Input timings are measured at the pins.
3. All output specifications are measured from the midpoint voltage of the rising edge of L2SYNC_IN to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 10).
4. The outputs are valid for both single-ended and differential L2CLK modes. For pipelined registered synchronous BurstRAMs, L2CR[14–15] = 01 or 10 is recommended. For pipelined late write synchronous BurstRAMs, L2CR[14–15] = 11 is recommended.
5. Guaranteed by design and characterization.
6. Revisions prior to Rev. 2.8 (Rev. E) were limited in performance and did not conform to this specification. For more information, refer to Section 10.2, “Part Numbers Not Fully Addressed by This Document.”

Figure 8 shows the L2 bus input timing diagrams for the MPC755.

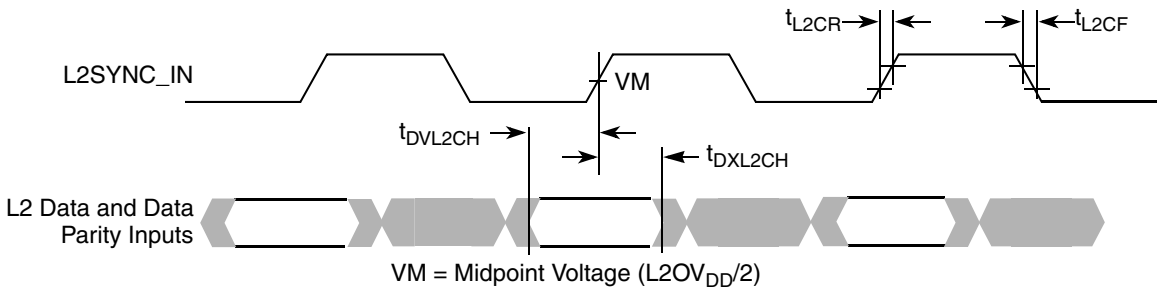



**Figure 8. L2 Bus Input Timing Diagrams**

Figure 9 shows the L2 bus output timing diagrams for the MPC755.

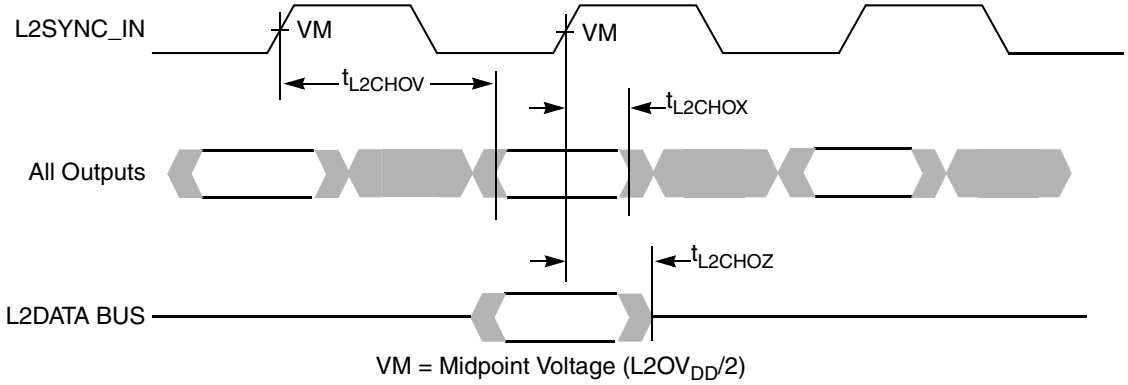



**Figure 9. L2 Bus Output Timing Diagrams**

Figure 10 provides the AC test load for L2 interface of the MPC755.

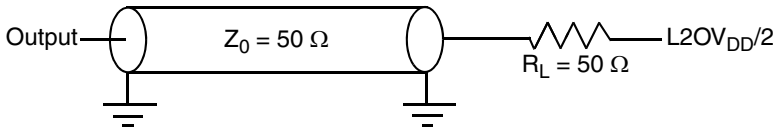



**Figure 10. AC Test Load for the L2 Interface**

Figure 12 provides the JTAG clock input timing diagram.

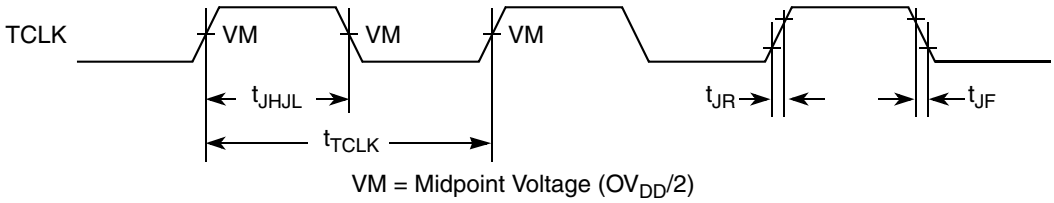



**Figure 12. JTAG Clock Input Timing Diagram**

Figure 13 provides the $\overline{\text{TRST}}$ timing diagram.

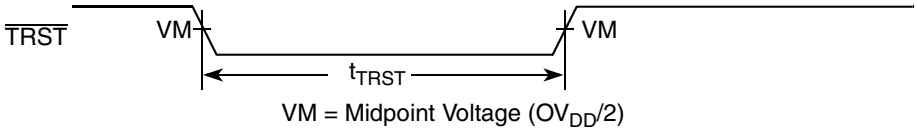



**Figure 13. $\overline{\text{TRST}}$ Timing Diagram**

Figure 14 provides the boundary-scan timing diagram.

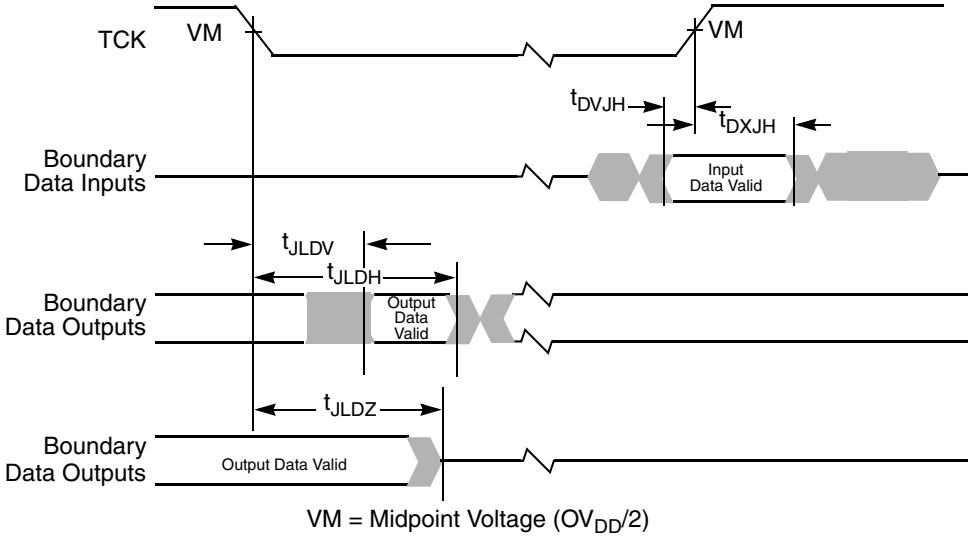
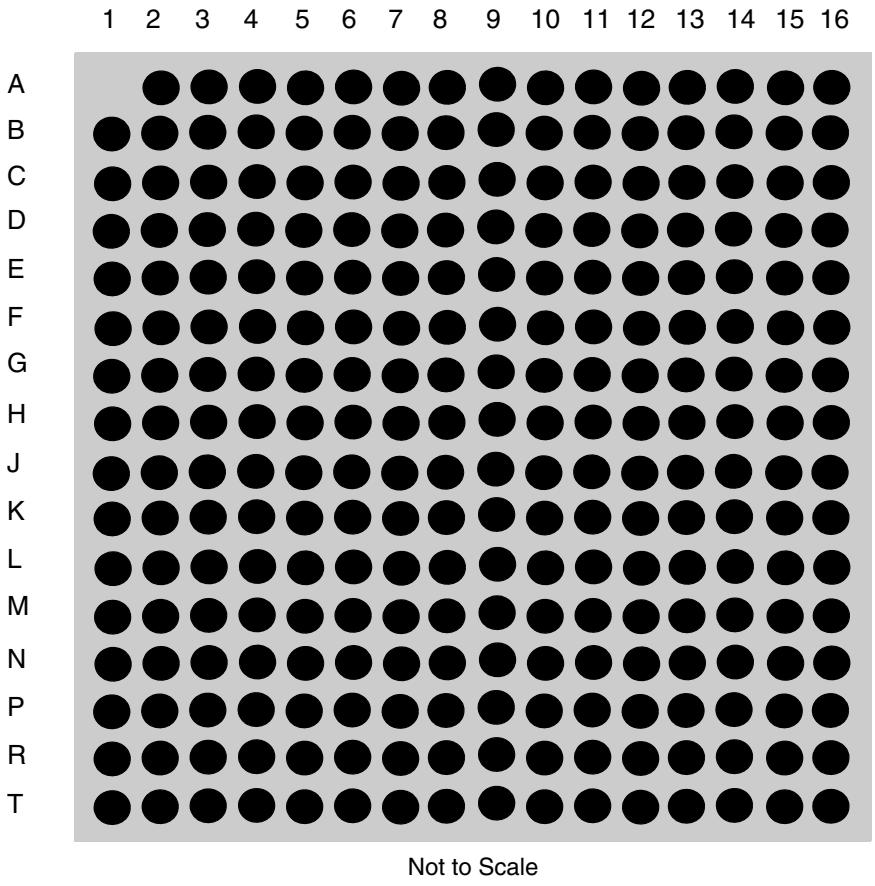



**Figure 14. Boundary-Scan Timing Diagram**

# 5 Pin Assignments

Figure 16 (in Part A) shows the pinout of the MPC745, 255 PBGA package as viewed from the top surface. Part B shows the side profile of the PBGA package to indicate the direction of the top surface view.

**Part A**




**Part B**

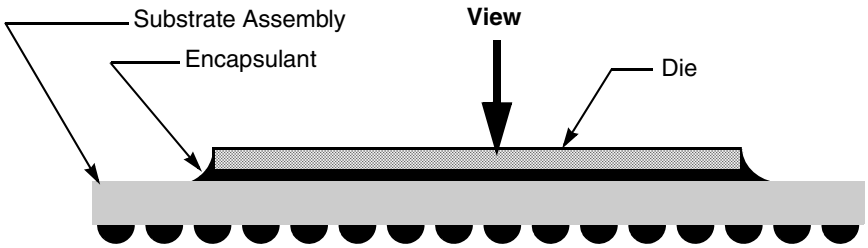



**Figure 16. Pinout of the MPC745, 255 PBGA Package as Viewed from the Top Surface**

**Table 14. Pinout Listing for the MPC745, 255 PBGA Package (continued)**

| Signal Name | Pin Number | Active | I/O | I/F Voltage [1] | Notes |
|---|---|---|---|---|---|
| $\overline{\text{INT}}$ | B15 | Low | Input | $OV_{DD}$ | |
| L1_TSTCLK | D11 | High | Input | — | 2 |
| L2_TSTCLK | D12 | High | Input | — | 2 |
| $\overline{\text{LSSD\_MODE}}$ | B10 | Low | Input | — | 2 |
| $\overline{\text{MCP}}$ | C13 | Low | Input | $OV_{DD}$ | |
| NC (No Connect) | B7, B8, C3, C6, C8, D5, D6, H4, J16, A4, A5, A2, A3, B5 | — | — | — | |
| $OV_{DD}$ | C7, E5, E7, E10, E12, G3, G5, G12, G14, K3, K5, K12, K14, M5, M7, M10, M12, P7, P10 | — | — | 2.5 V/3.3 V | |
| PLL_CFG[0:3] | A8, B9, A9, D9 | High | Input | $OV_{DD}$ | |
| $\overline{\text{QACK}}$ | D3 | Low | Input | $OV_{DD}$ | |
| $\overline{\text{QREQ}}$ | J3 | Low | Output | $OV_{DD}$ | |
| $\overline{\text{RSRV}}$ | D1 | Low | Output | $OV_{DD}$ | |
| $\overline{\text{SMI}}$ | A16 | Low | Input | $OV_{DD}$ | |
| $\overline{\text{SRESET}}$ | B14 | Low | Input | $OV_{DD}$ | |
| SYSCLK | C9 | — | Input | $OV_{DD}$ | |
| $\overline{\text{TA}}$ | H14 | Low | Input | $OV_{DD}$ | |
| TBEN | C2 | High | Input | $OV_{DD}$ | |
| $\overline{\text{TBST}}$ | A14 | Low | I/O | $OV_{DD}$ | |
| TCK | C11 | High | Input | $OV_{DD}$ | |
| TDI | A11 | High | Input | $OV_{DD}$ | 5 |
| TDO | A12 | High | Output | $OV_{DD}$ | |
| $\overline{\text{TEA}}$ | H13 | Low | Input | $OV_{DD}$ | |
| $\overline{\text{TLBISYNC}}$ | C4 | Low | Input | $OV_{DD}$ | |
| TMS | B11 | High | Input | $OV_{DD}$ | 5 |
| $\overline{\text{TRST}}$ | C10 | Low | Input | $OV_{DD}$ | 5 |
| $\overline{\text{TS}}$ | J13 | Low | I/O | $OV_{DD}$ | |
| TSIZ[0:2] | A13, D10, B12 | High | Output | $OV_{DD}$ | |
| TT[0:4] | B13, A15, B16, C14, C15 | High | I/O | $OV_{DD}$ | |
| $\overline{\text{WT}}$ | D2 | Low | Output | $OV_{DD}$ | |
| $V_{DD}$ | F6, F8, F9, F11, G7, G10, H6, H8, H9, H11, J6, J8, J9, J11, K7, K10, L6, L8, L9, L11 | — | — | 2.0 V | |

**Table 15. Pinout Listing for the MPC755, 360 BGA Package (continued)**

| Signal Name | Pin Number | Active | I/O | I/F Voltage [1] | Notes |
|---|---|---|---|---|---|
| DH[0:31] | W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5 | High | I/O | $OV_{DD}$ | |
| DL[0:31] | M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2 | High | I/O | $OV_{DD}$ | |
| DP[0:7] | L1, P2, M2, V2, M1, N2, T3, R1 | High | I/O | $OV_{DD}$ | |
| $\overline{\text{DRTRY}}$ | H6 | Low | Input | $OV_{DD}$ | |
| $\overline{\text{GBL}}$ | B1 | Low | I/O | $OV_{DD}$ | |
| GND | D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16 | — | — | GND | |
| $\overline{\text{HRESET}}$ | B6 | Low | Input | $OV_{DD}$ | |
| $\overline{\text{INT}}$ | C11 | Low | Input | $OV_{DD}$ | |
| L1_TSTCLK | F8 | High | Input | — | 2 |
| L2ADDR[16:0] | G18, H19, J13, J14, H17, H18, J16, J17, J18, J19, K15, K17, K18, M19, L19, L18, L17 | High | Output | $L2OV_{DD}$ | |
| $L2AV_{DD}$ | L13 | — | — | 2.0 V | |
| $\overline{\text{L2CE}}$ | P17 | Low | Output | $L2OV_{DD}$ | |
| L2CLK_OUTA | N15 | — | Output | $L2OV_{DD}$ | |
| L2CLK_OUTB | L16 | — | Output | $L2OV_{DD}$ | |
| L2DATA[0:63] | U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13 | High | I/O | $L2OV_{DD}$ | |
| L2DP[0:7] | V14, U16, T19, N18, H14, F17, C19, B15 | High | I/O | $L2OV_{DD}$ | |
| $L2OV_{DD}$ | D15, E14, E16, H16, J15, L15, M16, P15, R14, R16, T15, F15 | — | — | $L2OV_{DD}$ | |
| L2SYNC_IN | L14 | — | Input | $L2OV_{DD}$ | |
| L2SYNC_OUT | M14 | — | Output | $L2OV_{DD}$ | |
| L2_TSTCLK | F7 | High | Input | — | 2 |
| L2VSEL | A19 | High | Input | $L2OV_{DD}$ | 1, 5, 6, 7 |
| $\overline{\text{L2WE}}$ | N16 | Low | Output | $L2OV_{DD}$ | |

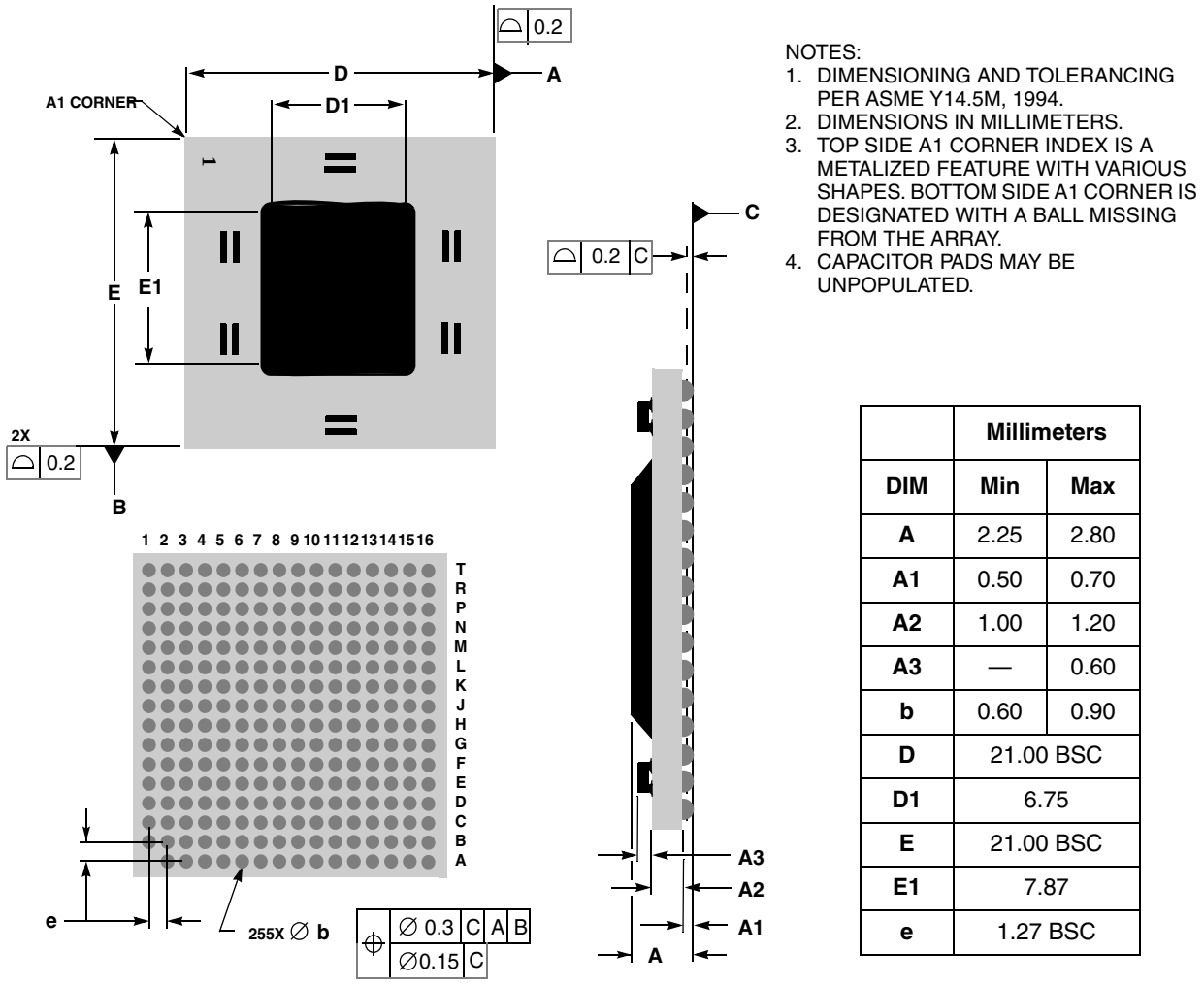
## 7.1 Package Parameters for the MPC745 PBGA

The package parameters are as provided in the following list. The package type is 21 × 21 mm, 255-lead plastic ball grid array (PBGA).

| | |
|---|---|
| Package outline | 21 × 21 mm |
| Interconnects | 255 (16 × 16 ball array – 1) |
| Pitch | 1.27 mm (50 mil) |
| Minimum module height | 2.25 mm |
| Maximum module height | 2.80 mm |
| Ball diameter (typical) | 0.75 mm (29.5 mil) |

## 7.2 Mechanical Dimensions for the MPC745 PBGA

Figure 18 provides the mechanical dimensions and bottom surface nomenclature for the MPC745, 255 PBGA package.




| | Millimeters | |
|---|---|---|
| DIM | Min | Max |
| A | 2.25 | 2.80 |
| A1 | 0.50 | 0.70 |
| A2 | 1.00 | 1.20 |
| A3 | — | 0.60 |
| b | 0.60 | 0.90 |
| D | 21.00 BSC | |
| D1 | 6.75 | |
| E | 21.00 BSC | |
| E1 | 7.87 | |
| e | 1.27 BSC | |

**Figure 18. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC745, 255 PBGA Package**

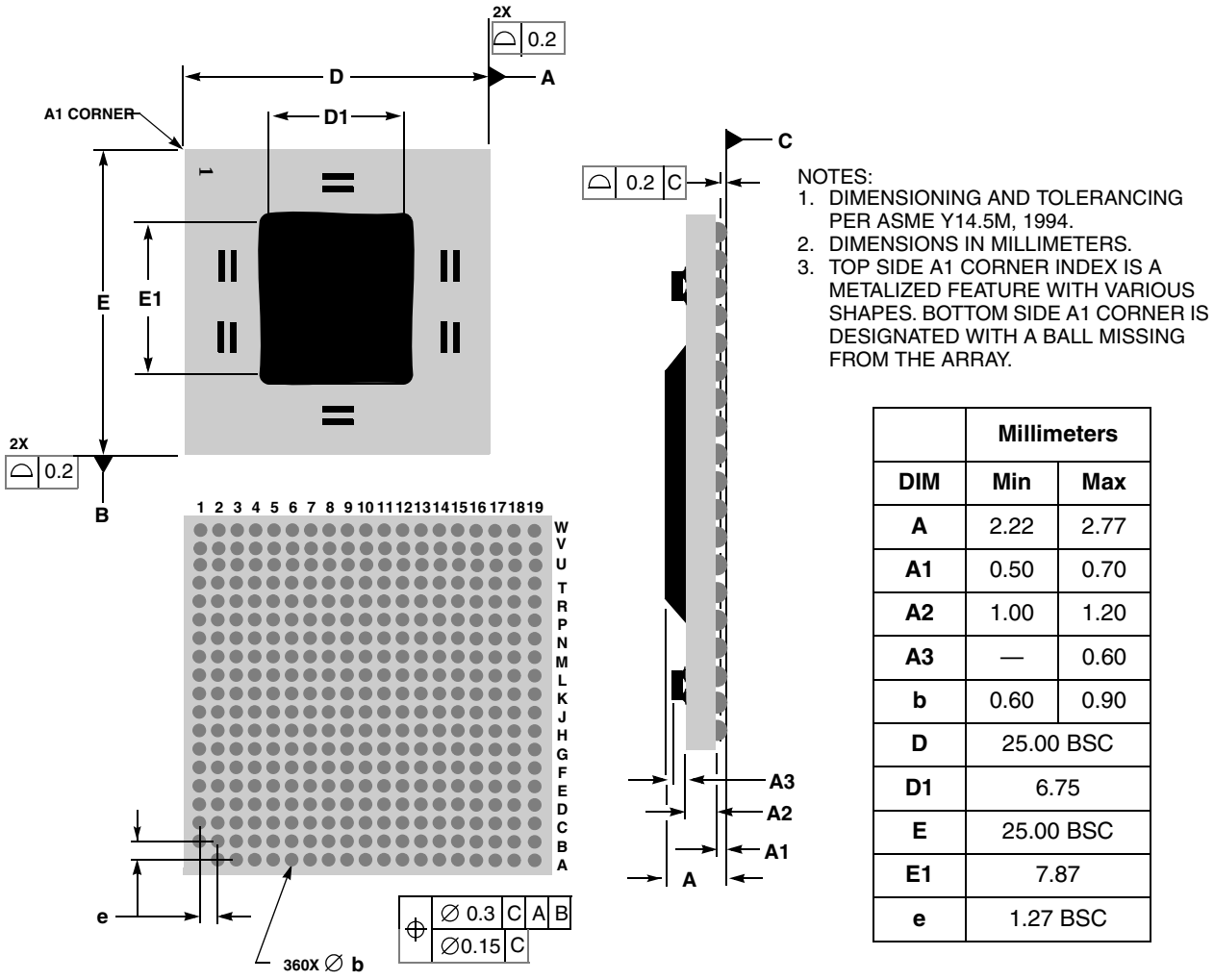
## 7.5 Package Parameters for the MPC755 PBGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead plastic ball grid array (PBGA).

| | |
|---|---|
| Package outline | 25 × 25 mm |
| Interconnects | 360 (19 × 19 ball array – 1) |
| Pitch | 1.27 mm (50 mil) |
| Minimum module height | 2.22 mm |
| Maximum module height | 2.77 mm |
| Ball diameter | 0.75 mm (29.5 mil) |

## 7.6 Mechanical Dimensions for the MPC755

Figure 20 provides the mechanical dimensions and bottom surface nomenclature for the MPC755, 360 PBGA package.




| | Millimeters | |
|---|---|---|
| DIM | Min | Max |
| A | 2.22 | 2.77 |
| A1 | 0.50 | 0.70 |
| A2 | 1.00 | 1.20 |
| A3 | — | 0.60 |
| b | 0.60 | 0.90 |
| D | 25.00 BSC | |
| D1 | 6.75 | |
| E | 25.00 BSC | |
| E1 | 7.87 | |
| e | 1.27 BSC | |

**Figure 20. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC755, 360 PBGA Package**

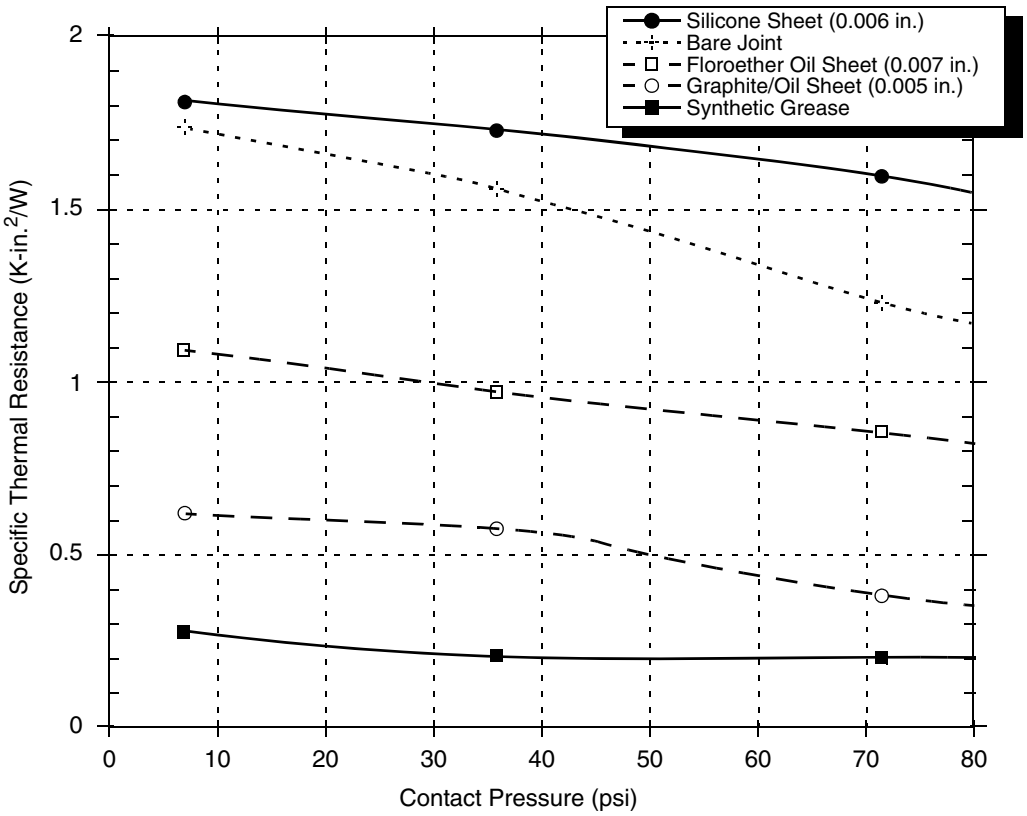



**Figure 27. Thermal Performance of Select Thermal Interface Materials**

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company — 800-347-4572
18930 West 78th St.
Chanhassen, MN 55317
Internet: www.bergquistcompany.com

Chomerics, Inc. — 781-935-4850
77 Dragon Ct.
Woburn, MA 01888-4014
Internet: www.chomerics.com

Dow-Corning Corporation — 800-248-2481
Dow-Corning Electronic Materials
2200 W. Salzburg Rd.
Midland, MI 48686-0997
Internet: www.dow.com

Shin-Etsu MicroSi, Inc. 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

### 8.8.3 Heat Sink Selection Example

This section provides a heat sink selection example using one of the commercially-available heat sinks. For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) \times P_d$$

where:

$T_j$ is the die-junction temperature
$T_a$ is the inlet cabinet ambient temperature
$T_r$ is the air temperature rise within the computer cabinet
$\theta_{jc}$ is the junction-to-case thermal resistance
$\theta_{int}$ is the adhesive or interface material thermal resistance
$\theta_{sa}$ is the heat sink base-to-ambient thermal resistance
$P_d$ is the power dissipated by the device

During operation the die-junction temperatures ($T_j$) should be maintained less than the value specified in Table 3. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature ($T_a$) may range from 30° to 40°C. The air temperature rise within a cabinet ($T_r$) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($\theta_{int}$) is typically about 1°C/W. Assuming a $T_a$ of 30°C, a $T_r$ of 5°C, a CBGA package $R_{\theta jc} < 0.1$, and a power consumption ($P_d$) of 5.0 W, the following expression for $T_j$ is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 1.0°C/W + \theta_{sa}) \times 5.0\ W$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance ($\theta_{sa}$) versus airflow velocity is shown in Figure 28.

Assuming an air velocity of 0.5 m/s, we have an effective $R_{sa}$ of 7°C/W, thus

$$T_j = 30°C + 5°C + (0.1°C/W + 1.0°C/W + 7°C/W) \times 5.0\ W,$$

resulting in a die-junction temperature of approximately 76°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, The Bergquist Company, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.

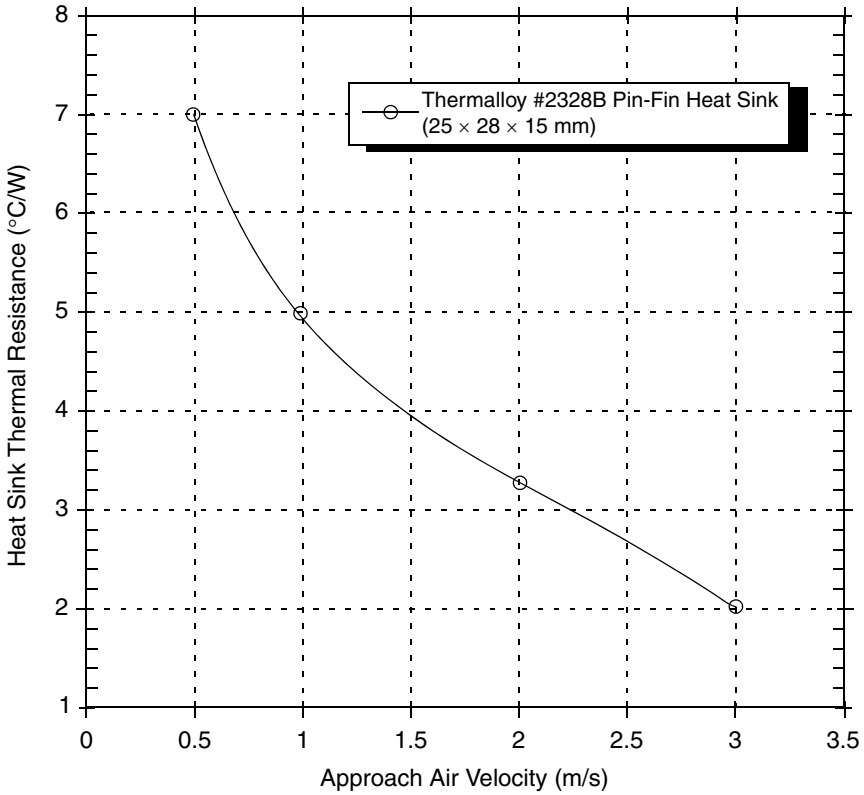



**Figure 28. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity**

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs.