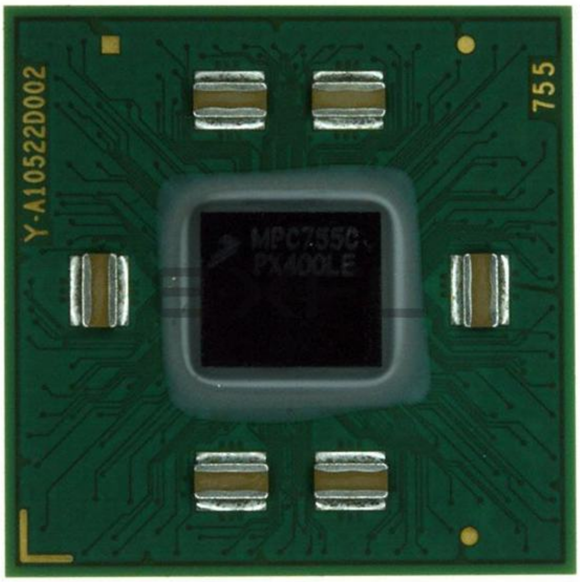

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Details	
Product Status	Obsolete
Core Processor	PowerPC
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	350MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BBGA, FCBGA
Supplier Device Package	360-FCPBGA (25x25)
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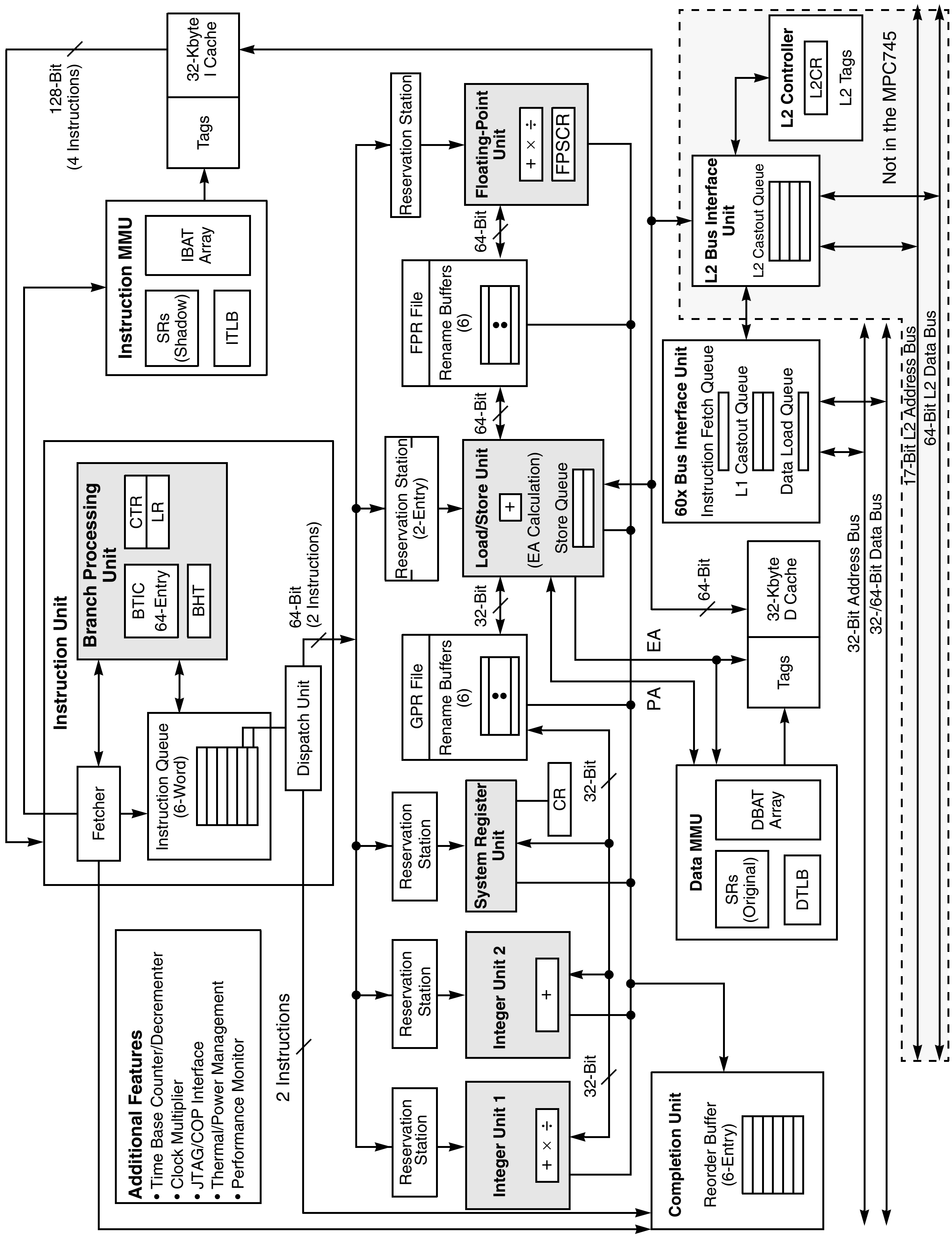


Figure 1. MPC755 Block Diagram

Figure 2 shows the allowable undershoot and overshoot voltage on the MPC755.

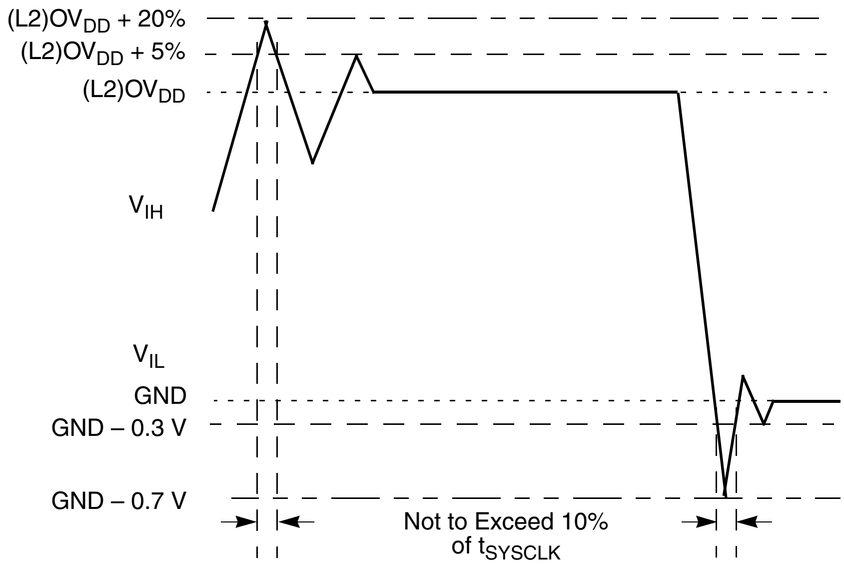


Figure 2. Overshoot/Undershoot Voltage

The MPC755 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC755 core voltage must always be provided at nominal 2.0 V (see Table 3 for actual recommended core voltage). Voltage to the L2 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 2. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL during operation. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

Table 2 describes the input threshold voltage setting.

Table 2. Input Threshold Voltage Setting

Part Revision	BVSEL Signal	Processor Bus Interface Voltage	L2VSEL Signal	L2 Bus Interface Voltage
E	0	Not Available	0	Not Available
	1	2.5 V/3.3 V	1	2.5 V/3.3 V

Caution: The input threshold selection must agree with the OV_{DD}/$L2OV_{DD}$ voltages supplied.

Note: The input threshold settings above are different for all revisions prior to Rev. 2.8 (Rev. E). For more information, refer to Section 10.2, "Part Numbers Not Fully Addressed by This Document."

Table 4. Package Thermal Characteristics [6]

Characteristic	Symbol	Value			Unit	Notes
		MPC755 CBGA	MPC755 PBGA	MPC745 PBGA		
Junction-to-ambient thermal resistance, natural convection	$R_{\theta JA}$	24	31	34	°C/W	1, 2
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JMA}$	17	25	26	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	18	25	27	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	14	21	22	°C/W	1, 3
Junction-to-board thermal resistance	$R_{\theta JB}$	8	17	17	°C/W	4
Junction-to-case thermal resistance	$R_{\theta JC}$	<0.1	<0.1	<0.1	°C/W	5

Notes:

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.
6. Refer to Section 8.8, "Thermal Management Information," for more details about thermal management.

The MPC755 incorporates a thermal management assist unit (TAU) composed of a thermal sensor, digital-to-analog converter, comparator, control logic, and dedicated special-purpose registers (SPRs). See the *MPC750 RISC Microprocessor Family User's Manual* for more information on the use of this feature. Specifications for the thermal sensor portion of the TAU are found in Table 5.

Table 10. Processor Bus AC Timing Specifications [1]

At recommended operating conditions (see Table 3)

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
Setup times: All inputs	t_{IVKH}	2.5	—	ns	
Input hold times: TLBISYNC, MCP, SMI	t_{IXKH}	0.6	—	ns	6
Input hold times: All inputs, except TLBISYNC, MCP, SMI	t_{IXKH}	0.2	—	ns	6
Valid times: All outputs	t_{KHOV}	—	4.1	ns	
Output hold times: All outputs	t_{KHOX}	1.0	—	ns	
SYSCLK to output enable	t_{KHOE}	0.5	—	ns	2
SYSCLK to output high impedance (all except ABB, ARTRY, DBB)	t_{KHOZ}	—	6.0	ns	2
SYSCLK to ABB, DBB high impedance after precharge	t_{KHABPZ}	—	1.0	t_{sysclk}	2, 3, 4
Maximum delay to ARTRY precharge	t_{KHARP}	—	1	t_{sysclk}	2, 3, 5
SYSCLK to ARTRY high impedance after precharge	t_{KHARPZ}	—	2	t_{sysclk}	2, 3, 5

Notes:

1. Revisions prior to Rev. 2.8 (Rev. E) were limited in performance and did not conform to this specification. For more information, refer to Section 10.2, "Part Numbers Not Fully Addressed by This Document."
2. Guaranteed by design and characterization.
3. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. Per the 60x bus protocol, TS, ABB, and DBB are driven only by the currently active bus master. They are asserted low, then precharged high before returning to high-Z as shown in Figure 6. The nominal precharge width for TS, ABB, or DBB is $0.5 \times t_{sysclk}$, that is, less than the minimum t_{sysclk} period, to ensure that another master asserting TS, ABB, or DBB on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
5. Per the 60x bus protocol, ARTRY can be driven by multiple bus masters through the clock period immediately following AACK. Bus contention is not an issue since any master asserting ARTRY will be driving it low. Any master asserting it low in the first clock following AACK will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of AACK. The nominal precharge width for ARTRY is 1.0 t_{sysclk}; that is, it should be high-Z as shown in Figure 6 before the first opportunity for another master to assert ARTRY. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z and precharge behavior is guaranteed by design.
6. MCP and SRESET must be held asserted for a minimum of two bus clock cycles; INT and SMI should be held asserted until the exception is taken; CKSTP_IN must be held asserted until the system has been reset. See the *MPC750 RISC Microprocessor Family User's Manual* for more information.

Figure 6 provides the input/output timing diagram for the MPC755.

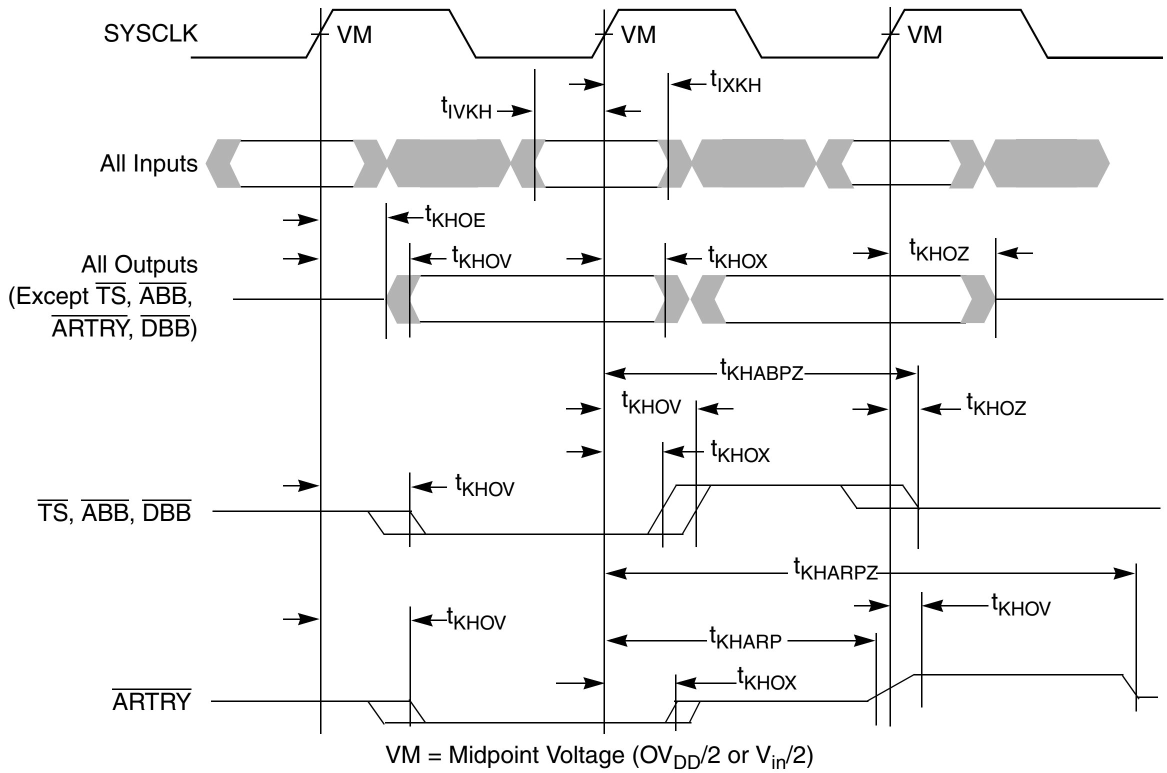


Figure 6. Input/Output Timing Diagram

4.2.3 L2 Clock AC Specifications

The L2CLK frequency is programmed by the L2 configuration register (L2CR[4–6]) core-to-L2 divisor ratio. See Table 17 for example core and L2 frequencies at various divisors. Table 11 provides the potential range of L2CLK output AC timing specifications as defined in Figure 7.

The minimum L2CLK frequency of Table 11 is specified by the maximum delay of the internal DLL. The variable-tap DLL introduces up to a full clock period delay in the L2CLK_OUTA, L2CLK_OUTB, and L2SYNC_OUT signals so that the returning L2SYNC_IN signal is phase-aligned with the next core clock (divided by the L2 divisor ratio). Do not choose a core-to-L2 divisor which results in an L2 frequency below this minimum, or the L2CLK_OUT signals provided for SRAM clocking will not be phase-aligned with the MPC755 core clock at the SRAMs.

The maximum L2CLK frequency shown in Table 11 is the core frequency divided by one. Very few L2 SRAM designs will be able to operate in this mode, especially at higher core frequencies. Therefore, most designs will select a greater core-to-L2 divisor to provide a longer L2CLK period for read and write access to the L2 SRAMs. The maximum L2CLK frequency for any application of the MPC755 will be a function of the AC timings of the MPC755, the AC timings for the SRAM, bus loading, and printed-circuit board trace length. The current AC timing of the MPC755 supports up to 200 MHz with typical, similarly-rated SRAM parts, provided careful design practices are observed. Clock trace lengths must be matched and all trace lengths should be as short as possible. Higher frequencies can be achieved by using better performing

Table 11. L2CLK Output AC Timing Specification

At recommended operating conditions (see Table 3)

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
L2CLK frequency	f_{L2CLK}	80	450	MHz	1, 4
L2CLK cycle time	t_{L2CLK}	2.5	12.5	ns	
L2CLK duty cycle	t_{CHCL}/t_{L2CLK}	45	55	%	2, 7
Internal DLL-relock time		640	—	L2CLK	3, 7
DLL capture window		0	10	ns	5, 7
L2CLK_OUT output-to-output skew	t_{L2CSKW}	—	50	ps	6, 7
L2CLK_OUT output jitter		—	±150	ps	6, 7

Notes:

1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB, L2CLK_OUT, and L2SYNC_OUT pins. The L2CLK frequency-to-core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. The maximum L2LCK frequency will be system dependent. L2CLK_OUTA and L2CLK_OUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The DLL-relock time is specified in terms of L2CLK periods. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in ns. Relock timing is guaranteed by design and characterization.
4. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz. This adds more delay to each tap of the DLL.
5. Allowable skew between L2SYNC_OUT and L2SYNC_IN.
6. This output jitter number represents the maximum delay of one tap forward or one tap back from the current DLL tap as the phase comparator seeks to minimize the phase difference between L2SYNC_IN and the internal L2CLK. This number must be comprehended in the L2 timing analysis. The input jitter on SYSCLK affects L2CLK_OUT and the L2 address/data/control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L2 timing analysis.
7. Guaranteed by design.

Figure 9 shows the L2 bus output timing diagrams for the MPC755.

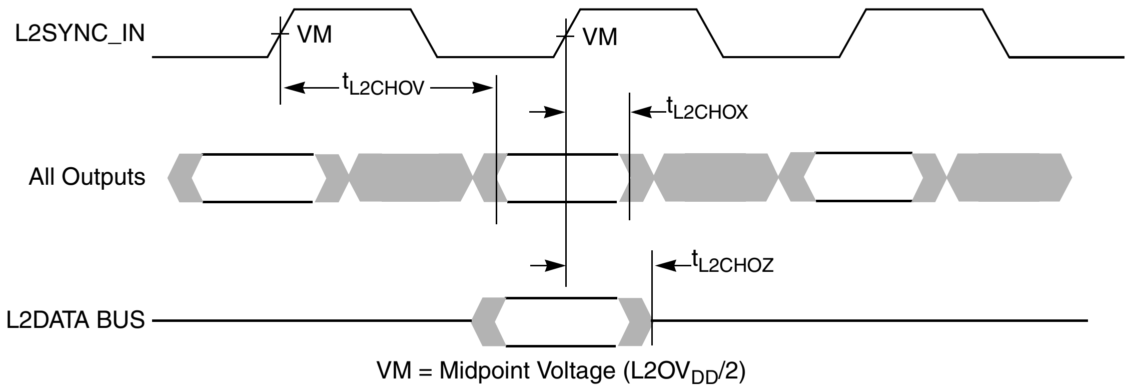


Figure 9. L2 Bus Output Timing Diagrams

Figure 10 provides the AC test load for L2 interface of the MPC755.

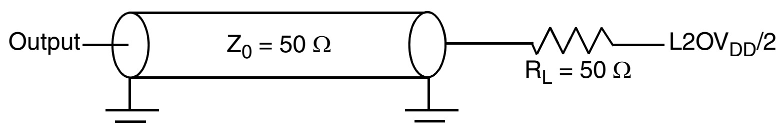


Figure 10. AC Test Load for the L2 Interface

Figure 15 provides the test access port timing diagram.

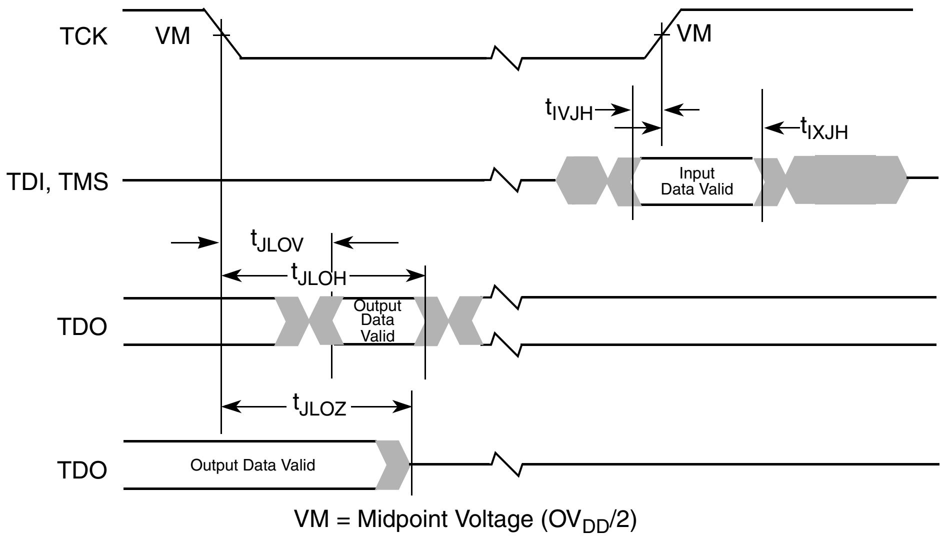
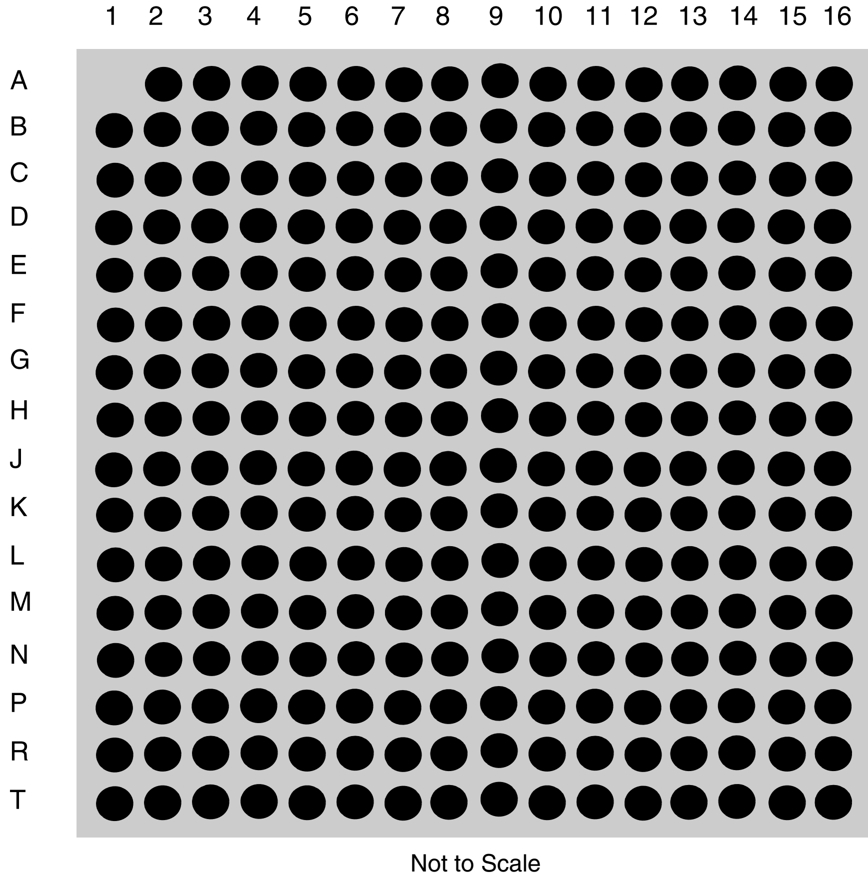


Figure 15. Test Access Port Timing Diagram

5 Pin Assignments

Figure 16 (in Part A) shows the pinout of the MPC745, 255 PBGA package as viewed from the top surface. Part B shows the side profile of the PBGA package to indicate the direction of the top surface view.

Part A



Part B

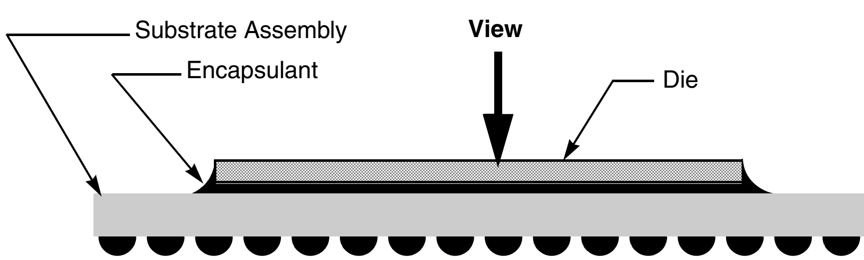


Figure 16. Pinout of the MPC745, 255 PBGA Package as Viewed from the Top Surface

Table 14. Pinout Listing for the MPC745, 255 PBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
VOLTDET	F3	High	Output	—	6

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals; and V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL pin configuration of Table 2 and the voltage supplied. For actual recommended value of V_{in} or supply voltages, see Table 3.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. This pin must be pulled up to OV_{DD} for proper operation of the processor interface. To allow for future I/O voltage changes, provide the option to connect BVSEL independently to either OV_{DD} or GND.
4. Uses 1 of 15 existing no connects in the MPC740, 255 BGA package.
5. Internal pull-up on die.
6. Internally tied to GND in the MPC745, 255 BGA package to indicate to the power supply that a low-voltage processor is present. This signal is not a power supply input.
   Caution: This differs from the MPC755, 360 BGA package.

Table 15 provides the pinout listing for the MPC755, 360 PBGA and CBGA packages.

Table 15. Pinout Listing for the MPC755, 360 BGA Package

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
A[0:31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O	OV_{DD}	
$\overline{\text{AACK}}$	N3	Low	Input	OV_{DD}	
$\overline{\text{ABB}}$	L7	Low	I/O	OV_{DD}	
AP[0:3]	C4, C5, C6, C7	High	I/O	OV_{DD}	
$\overline{\text{ARTRY}}$	L6	Low	I/O	OV_{DD}	
AV_{DD}	A8	—	—	2.0 V	
$\overline{\text{BG}}$	H1	Low	Input	OV_{DD}	
$\overline{\text{BR}}$	E7	Low	Output	OV_{DD}	
BVSEL	W1	High	Input	OV_{DD}	3, 5, 6
$\overline{\text{CI}}$	C2	Low	Output	OV_{DD}	
$\overline{\text{CKSTP\_IN}}$	B8	Low	Input	OV_{DD}	
$\overline{\text{CKSTP\_OUT}}$	D7	Low	Output	OV_{DD}	
CLK_OUT	E3	—	Output	OV_{DD}	
$\overline{\text{DBB}}$	K5	Low	I/O	OV_{DD}	
$\overline{\text{DBDIS}}$	G1	Low	Input	OV_{DD}	
$\overline{\text{DBG}}$	K1	Low	Input	OV_{DD}	
$\overline{\text{DBWO}}$	D1	Low	Input	OV_{DD}	

Table 15. Pinout Listing for the MPC755, 360 BGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
DH[0:31]	W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5	High	I/O	OV_{DD}	
DL[0:31]	M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2	High	I/O	OV_{DD}	
DP[0:7]	L1, P2, M2, V2, M1, N2, T3, R1	High	I/O	OV_{DD}	
$\overline{DRTRY}$	H6	Low	Input	OV_{DD}	
$\overline{GBL}$	B1	Low	I/O	OV_{DD}	
GND	D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16	—	—	GND	
$\overline{HRESET}$	B6	Low	Input	OV_{DD}	
$\overline{INT}$	C11	Low	Input	OV_{DD}	
L1_TSTCLK	F8	High	Input	—	2
L2ADDR[16:0]	G18, H19, J13, J14, H17, H18, J16, J17, J18, J19, K15, K17, K18, M19, L19, L18, L17	High	Output	$L2OV_{DD}$	
$L2AV_{DD}$	L13	—	—	2.0 V	
$\overline{L2CE}$	P17	Low	Output	$L2OV_{DD}$	
L2CLK_OUTA	N15	—	Output	$L2OV_{DD}$	
L2CLK_OUTB	L16	—	Output	$L2OV_{DD}$	
L2DATA[0:63]	U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13	High	I/O	$L2OV_{DD}$	
L2DP[0:7]	V14, U16, T19, N18, H14, F17, C19, B15	High	I/O	$L2OV_{DD}$	
$L2OV_{DD}$	D15, E14, E16, H16, J15, L15, M16, P15, R14, R16, T15, F15	—	—	$L2OV_{DD}$	
L2SYNC_IN	L14	—	Input	$L2OV_{DD}$	
L2SYNC_OUT	M14	—	Output	$L2OV_{DD}$	
L2_TSTCLK	F7	High	Input	—	2
L2VSEL	A19	High	Input	$L2OV_{DD}$	1, 5, 6, 7
$\overline{L2WE}$	N16	Low	Output	$L2OV_{DD}$	

Table 15. Pinout Listing for the MPC755, 360 BGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
L2ZZ	G17	High	Output	$L2OV_{DD}$	
$\overline{\text{LSSD\_MODE}}$	F9	Low	Input	—	2
$\overline{\text{MCP}}$	B11	Low	Input	OV_{DD}	
NC (No Connect)	B3, B4, B5, W19, K9, K11 [4], K19 [4]	—	—	—	
OV_{DD}	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12	—	—	OV_{DD}	
PLL_CFG[0:3]	A4, A5, A6, A7	High	Input	OV_{DD}	
$\overline{\text{QACK}}$	B2	Low	Input	OV_{DD}	
$\overline{\text{QREQ}}$	J3	Low	Output	OV_{DD}	
$\overline{\text{RSRV}}$	D3	Low	Output	OV_{DD}	
$\overline{\text{SMI}}$	A12	Low	Input	OV_{DD}	
$\overline{\text{SRESET}}$	E10	Low	Input	OV_{DD}	
SYSCLK	H9	—	Input	OV_{DD}	
$\overline{\text{TA}}$	F1	Low	Input	OV_{DD}	
TBEN	A2	High	Input	OV_{DD}	
$\overline{\text{TBST}}$	A11	Low	I/O	OV_{DD}	
TCK	B10	High	Input	OV_{DD}	
TDI	B7	High	Input	OV_{DD}	6
TDO	D9	High	Output	OV_{DD}	
$\overline{\text{TEA}}$	J1	Low	Input	OV_{DD}	
$\overline{\text{TLBISYNC}}$	A3	Low	Input	OV_{DD}	
TMS	C8	High	Input	OV_{DD}	6
$\overline{\text{TRST}}$	A10	Low	Input	OV_{DD}	6
$\overline{\text{TS}}$	K7	Low	I/O	OV_{DD}	
TSIZ[0:2]	A9, B9, C9	High	Output	OV_{DD}	
TT[0:4]	C10, D11, B12, C12, F11	High	I/O	OV_{DD}	
$\overline{\text{WT}}$	C3	Low	Output	OV_{DD}	
V_{DD}	G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12	—	—	2.0 V	

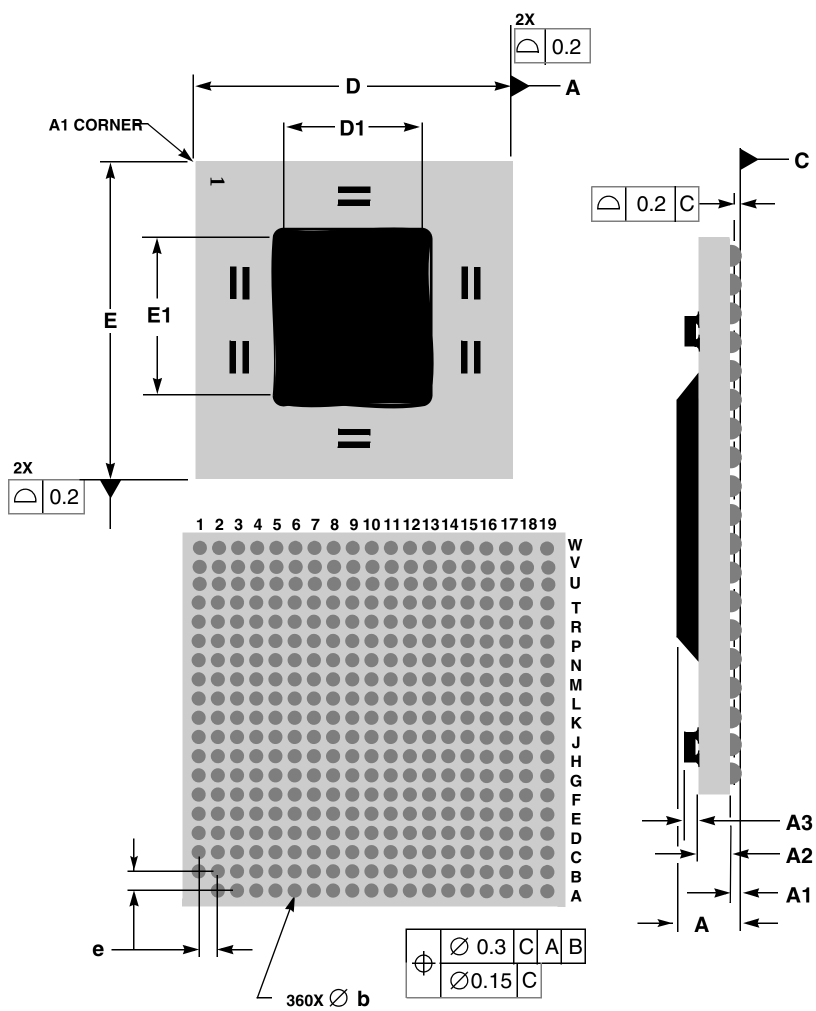
7.3 Package Parameters for the MPC755 CBGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead ceramic ball grid array (CBGA).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.65 mm
Maximum module height	3.20 mm
Ball diameter	0.89 mm (35 mil)

7.4 Mechanical Dimensions for the MPC755 CBGA

Figure 19 provides the mechanical dimensions and bottom surface nomenclature for the MPC755, 360 CBGA package.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.

	Millimeters	
DIM	Min	Max
A	2.65	3.20
A1	0.79	0.99
A2	1.10	1.30
A3	—	0.60
b	0.82	0.93
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	

Figure 19. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC755, 360 CBGA Package

Table 18 summarizes the signal impedance results. The driver impedance values were characterized at 0°, 65°, and 105°C. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 18. Impedance Characteristics

V_{DD} = 2.0 V, OV_{DD} = 3.3 V, T_j = 0°–105°C

Impedance	Processor Bus	L2 Bus	Symbol	Unit
R_N	25–36	25–36	Z_0	Ω
R_P	26–39	26–39	Z_0	Ω

8.6 Pull-Up Resistor Requirements

The MPC755 requires pull-up resistors (1–5 kΩ) on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC755 or other bus masters. These pins are $\overline{TS}$, $\overline{ABB}$, $\overline{AACK}$, $\overline{ARTRY}$, $\overline{DBB}$, $\overline{DBWO}$, $\overline{TA}$, $\overline{TEA}$, and $\overline{DBDIS}$. $\overline{DRTRY}$ should also be connected to a pull-up resistor (1–5 kΩ) if it will be used by the system; otherwise, this signal should be connected to $\overline{HRESET}$ to select NO-DRTRY mode (see the *MPC750 RISC Microprocessor Family User's Manual* for more information on this mode).

Three test pins also require pull-up resistors (100 Ω–1 kΩ). These pins are L1_TSTCLK, L2_TSTCLK, and $\overline{LSSD\_MODE}$. These signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.

In addition, $\overline{CKSTP\_OUT}$ is an open-drain style output that requires a pull-up resistor (1–5 kΩ) if it is used by the system.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Since the MPC755 must continually monitor these signals for snooping, this float condition may cause additional power draw by the input receivers on the MPC755 or by other receivers in the system. These signals can be pulled up through weak (10-kΩ) pull-up resistors by the system or may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw, but address bus pull-up resistors are not necessary for proper device operation. The snooped address and transfer attribute inputs are: A[0:31], AP[0:3], TT[0:4], $\overline{TBST}$, and $\overline{GBL}$.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: DH[0:31], DL[0:31], and DP[0:7].

If 32-bit data bus mode is selected, the input receivers of the unused data and parity bits will be disabled, and their outputs will drive logic zeros when they would otherwise normally be driven. For this mode, these pins do not require pull-up resistors, and should be left unconnected by the system to minimize possible output switching.

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If all parity generation is disabled through HID0, then all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

The L2 interface does not require pull-up resistors.

8.7 JTAG Configuration Signals

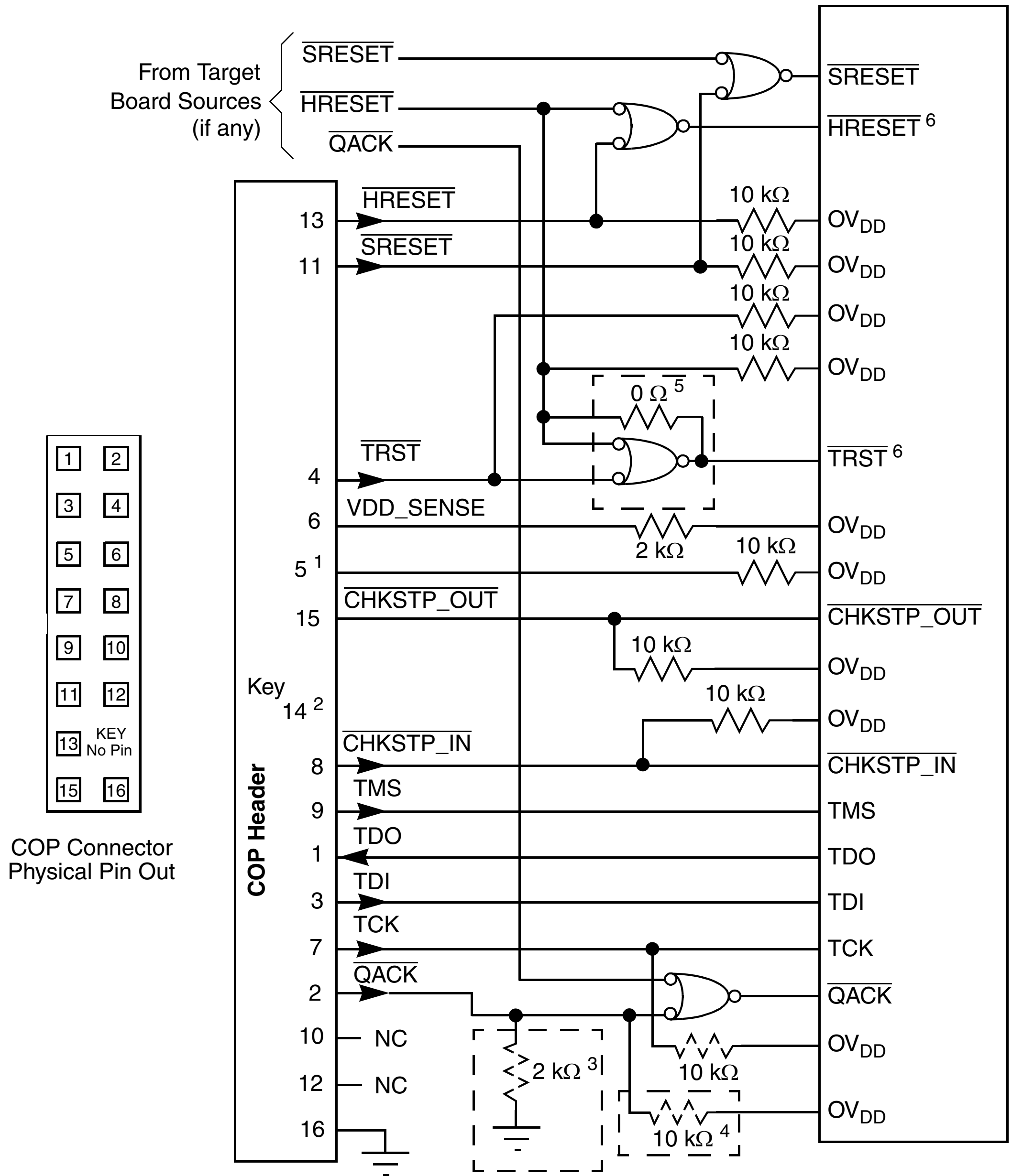
Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 24 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted ensuring that the JTAG scan chain is initialized during power-on. While Freescale recommends that the COP header be designed into the system as shown in Figure 24, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 24 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.



Notes:

1. RUN/STOP, normally found on pin 5 of the COP header, is not implemented on the MPC755. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive QACK.
4. Populate only if debug tool uses an open-drain type output and does not actively deassert QACK.
5. If the JTAG interface is implemented, connect HRESET from the target source to TRST from the COP header though an AND gate to TRST of the part. If the JTAG interface is not implemented, connect HRESET from the target source to TRST of the part through a 0-Ω isolation resistor.
6. The COP port and target board should be able to independently assert HRESET and TRST to the processor in order to fully control the processor as shown above.

Figure 24. JTAG Interface Connection

There is no standardized way to number the COP header shown in Figure 24; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 25 is common to all known emulators.

The $\overline{QACK}$ signal shown in Figure 24 is usually connected to the PCI bridge chip in a system and is an input to the MPC755 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC755 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{QACK}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is deasserted when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{QACK}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{QACK}$ should be merged via logic so that it also can be driven by the PCI bridge.

8.8 Thermal Management Information

This section provides thermal management information for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly; see Figure 25. This spring force should not exceed 5.5 pounds (2.5 kg) of force.

Figure 25 describes the package exploded cross-sectional view with several heat sink options.

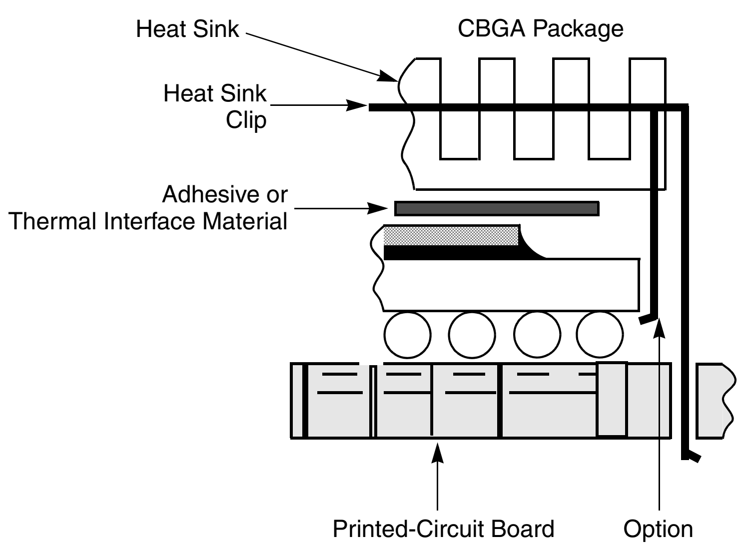


Figure 25. Package Exploded Cross-Sectional View with Several Heat Sink Options

The board designer can choose between several types of heat sinks to place on the MPC755. There are several commercially-available heat sinks for the MPC755 provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

8.8.1 Internal Package Conduction Resistance

For the exposed-die packaging technology, shown in Table 4, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case (or top-of-die for exposed silicon) thermal resistance
- The die junction-to-ball thermal resistance

Figure 26 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.

Shin-Etsu MicroSi, Inc. 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

8.8.3 Heat Sink Selection Example

This section provides a heat sink selection example using one of the commercially-available heat sinks. For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) \times P_d$$

where:

T_j is the die-junction temperature

T_a is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

θ_{jc} is the junction-to-case thermal resistance

θ_{int} is the adhesive or interface material thermal resistance

θ_{sa} is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation the die-junction temperatures (T_j) should be maintained less than the value specified in Table 3. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material (θ_{int}) is typically about 1°C/W. Assuming a T_a of 30°C, a T_r of 5°C, a CBGA package $R_{\theta jc} < 0.1$, and a power consumption (P_d) of 5.0 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 1.0°C/W + \theta_{sa}) \times 5.0\ W$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{sa}) versus airflow velocity is shown in Figure 28.

Assuming an air velocity of 0.5 m/s, we have an effective R_{sa} of 7°C/W, thus

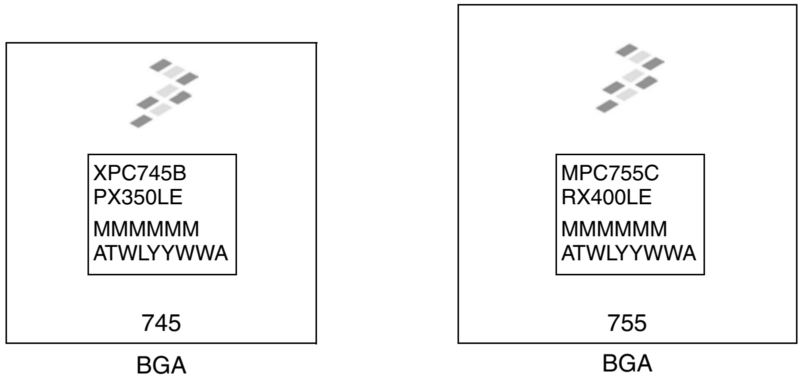
$$T_j = 30°C + 5°C + (0.1°C/W + 1.0°C/W + 7°C/W) \times 5.0\ W,$$

resulting in a die-junction temperature of approximately 76°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, The Bergquist Company, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.

10.3 Part Marking

Parts are marked as the example shown in Figure 29.



Notes:

MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 29. Part Marking for BGA Device