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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	350MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-CBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc755brx350le

Figure 2 shows the allowable undershoot and overshoot voltage on the MPC755.

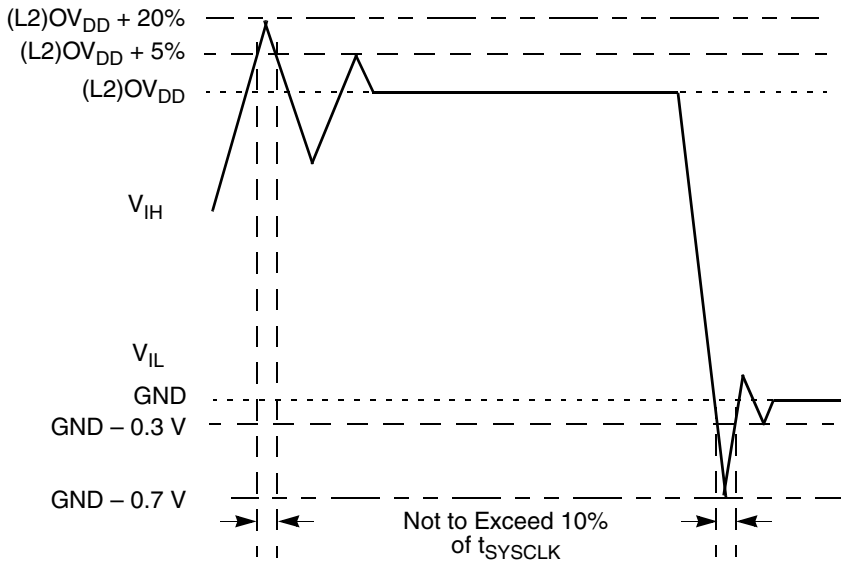


Figure 2. Overshoot/Undershoot Voltage

The MPC755 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC755 core voltage must always be provided at nominal 2.0 V (see Table 3 for actual recommended core voltage). Voltage to the L2 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 2. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL during operation. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

Table 2 describes the input threshold voltage setting.

Table 2. Input Threshold Voltage Setting

Part Revision	BVSEL Signal	Processor Bus Interface Voltage	L2VSEL Signal	L2 Bus Interface Voltage
E	0	Not Available	0	Not Available
	1	2.5 V/3.3 V	1	2.5 V/3.3 V

Caution: The input threshold selection must agree with the OV_{DD}/$L2OV_{DD}$ voltages supplied.

Note: The input threshold settings above are different for all revisions prior to Rev. 2.8 (Rev. E). For more information, refer to Section 10.2, "Part Numbers Not Fully Addressed by This Document."

Table 4. Package Thermal Characteristics [6]

Characteristic	Symbol	Value			Unit	Notes
		MPC755 CBGA	MPC755 PBGA	MPC745 PBGA		
Junction-to-ambient thermal resistance, natural convection	$R_{\theta JA}$	24	31	34	°C/W	1, 2
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JMA}$	17	25	26	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	18	25	27	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	14	21	22	°C/W	1, 3
Junction-to-board thermal resistance	$R_{\theta JB}$	8	17	17	°C/W	4
Junction-to-case thermal resistance	$R_{\theta JC}$	<0.1	<0.1	<0.1	°C/W	5

Notes:

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.
6. Refer to Section 8.8, "Thermal Management Information," for more details about thermal management.

The MPC755 incorporates a thermal management assist unit (TAU) composed of a thermal sensor, digital-to-analog converter, comparator, control logic, and dedicated special-purpose registers (SPRs). See the *MPC750 RISC Microprocessor Family User's Manual* for more information on the use of this feature. Specifications for the thermal sensor portion of the TAU are found in Table 5.

Table 5. Thermal Sensor Specifications

At recommended operating conditions (see Table 3)

Characteristic	Min	Max	Unit	Notes
Temperature range	0	127	°C	1
Comparator settling time	20	—	µs	2, 3
Resolution	4	—	°C	3
Accuracy	–12	+12	°C	3

Notes:

1. The temperature is the junction temperature of the die. The thermal assist unit's raw output does not indicate an absolute temperature, but must be interpreted by software to derive the absolute junction temperature. For information about the use and calibration of the TAU, see Freescale Application Note AN1800/D, *Programming the Thermal Assist Unit in the MPC750 Microprocessor.*
2. The comparator settling time value must be converted into the number of CPU clocks that need to be written into the THRM3 SPR.
3. Guaranteed by design and characterization.

Table 6 provides the DC electrical characteristics for the MPC755.

Table 6. DC Electrical Specifications

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage [1]	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs except SYSCLK)	2.5	V_{IH}	1.6	(L2)OV_{DD} + 0.3	V	2, 3
	3.3	V_{IH}	2.0	(L2)OV_{DD} + 0.3	V	2, 3
Input low voltage (all inputs except SYSCLK)	2.5	V_{IL}	–0.3	0.6	V	2
	3.3	V_{IL}	–0.3	0.8	V	
SYSCLK input high voltage	2.5	KV_{IH}	1.8	OV_{DD} + 0.3	V	
	3.3	KV_{IH}	2.4	OV_{DD} + 0.3	V	
SYSCLK input low voltage	2.5	KV_{IL}	–0.3	0.4	V	
	3.3	KV_{IL}	–0.3	0.4	V	
Input leakage current, V_{in} = L2OV_{DD}/OV_{DD}		I_{in}	—	10	µA	2, 3
High-Z (off-state) leakage current, V_{in} = L2OV_{DD}/OV_{DD}		I_{TSI}	—	10	µA	2, 3, 5
Output high voltage, I_{OH} = –6 mA	2.5	V_{OH}	1.7	—	V	
	3.3	V_{OH}	2.4	—	V	
Output low voltage, I_{OL} = 6 mA	2.5	V_{OL}	—	0.45	V	
	3.3	V_{OL}	—	0.4	V	

Table 6. DC Electrical Specifications (continued)

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage [1]	Symbol	Min	Max	Unit	Notes
Capacitance, V_{in} = 0 V, f = 1 MHz		C_{in}	—	5.0	pF	3, 4

Notes:

1. Nominal voltages; see Table 3 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD} while $L2OV_{DD}$ is the reference for the L2 bus signals.
3. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK) and IEEE 1149.1 boundary scan (JTAG) signals.
4. Capacitance is periodically sampled rather than 100% tested.
5. The leakage is measured for nominal OV_{DD} and V_{DD}, or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or –5%).

Table 7 provides the power consumption for the MPC755.

Table 7. Power Consumption for MPC755

	Processor (CPU) Frequency			Unit	Notes
	300 MHz	350 MHz	400 MHz		
Full-Power Mode					
Typical	3.1	3.6	5.4	W	1, 3, 4
Maximum	4.5	6.0	8.0	W	1, 2
Doze Mode					
Maximum	1.8	2.0	2.3	W	1, 2, 4
Nap Mode					
Maximum	1.0	1.0	1.0	W	1, 2, 4
Sleep Mode					
Maximum	550	550	550	mW	1, 2, 4
Sleep Mode (PLL and DLL Disabled)					
Maximum	510	510	510	mW	1, 2

Notes:

1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O supply power (OV_{DD} and $L2OV_{DD}$) or PLL/DLL supply power (AV_{DD} and $L2AV_{DD}$). OV_{DD} and $L2OV_{DD}$ power is system dependent, but is typically <10% of V_{DD} power. Worst case power consumption for AV_{DD} = 15 mW and $L2AV_{DD}$ = 15 mW.
2. Maximum power is measured at nominal V_{DD} (see Table 3) while running an entirely cache-resident, contrived sequence of instructions which keep the execution units maximally busy.
3. Typical power is an average value measured at the nominal recommended V_{DD} (see Table 3) and 65°C in a system while running a typical code sequence.
4. Not 100% tested. Characterized and periodically sampled.

Figure 3 provides the SYSCLK input timing diagram.

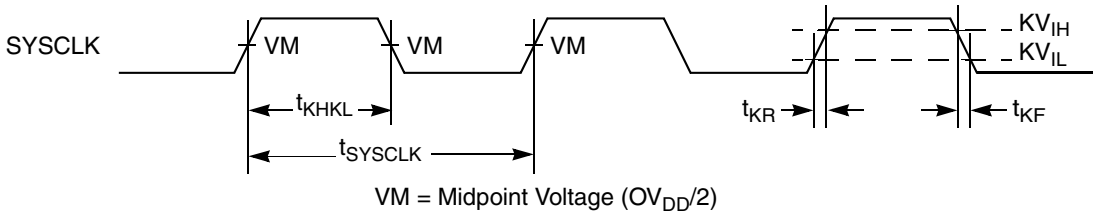


Figure 3. SYSCLK Input Timing Diagram

4.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC755 as defined in Figure 4 and Figure 6. Timing specifications for the L2 bus are provided in Section 4.2.3, "L2 Clock AC Specifications."

Table 9. Processor Bus Mode Selection AC Timing Specifications [1]

At recommended operating conditions (see Table 3)

Parameter	Symbol [2]	All Speed Grades		Unit	Notes
		Min	Max		
Mode select input setup to $\overline{\text{HRESET}}$	t_{MVRH}	8	—	t_{sysclk}	3, 4, 5, 6, 7
$\overline{\text{HRESET}}$ to mode select input hold	t_{MXRH}	0	—	ns	3, 4, 6, 7, 8

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 5). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK (K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH)—note the position of the reference and its state for inputs—and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 4).
4. This specification is for configuration mode select only. Also note that the $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
5. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
6. Mode select signals are BVSEL, L2VSEL, PLL_CFG[0:3], and $\overline{\text{TLBISYNC}}$.
7. Guaranteed by design and characterization.
8. Bus mode select pins must remain stable during operation. Changing the logic states of BVSEL or L2VSEL during operation will cause the bus mode voltage selection to change. Changing the logic states of the PLL_CFG pins during operation will cause the PLL division ratio selection to change. Both of these conditions are considered outside the specification and are not supported. Once $\overline{\text{HRESET}}$ is negated the states of the bus mode selection pins must remain stable.

Figure 4 provides the mode select input timing diagram for the MPC755.

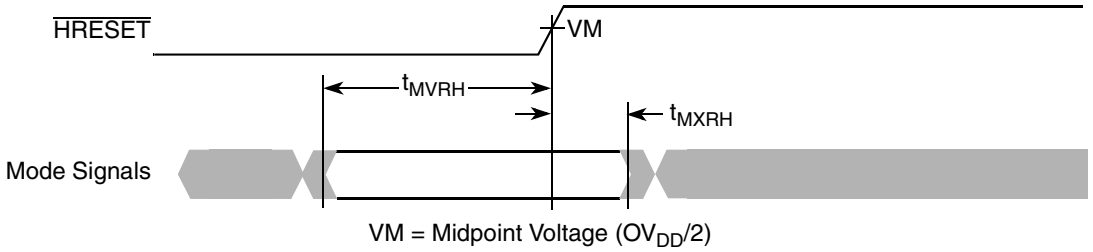


Figure 4. Mode Input Timing Diagram

Figure 5 provides the AC test load for the MPC755.

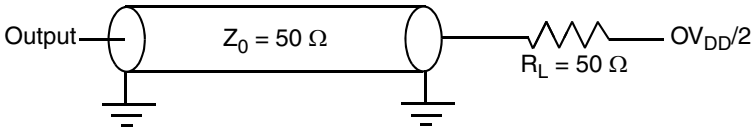


Figure 5. AC Test Load

Figure 6 provides the input/output timing diagram for the MPC755.

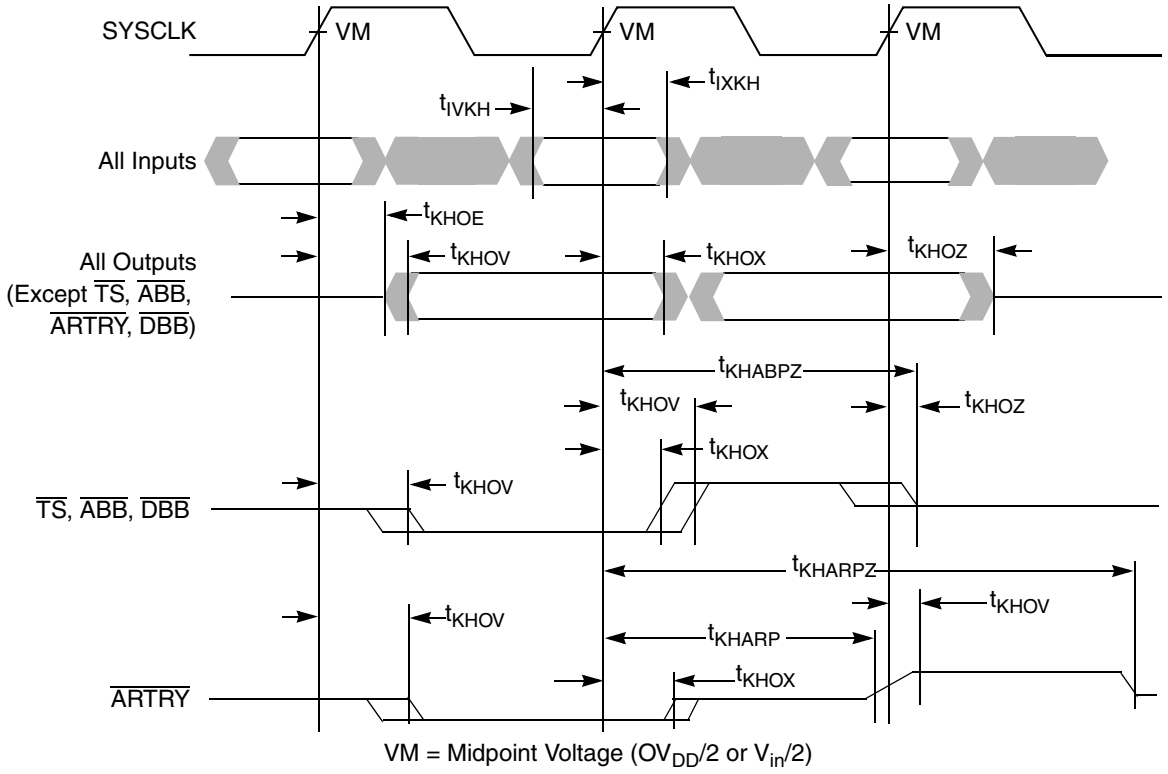


Figure 6. Input/Output Timing Diagram

4.2.3 L2 Clock AC Specifications

The L2CLK frequency is programmed by the L2 configuration register (L2CR[4–6]) core-to-L2 divisor ratio. See Table 17 for example core and L2 frequencies at various divisors. Table 11 provides the potential range of L2CLK output AC timing specifications as defined in Figure 7.

The minimum L2CLK frequency of Table 11 is specified by the maximum delay of the internal DLL. The variable-tap DLL introduces up to a full clock period delay in the L2CLK_OUTA, L2CLK_OUTB, and L2SYNC_OUT signals so that the returning L2SYNC_IN signal is phase-aligned with the next core clock (divided by the L2 divisor ratio). Do not choose a core-to-L2 divisor which results in an L2 frequency below this minimum, or the L2CLK_OUT signals provided for SRAM clocking will not be phase-aligned with the MPC755 core clock at the SRAMs.

The maximum L2CLK frequency shown in Table 11 is the core frequency divided by one. Very few L2 SRAM designs will be able to operate in this mode, especially at higher core frequencies. Therefore, most designs will select a greater core-to-L2 divisor to provide a longer L2CLK period for read and write access to the L2 SRAMs. The maximum L2CLK frequency for any application of the MPC755 will be a function of the AC timings of the MPC755, the AC timings for the SRAM, bus loading, and printed-circuit board trace length. The current AC timing of the MPC755 supports up to 200 MHz with typical, similarly-rated SRAM parts, provided careful design practices are observed. Clock trace lengths must be matched and all trace lengths should be as short as possible. Higher frequencies can be achieved by using better performing

Table 11. L2CLK Output AC Timing Specification

At recommended operating conditions (see Table 3)

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
L2CLK frequency	f_{L2CLK}	80	450	MHz	1, 4
L2CLK cycle time	t_{L2CLK}	2.5	12.5	ns	
L2CLK duty cycle	t_{CHCL}/t_{L2CLK}	45	55	%	2, 7
Internal DLL-relock time		640	—	L2CLK	3, 7
DLL capture window		0	10	ns	5, 7
L2CLK_OUT output-to-output skew	t_{L2CSKW}	—	50	ps	6, 7
L2CLK_OUT output jitter		—	±150	ps	6, 7

Notes:

1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB, L2CLK_OUT, and L2SYNC_OUT pins. The L2CLK frequency-to-core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. The maximum L2LCK frequency will be system dependent. L2CLK_OUTA and L2CLK_OUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The DLL-relock time is specified in terms of L2CLK periods. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in ns. Relock timing is guaranteed by design and characterization.
4. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz. This adds more delay to each tap of the DLL.
5. Allowable skew between L2SYNC_OUT and L2SYNC_IN.
6. This output jitter number represents the maximum delay of one tap forward or one tap back from the current DLL tap as the phase comparator seeks to minimize the phase difference between L2SYNC_IN and the internal L2CLK. This number must be comprehended in the L2 timing analysis. The input jitter on SYSCLK affects L2CLK_OUT and the L2 address/data/control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L2 timing analysis.
7. Guaranteed by design.

Figure 12 provides the JTAG clock input timing diagram.

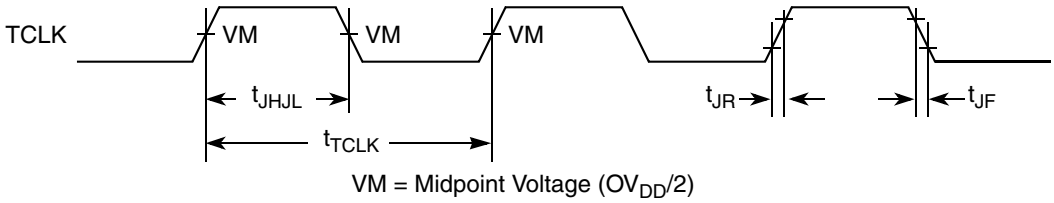


Figure 12. JTAG Clock Input Timing Diagram

Figure 13 provides the $\overline{\text{TRST}}$ timing diagram.

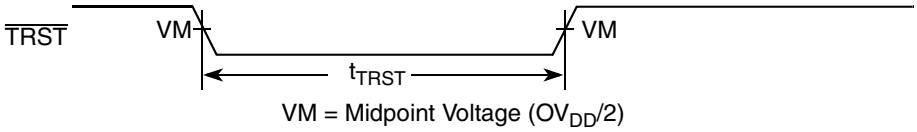


Figure 13. $\overline{\text{TRST}}$ Timing Diagram

Figure 14 provides the boundary-scan timing diagram.

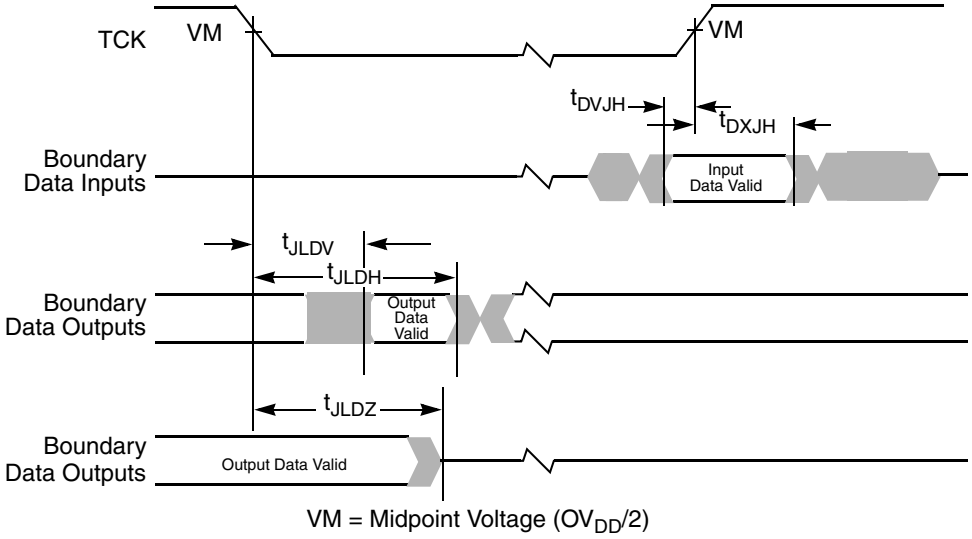
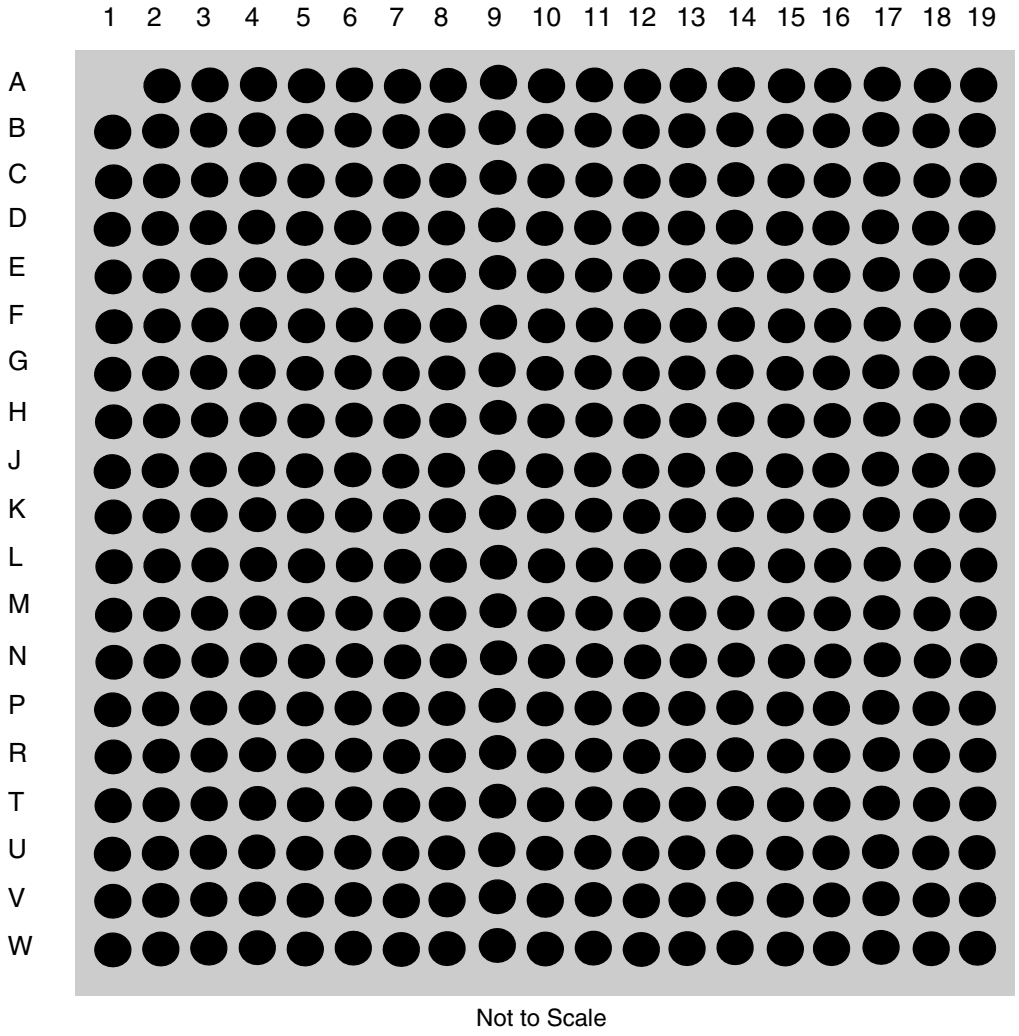


Figure 14. Boundary-Scan Timing Diagram

Figure 17 (in Part A) shows the pinout of the MPC755, 360 PBGA and 360 CBGA packages as viewed from the top surface. Part B shows the side profile of the PBGA and CBGA package to indicate the direction of the top surface view.

Part A



Part B

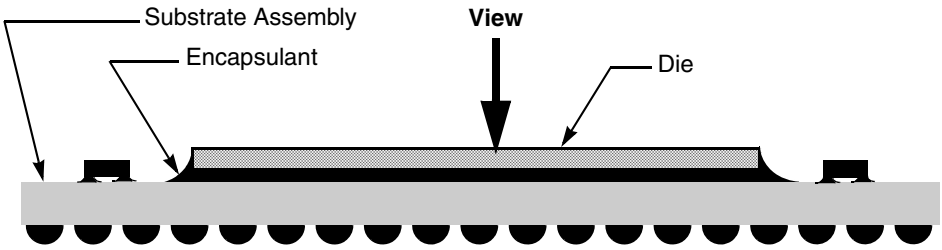


Figure 17. Pinout of the MPC755, 360 PBGA and CBGA Packages as Viewed from the Top Surface

Table 14. Pinout Listing for the MPC745, 255 PBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
$\overline{\text{INT}}$	B15	Low	Input	OV_{DD}	
L1_TSTCLK	D11	High	Input	—	2
L2_TSTCLK	D12	High	Input	—	2
$\overline{\text{LSSD\_MODE}}$	B10	Low	Input	—	2
$\overline{\text{MCP}}$	C13	Low	Input	OV_{DD}	
NC (No Connect)	B7, B8, C3, C6, C8, D5, D6, H4, J16, A4, A5, A2, A3, B5	—	—	—	
OV_{DD}	C7, E5, E7, E10, E12, G3, G5, G12, G14, K3, K5, K12, K14, M5, M7, M10, M12, P7, P10	—	—	2.5 V/3.3 V	
PLL_CFG[0:3]	A8, B9, A9, D9	High	Input	OV_{DD}	
$\overline{\text{QACK}}$	D3	Low	Input	OV_{DD}	
$\overline{\text{QREQ}}$	J3	Low	Output	OV_{DD}	
$\overline{\text{RSRV}}$	D1	Low	Output	OV_{DD}	
$\overline{\text{SMI}}$	A16	Low	Input	OV_{DD}	
$\overline{\text{SRESET}}$	B14	Low	Input	OV_{DD}	
SYSCLK	C9	—	Input	OV_{DD}	
$\overline{\text{TA}}$	H14	Low	Input	OV_{DD}	
TBEN	C2	High	Input	OV_{DD}	
$\overline{\text{TBST}}$	A14	Low	I/O	OV_{DD}	
TCK	C11	High	Input	OV_{DD}	
TDI	A11	High	Input	OV_{DD}	5
TDO	A12	High	Output	OV_{DD}	
$\overline{\text{TEA}}$	H13	Low	Input	OV_{DD}	
$\overline{\text{TLBISYNC}}$	C4	Low	Input	OV_{DD}	
TMS	B11	High	Input	OV_{DD}	5
$\overline{\text{TRST}}$	C10	Low	Input	OV_{DD}	5
$\overline{\text{TS}}$	J13	Low	I/O	OV_{DD}	
TSIZ[0:2]	A13, D10, B12	High	Output	OV_{DD}	
TT[0:4]	B13, A15, B16, C14, C15	High	I/O	OV_{DD}	
$\overline{\text{WT}}$	D2	Low	Output	OV_{DD}	
V_{DD}	F6, F8, F9, F11, G7, G10, H6, H8, H9, H11, J6, J8, J9, J11, K7, K10, L6, L8, L9, L11	—	—	2.0 V	

Table 15. Pinout Listing for the MPC755, 360 BGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
L2ZZ	G17	High	Output	$L2OV_{DD}$	
$\overline{\text{LSSD\_MODE}}$	F9	Low	Input	—	2
$\overline{\text{MCP}}$	B11	Low	Input	OV_{DD}	
NC (No Connect)	B3, B4, B5, W19, K9, K11 [4], K19 [4]	—	—	—	
OV_{DD}	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12	—	—	OV_{DD}	
PLL_CFG[0:3]	A4, A5, A6, A7	High	Input	OV_{DD}	
$\overline{\text{QACK}}$	B2	Low	Input	OV_{DD}	
$\overline{\text{QREQ}}$	J3	Low	Output	OV_{DD}	
$\overline{\text{RSRV}}$	D3	Low	Output	OV_{DD}	
$\overline{\text{SMI}}$	A12	Low	Input	OV_{DD}	
$\overline{\text{SRESET}}$	E10	Low	Input	OV_{DD}	
SYSCLK	H9	—	Input	OV_{DD}	
$\overline{\text{TA}}$	F1	Low	Input	OV_{DD}	
TBEN	A2	High	Input	OV_{DD}	
$\overline{\text{TBST}}$	A11	Low	I/O	OV_{DD}	
TCK	B10	High	Input	OV_{DD}	
TDI	B7	High	Input	OV_{DD}	6
TDO	D9	High	Output	OV_{DD}	
$\overline{\text{TEA}}$	J1	Low	Input	OV_{DD}	
$\overline{\text{TLBISYNC}}$	A3	Low	Input	OV_{DD}	
TMS	C8	High	Input	OV_{DD}	6
$\overline{\text{TRST}}$	A10	Low	Input	OV_{DD}	6
$\overline{\text{TS}}$	K7	Low	I/O	OV_{DD}	
TSIZ[0:2]	A9, B9, C9	High	Output	OV_{DD}	
TT[0:4]	C10, D11, B12, C12, F11	High	I/O	OV_{DD}	
$\overline{\text{WT}}$	C3	Low	Output	OV_{DD}	
V_{DD}	G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12	—	—	2.0 V	

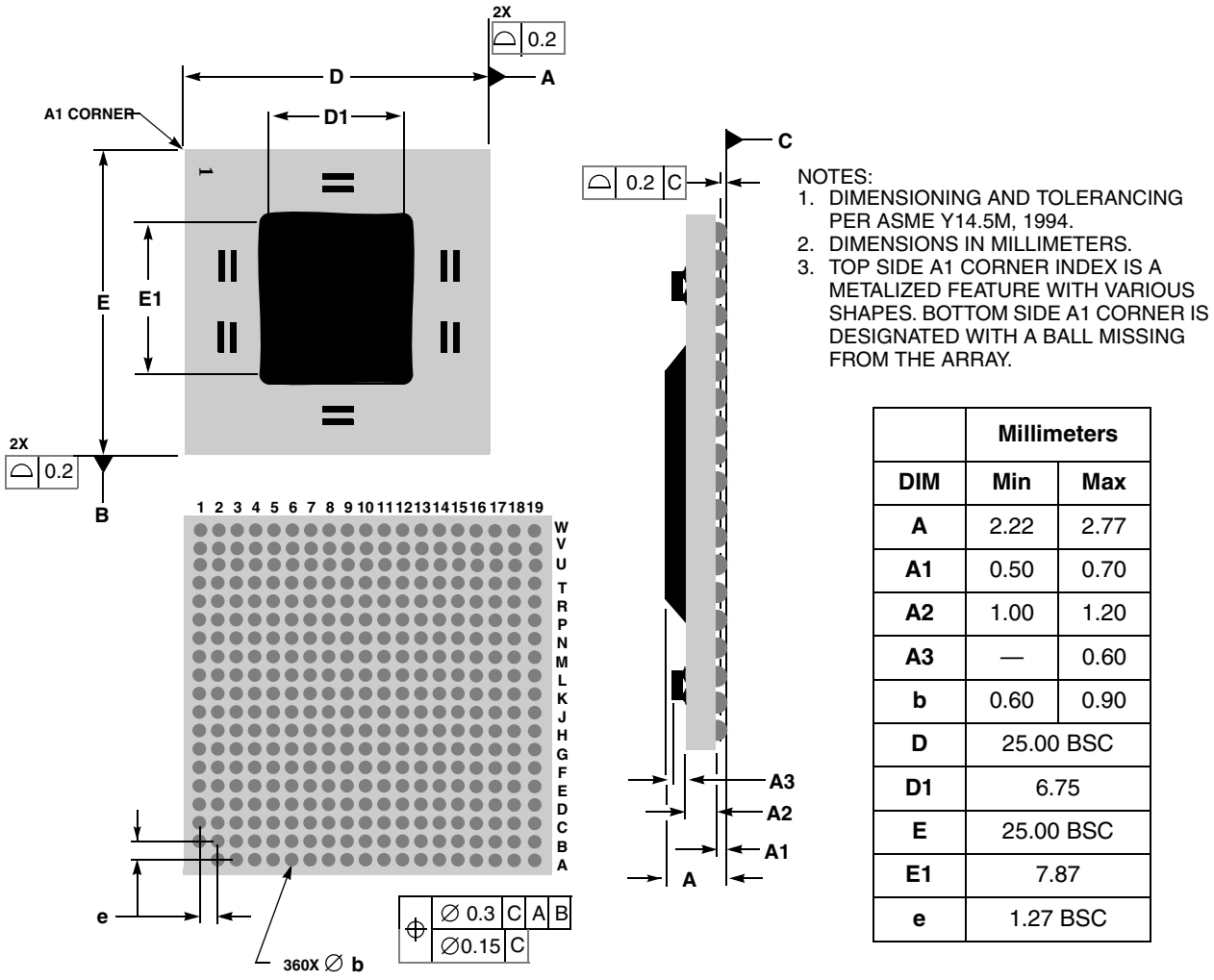
7.5 Package Parameters for the MPC755 PBGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead plastic ball grid array (PBGA).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.22 mm
Maximum module height	2.77 mm
Ball diameter	0.75 mm (29.5 mil)

7.6 Mechanical Dimensions for the MPC755

Figure 20 provides the mechanical dimensions and bottom surface nomenclature for the MPC755, 360 PBGA package.



	Millimeters	
DIM	Min	Max
A	2.22	2.77
A1	0.50	0.70
A2	1.00	1.20
A3	—	0.60
b	0.60	0.90
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	

Figure 20. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC755, 360 PBGA Package

Table 17. Sample Core-to-L2 Frequencies (continued)

Core Frequency (MHz)	÷1	÷1.5	÷2	÷2.5	÷3
375	375	250	188	150	125
400	400	266	200	160	133

Note: The core and L2 frequencies are for reference only. Some examples may represent core or L2 frequencies which are not useful, not supported, or not tested for by the MPC755; see Section 4.2.3, "L2 Clock AC Specifications," for valid L2CLK frequencies. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz.

8.2 PLL Power Supply Filtering

The AV_{DD} and $L2AV_{DD}$ power signals are provided on the MPC755 to provide power to the clock generation PLL and L2 cache DLL, respectively. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 21 using surface mount capacitors with minimum Effective Series Inductance (ESL) is recommended. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. An identical but separate circuit should be placed as close as possible to the $L2AV_{DD}$ pin. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 BGA footprint, without the inductance of vias. The $L2AV_{DD}$ pin may be more difficult to route, but is proportionately less critical.

Figure 21 shows the PLL power supply filter circuit.

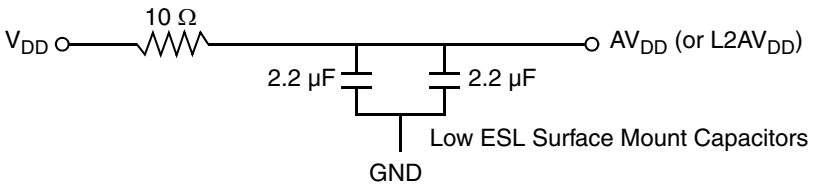
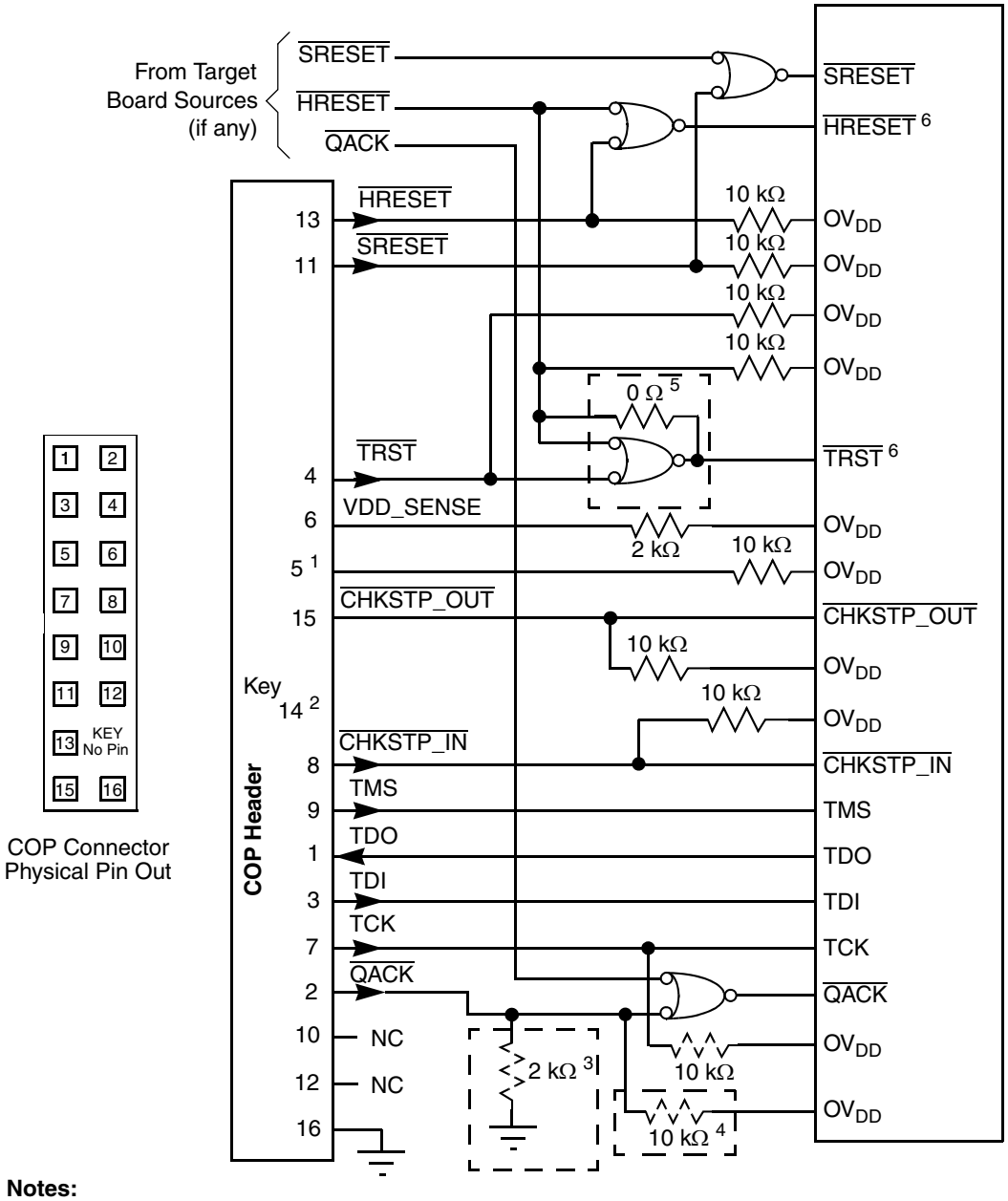


Figure 21. PLL Power Supply Filter Circuit

8.3 Decoupling Recommendations

Due to the MPC755 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC755 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC755 system, and the MPC755 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and $L2OV_{DD}$ pin of the MPC755. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, $(L2)OV_{DD}$, and GND power planes in the PCB, utilizing short traces to minimize inductance.



Notes:

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the MPC755. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively deassert $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0-Ω isolation resistor.
6. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.

Figure 24. JTAG Interface Connection

Shin-Etsu MicroSi, Inc. 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

8.8.3 Heat Sink Selection Example

This section provides a heat sink selection example using one of the commercially-available heat sinks. For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) \times P_d$$

where:

T_j is the die-junction temperature
T_a is the inlet cabinet ambient temperature
T_r is the air temperature rise within the computer cabinet
θ_{jc} is the junction-to-case thermal resistance
θ_{int} is the adhesive or interface material thermal resistance
θ_{sa} is the heat sink base-to-ambient thermal resistance
P_d is the power dissipated by the device

During operation the die-junction temperatures (T_j) should be maintained less than the value specified in Table 3. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material (θ_{int}) is typically about 1°C/W. Assuming a T_a of 30°C, a T_r of 5°C, a CBGA package $R_{\theta jc} < 0.1$, and a power consumption (P_d) of 5.0 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 1.0°C/W + \theta_{sa}) \times 5.0\ W$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{sa}) versus airflow velocity is shown in Figure 28.

Assuming an air velocity of 0.5 m/s, we have an effective R_{sa} of 7°C/W, thus

$$T_j = 30°C + 5°C + (0.1°C/W + 1.0°C/W + 7°C/W) \times 5.0\ W,$$

resulting in a die-junction temperature of approximately 76°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, The Bergquist Company, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.

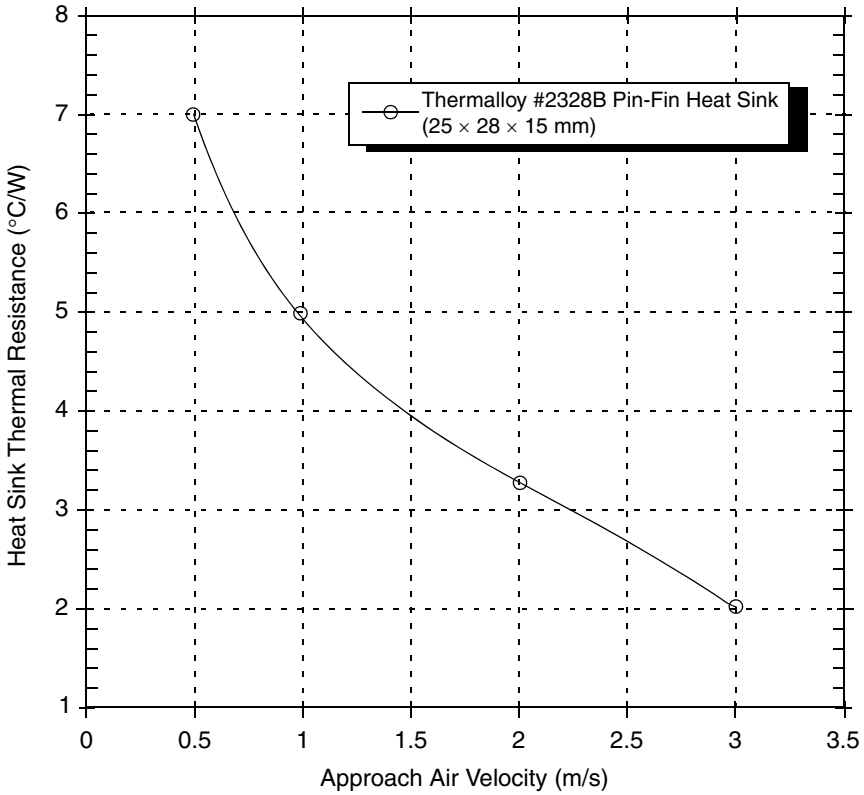


Figure 28. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs.

Table 19. Document Revision History (continued)

Revision	Date	Substantive Change(s)
4	—	Added 450 MHz speed bin.
		Changed Table 16 to show 450 MHz part in example.
		Added row for 433 and 450 MHz core frequencies to Table 17.
		In Section 1.8.8, revised the heat sink vendor list.
		In Section 1.8.8.2, revised the interface vendor list.
3	—	Updated format and thermal resistance specifications of Table 4.
		Reformatted Tables 9, 10, 11, and 12.
		Added dimensions A3, D1, and E1 to Figures 18, 19, and 20.
		Revised Section 1.8.7 and Figure 25, removed Figure 26 and Table 19 (information now included in Figure 25).
		Reformatted Section 1.10.
		Clarified address bus and address attribute pull-up recommendations in Section 1.8.7.
		Clarified Table 2.
		Updated voltage sequencing requirements in Table 1 and removed Section 1.8.3.
2	—	1.8 V/2.0 V mode no longer supported; added 2.5 V support.
		Removed 1.8 V/2.0 V mode data from Tables 2, 3, and 6.
		Added 2.5 V mode data to Tables 2, 3, and 6.
		Extended recommended operating voltage (down to 1.8 V) for V_{DD}, AV_{DD}, and $L2AV_{DD}$ for 300 and 350 MHz parts in Table 3.
		Updated Table 7 and test conditions for power consumption specifications.
		Corrected Note 6 of Table 9 to include $\overline{\text{TLBISYNC}}$ as a mode-select signal.
		Updated AC timing specifications in Table 10.
		Updated AC timing specifications in Table 12.
		Corrected AC timing specifications in Table 13.
		Added L1_TSTCLK, L2_TSTCLK, and $\overline{\text{LSSD\_MODE}}$ pull-up requirements to Section 1.8.6.
		Corrected Figure 22.

10 Ordering Information

Ordering information for the devices fully covered by this specification document is provided in Section 10.1, “Part Numbers Fully Addressed by This Document.” Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number. Section 10.2, “Part Numbers Not Fully Addressed by This Document,” lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specifications addendum.

10.1 Part Numbers Fully Addressed by This Document

Table 20 provides the Freescale part numbering nomenclature for the MPC755 and MPC745 devices fully addressed by this document.

Table 20. Part Numbering Nomenclature

MPC	*xxx*	*x*	*xx*	*nnn*	*x*	*x*
Product Code	**Part Identifier**	**Process Descriptor**	**Package [1]**	**Processor Frequency**	**Application Modifier**	**Revision Level**
XPC[2]	755 745	B = HiP4DP	PX = PBGA RX = CBGA	300 350	L: 2.0 V ± 100 mV 0° to 105°C	E: 2.8; PVR = 0008 3203
	755	C = HiP4DP		400		
MPC	755	B = HiP4DP		300 350		
		C = HiP4DP		350 400		
	745	B = HiP4DP	PX = PBGA	300 350		
	745	C = HiP4DP	PX = PBGA VT = PBGAPb-free BGA	350		
	755 745	B = HiP4DP	VT = PBGAPb-free BGA	300 350		
	755	C = HiP4DP		350 400		

Notes:

1. See Section 7, “Package Description,” for more information on available package types.
2. The X prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These are from a limited production volume of prototypes manufactured, tested, and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes

10.2 Part Numbers Not Fully Addressed by This Document

Devices not fully addressed in this document are described in separate hardware specification addendums which supplement and supersede this document, as described in the following tables.

Table 21. Part Numbers Addressed by XPC755B*xxnnn*T*x* Series Part Numbers (Document No. MPC755ECSO1AD)

XPC	755	B	*xx*	*nnn*	T	*x*

Product Code	Part Identifier	Process Descriptor	Package	Processor Frequency	Application Modifier	Revision Level
XPC	755	B = HiP4DP	RX = CBGA	350 400	T: 2.0 V ± 100 mV –40° to 105°C	D: 2.7; PVR = 0008 3203 E: 2.8; PVR = 0008 3203
MPC	755	C=HiP4DP	RX = CBGA	350	T: 2.0 V ± 100 mV –40° to 105°C	E: 2.8; PVR = 0008 3203

Table 22. Part Numbers Addressed by XPC755B*xxnnn*LD Series Part Numbers (Document No. MPC755ECSO2AD)

XPC	*xxx*	B	*xx*	*nnn*	L	D

Product Code	Part Identifier	Process Descriptor	Package	Processor Frequency	Application Modifier	Revision Level
XPC	755 745	B = HiP4DP	PX = PBGA RX = CBGA	300 350 400	L: 2.0 V ± 100 mV 0° to 105°C	D: 2.7; PVR = 0008 3203

Table 23. Part Numbers Addressed by XPC755*xxxnnn*LE Series Part Numbers (Document No. MPC755ECSO3AD)

XPC	755	*x*	*xx*	*nnn*	L	E

Product Code	Part Identifier	Process Descriptor	Package	Processor Frequency	Application Modifier	Revision Level
XPC	755	B = HiP4DP	RX = CBGA	400	L: 2.0 V ± 100 mV 0° to 105°C	E: 2.8; PVR = 0008 3203
			PX = PBGA			
		C = HiP4DP	RX = CBGA	450		