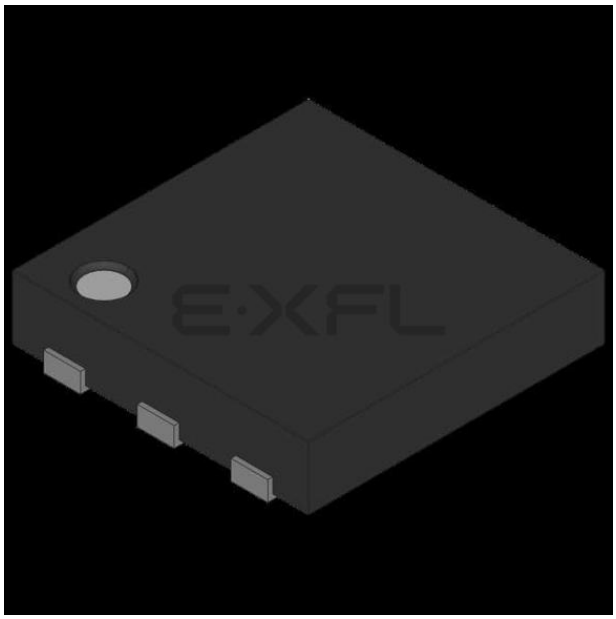

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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	350MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-CBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc755brx350te

  - Selectable interface voltages of 2.5 and 3.3 V
  - Parity checking on both L2 address and data
- Memory management unit
  - 128-entry, two-way set-associative instruction TLB
  - 128-entry, two-way set-associative data TLB
  - Hardware reload for TLBs
  - Hardware or optional software tablewalk support
  - Eight instruction BATs and eight data BATs
  - Eight SPRGs, for assistance with software tablewalks
  - Virtual memory support for up to 4 exabytes (2^{52}) of virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
- Bus interface
  - Compatible with 60x processor interface
  - 32-bit address bus
  - 64-bit data bus, 32-bit mode selectable
  - Bus-to-core frequency multipliers of 2x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 10x supported
  - Selectable interface voltages of 2.5 and 3.3 V
  - Parity checking on both address and data buses
- Power management
  - Low-power design with thermal requirements very similar to MPC740/MPC750
  - Three static power saving modes: doze, nap, and sleep
  - Dynamic power management
- Integrated thermal management assist unit
  - On-chip thermal sensor and control logic
  - Thermal management interrupt for software regulation of junction temperature
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface

3 General Parameters

The following list provides a summary of the general parameters of the MPC755:

Technology	0.22 µm CMOS, six-layer metal
Die size	6.61 mm × 7.73 mm (51 mm^2)
Transistor count	6.75 million
Logic design	Fully-static

Figure 2 shows the allowable undershoot and overshoot voltage on the MPC755.

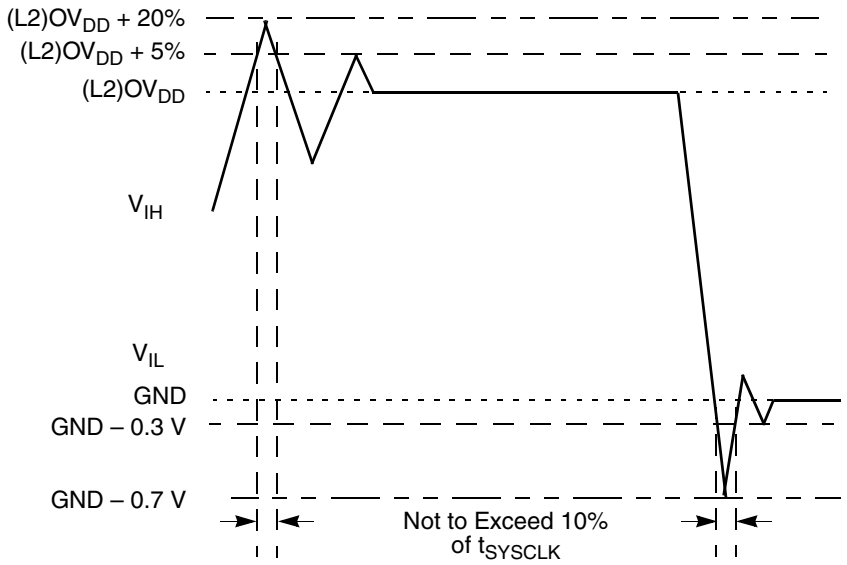


Figure 2. Overshoot/Undershoot Voltage

The MPC755 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC755 core voltage must always be provided at nominal 2.0 V (see Table 3 for actual recommended core voltage). Voltage to the L2 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 2. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL during operation. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

Table 2 describes the input threshold voltage setting.

Table 2. Input Threshold Voltage Setting

Part Revision	BVSEL Signal	Processor Bus Interface Voltage	L2VSEL Signal	L2 Bus Interface Voltage
E	0	Not Available	0	Not Available
	1	2.5 V/3.3 V	1	2.5 V/3.3 V

Caution: The input threshold selection must agree with the OV_{DD}/$L2OV_{DD}$ voltages supplied.

Note: The input threshold settings above are different for all revisions prior to Rev. 2.8 (Rev. E). For more information, refer to Section 10.2, "Part Numbers Not Fully Addressed by This Document."

Table 11. L2CLK Output AC Timing Specification

At recommended operating conditions (see Table 3)

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
L2CLK frequency	f_{L2CLK}	80	450	MHz	1, 4
L2CLK cycle time	t_{L2CLK}	2.5	12.5	ns	
L2CLK duty cycle	t_{CHCL}/t_{L2CLK}	45	55	%	2, 7
Internal DLL-relock time		640	—	L2CLK	3, 7
DLL capture window		0	10	ns	5, 7
L2CLK_OUT output-to-output skew	t_{L2CSKW}	—	50	ps	6, 7
L2CLK_OUT output jitter		—	±150	ps	6, 7

Notes:

1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB, L2CLK_OUT, and L2SYNC_OUT pins. The L2CLK frequency-to-core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. The maximum L2LCK frequency will be system dependent. L2CLK_OUTA and L2CLK_OUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The DLL-relock time is specified in terms of L2CLK periods. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in ns. Relock timing is guaranteed by design and characterization.
4. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz. This adds more delay to each tap of the DLL.
5. Allowable skew between L2SYNC_OUT and L2SYNC_IN.
6. This output jitter number represents the maximum delay of one tap forward or one tap back from the current DLL tap as the phase comparator seeks to minimize the phase difference between L2SYNC_IN and the internal L2CLK. This number must be comprehended in the L2 timing analysis. The input jitter on SYSCLK affects L2CLK_OUT and the L2 address/data/control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L2 timing analysis.
7. Guaranteed by design.

Figure 9 shows the L2 bus output timing diagrams for the MPC755.

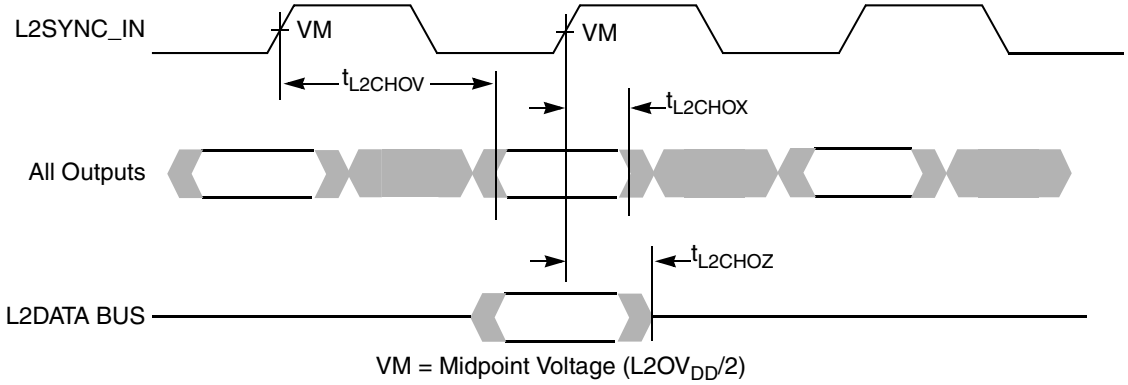


Figure 9. L2 Bus Output Timing Diagrams

Figure 10 provides the AC test load for L2 interface of the MPC755.

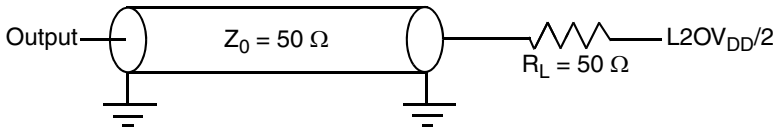


Figure 10. AC Test Load for the L2 Interface

4.2.5 IEEE 1149.1 AC Timing Specifications

Table 13 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 12 through Figure 15.

Table 13. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions (see Table 3)

Parameter		Symbol	Min	Max	Unit	Notes
TCK frequency of operation		f_{TCLK}	0	16	MHz	
TCK cycle time		t_{TCLK}	62.5	—	ns	
TCK clock pulse width measured at 1.4 V		t_{JHJL}	31	—	ns	
TCK rise and fall times		t_{JR}, t_{JF}	0	2	ns	
$\overline{\text{TRST}}$ assert time		t_{TRST}	25	—	ns	2
Input setup times:	Boundary-scan data TMS, TDI	t_{DVJH} t_{IVJH}	4 0	— —	ns	3
Input hold times:	Boundary-scan data TMS, TDI	t_{DXJH} t_{IXJH}	15 12	— —	ns	3
Valid times:	Boundary-scan data TDO	t_{JLDV} t_{JLOV}	— —	4 4	ns	4
Output hold times:	Boundary-scan data TDO	t_{JLDH} t_{JLOH}	25 12	— —	ns	4
TCK to output high impedance:	Boundary-scan data TDO	t_{JLDZ} t_{JLOZ}	3 3	19 9	ns	4, 5

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 11). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal which must be asserted for this minimum time to be recognized.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 11 provides the AC test load for TDO and the boundary-scan outputs of the MPC755.

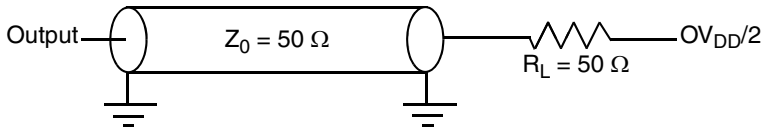


Figure 11. AC Test Load for the JTAG Interface

Figure 15 provides the test access port timing diagram.

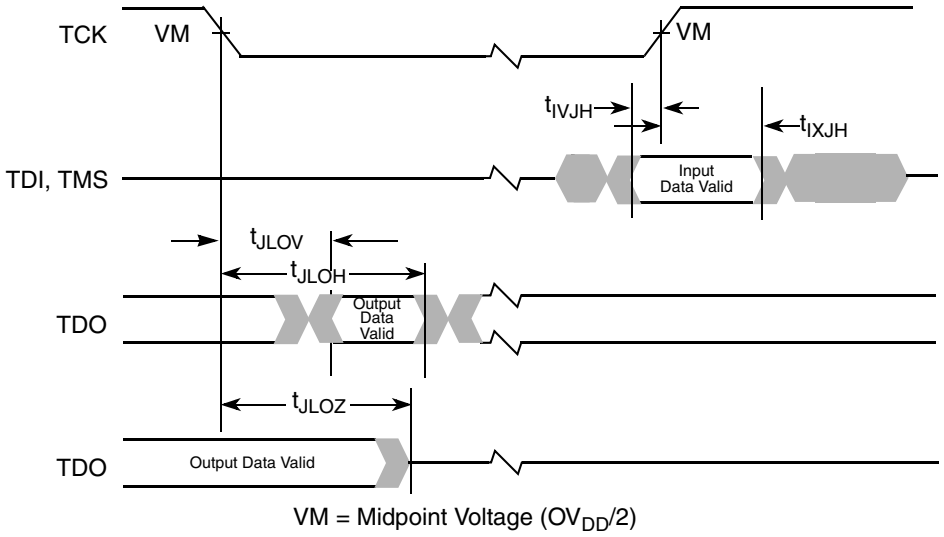
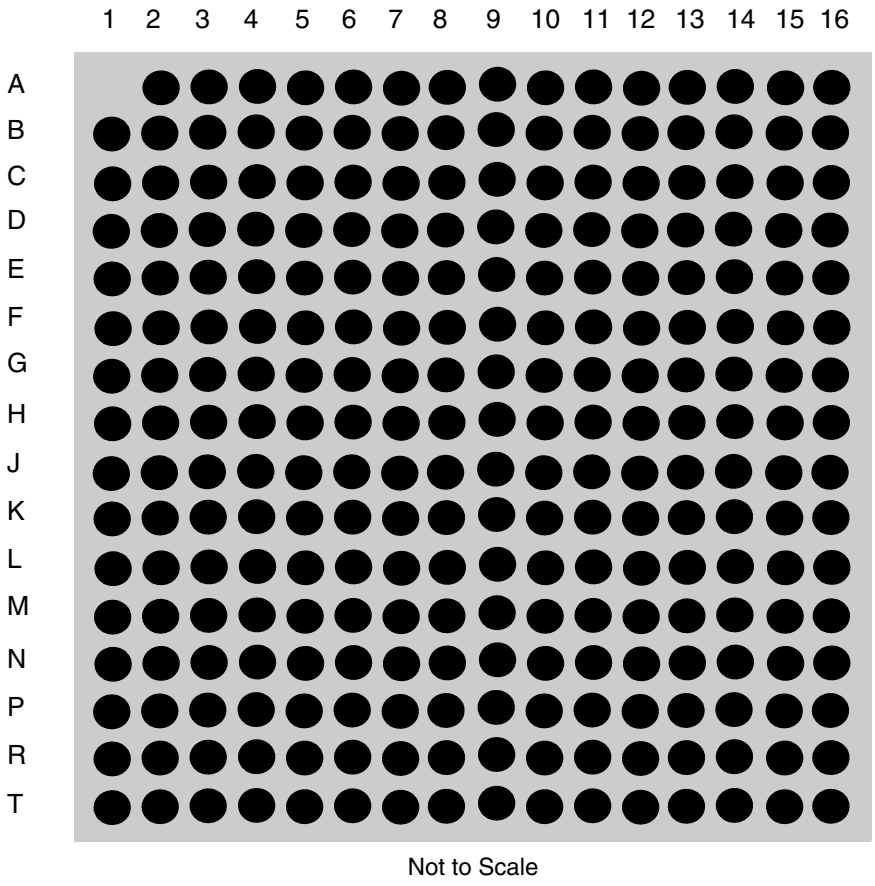


Figure 15. Test Access Port Timing Diagram

5 Pin Assignments

Figure 16 (in Part A) shows the pinout of the MPC745, 255 PBGA package as viewed from the top surface. Part B shows the side profile of the PBGA package to indicate the direction of the top surface view.

Part A



Part B

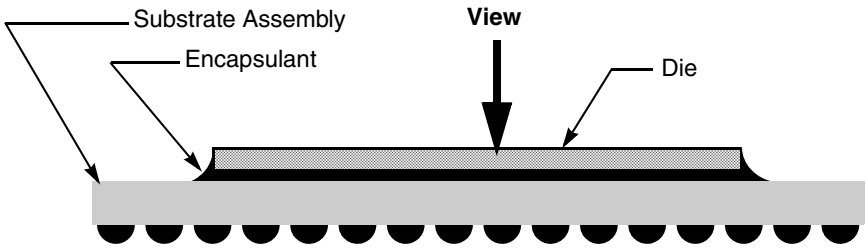
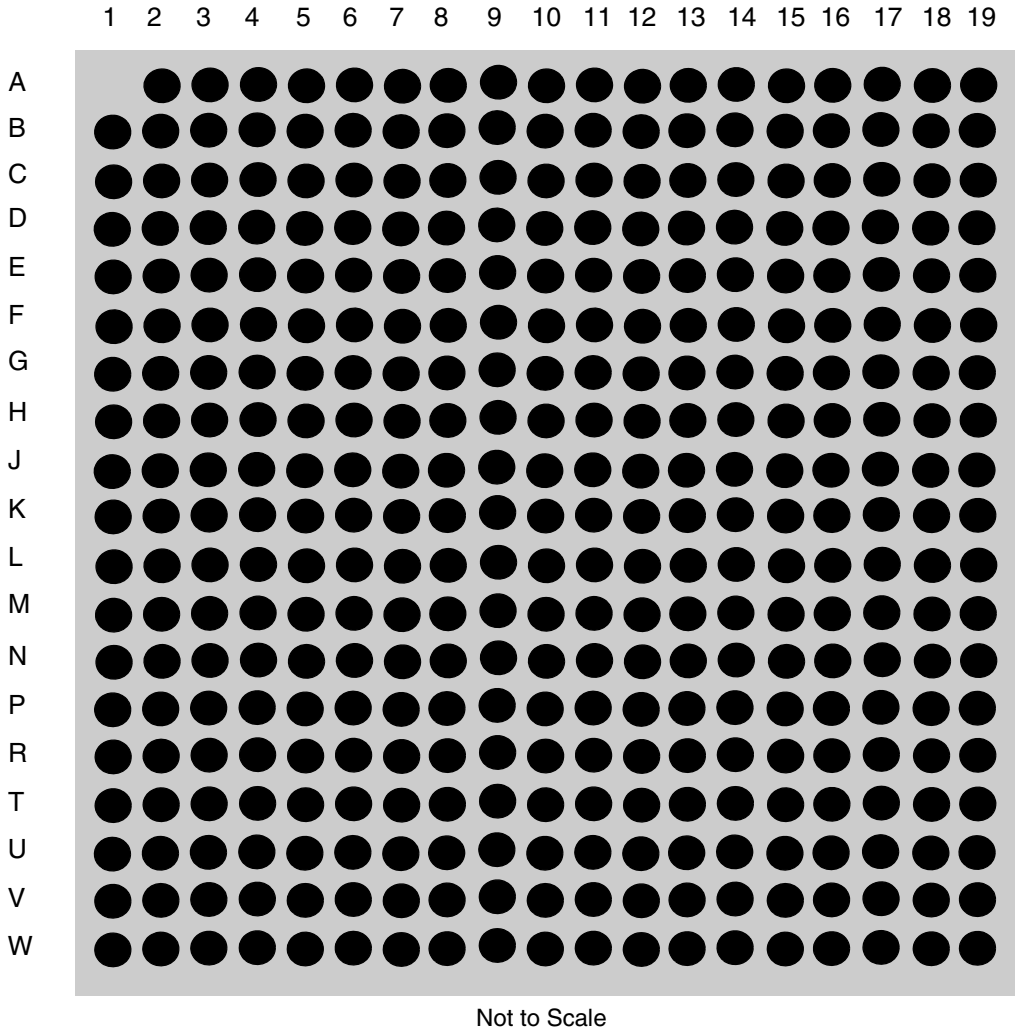


Figure 16. Pinout of the MPC745, 255 PBGA Package as Viewed from the Top Surface

Figure 17 (in Part A) shows the pinout of the MPC755, 360 PBGA and 360 CBGA packages as viewed from the top surface. Part B shows the side profile of the PBGA and CBGA package to indicate the direction of the top surface view.

Part A



Part B

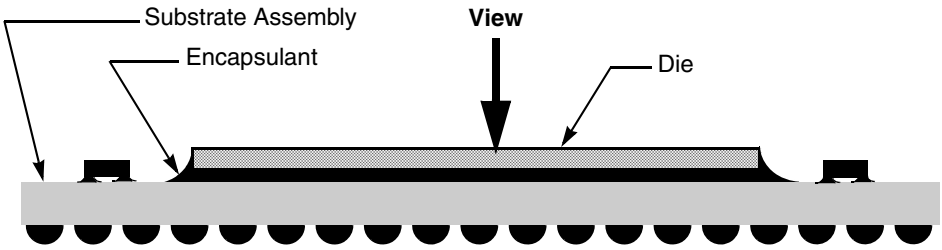


Figure 17. Pinout of the MPC755, 360 PBGA and CBGA Packages as Viewed from the Top Surface

6 Pinout Listings

Table 14 provides the pinout listing for the MPC745, 255 PBGA package.

Table 14. Pinout Listing for the MPC745, 255 PBGA Package

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
A[0:31]	C16, E4, D13, F2, D14, G1, D15, E2, D16, D4, E13, G2, E15, H1, E16, H2, F13, J1, F14, J2, F15, H3, F16, F4, G13, K1, G15, K2, H16, M1, J15, P1	High	I/O	OV_{DD}	
$\overline{\text{AACK}}$	L2	Low	Input	OV_{DD}	
$\overline{\text{ABB}}$	K4	Low	I/O	OV_{DD}	
AP[0:3]	C1, B4, B3, B2	High	I/O	OV_{DD}	
$\overline{\text{ARTRY}}$	J4	Low	I/O	OV_{DD}	
AV_{DD}	A10	—	—	2.0 V	
$\overline{\text{BG}}$	L1	Low	Input	OV_{DD}	
$\overline{\text{BR}}$	B6	Low	Output	OV_{DD}	
BVSEL	B1	High	Input	OV_{DD}	3, 4, 5
$\overline{\text{CI}}$	E1	Low	Output	OV_{DD}	
$\overline{\text{CKSTP\_IN}}$	D8	Low	Input	OV_{DD}	
$\overline{\text{CKSTP\_OUT}}$	A6	Low	Output	OV_{DD}	
CLK_OUT	D7	—	Output	OV_{DD}	
$\overline{\text{DBB}}$	J14	Low	I/O	OV_{DD}	
$\overline{\text{DBG}}$	N1	Low	Input	OV_{DD}	
$\overline{\text{DBDIS}}$	H15	Low	Input	OV_{DD}	
$\overline{\text{DBWO}}$	G4	Low	Input	OV_{DD}	
DH[0:31]	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P9, N9, T10, R9, T9, P8, N8, R8, T8, N7, R7, T7, P6, N6, R6, T6, R5, N5, T5, T4	High	I/O	OV_{DD}	
DL[0:31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P3, N3, N4, R3, T1, T2, P4, T3, R4	High	I/O	OV_{DD}	
DP[0:7]	M2, L3, N2, L4, R1, P2, M4, R2	High	I/O	OV_{DD}	
$\overline{\text{DRTRY}}$	G16	Low	Input	OV_{DD}	
$\overline{\text{GBL}}$	F1	Low	I/O	OV_{DD}	
GND	C5, C12, E3, E6, E8, E9, E11, E14, F5, F7, F10, F12, G6, G8, G9, G11, H5, H7, H10, H12, J5, J7, J10, J12, K6, K8, K9, K11, L5, L7, L10, L12, M3, M6, M8, M9, M11, M14, P5, P12	—	—	GND	
$\overline{\text{HRESET}}$	A7	Low	Input	OV_{DD}	

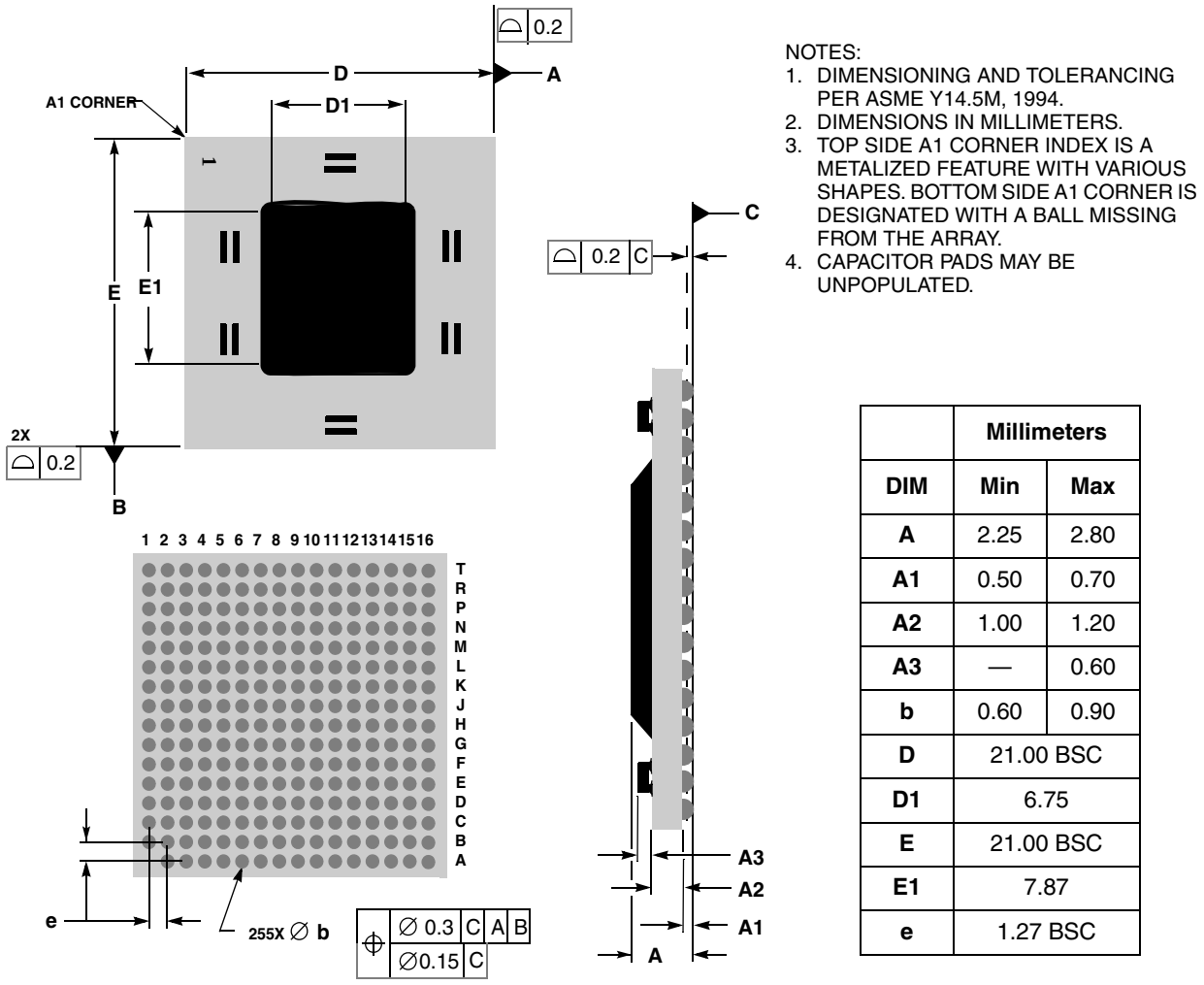
7.1 Package Parameters for the MPC745 PBGA

The package parameters are as provided in the following list. The package type is 21 × 21 mm, 255-lead plastic ball grid array (PBGA).

Package outline	21 × 21 mm
Interconnects	255 (16 × 16 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.25 mm
Maximum module height	2.80 mm
Ball diameter (typical)	0.75 mm (29.5 mil)

7.2 Mechanical Dimensions for the MPC745 PBGA

Figure 18 provides the mechanical dimensions and bottom surface nomenclature for the MPC745, 255 PBGA package.



	Millimeters	
DIM	Min	Max
A	2.25	2.80
A1	0.50	0.70
A2	1.00	1.20
A3	—	0.60
b	0.60	0.90
D	21.00 BSC	
D1	6.75	
E	21.00 BSC	
E1	7.87	
e	1.27 BSC	

Figure 18. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC745, 255 PBGA Package

8 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC755.

8.1 PLL Configuration

The MPC755 PLL is configured by the PLL_CFG[0:3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. These must be chosen such that they comply with Table 8. Table 16 shows the valid configurations of these signals and an example illustrating the core and VCO frequencies resulting from various PLL configurations and example bus frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the 400-MHz column in Table 8.

Table 16. MPC755 Microprocessor PLL Configuration Example for 400 MHz Parts

PLL_CFG [0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus 33 MHz	Bus 50 MHz	Bus 66 MHz	Bus 75 MHz	Bus 80 MHz	Bus 100 MHz
0100	2x	2x	—	—	—	—	—	200 (400)
1000	3x	2x	—	—	200 (400)	225 (450)	240 (480)	300 (600)
1110	3.5x	2x	—	—	233 (466)	263 (525)	280 (560)	350 (700)
1010	4x	2x	—	200 (400)	266 (533)	300 (600)	320 (640)	400 (800)
0111	4.5x	2x	—	225 (450)	300 (600)	338 (675)	360 (720)	—
1011	5x	2x	—	250 (500)	333 (666)	375 (750)	400 (800)	—
1001	5.5x	2x	—	275 (550)	366 (733)	—	—	—
1101	6x	2x	200 (400)	300 (600)	400 (800)	—	—	—
0101	6.5x	2x	216 (433)	325 (650)	—	—	—	—
0010	7x	2x	233 (466)	350 (700)	—	—	—	—
0001	7.5x	2x	250 (500)	375 (750)	—	—	—	—
1100	8x	2x	266 (533)	400 (800)	—	—	—	—
0110	10x	2x	333 (666)	—	—	—	—	—

Table 16. MPC755 Microprocessor PLL Configuration Example for 400 MHz Parts (continued)

PLL_CFG [0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus 33 MHz	Bus 50 MHz	Bus 66 MHz	Bus 75 MHz	Bus 80 MHz	Bus 100 MHz
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied					
1111	PLL off		PLL off, no core clocking occurs					

Notes:

1. PLL_CFG[0:3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the MPC755; see Section 4.2.1, "Clock AC Specifications," for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL off mode, no clocking occurs inside the MPC755 regardless of the SYSCLK input.

The MPC755 generates the clock for the external L2 synchronous data SRAMs by dividing the core clock frequency of the MPC755. The divided-down clock is then phase-adjusted by an on-chip delay-lock-loop (DLL) circuit and should be routed from the MPC755 to the external RAMs. A separate clock output, L2SYNC_OUT is sent out half the distance to the SRAMs and then returned as an input to the DLL on pin L2SYNC_IN so that the rising-edge of the clock as seen at the external RAMs can be aligned to the clocking of the internal latches in the L2 bus interface.

The core-to-L2 frequency divisor for the L2 PLL is selected through the L2CLK bits of the L2CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the MPC755 core, and the phase adjustment range that the L2 DLL supports. Table 17 shows various example L2 clock frequencies that can be obtained for a given set of core frequencies. The minimum L2 frequency target is 80 MHz.

Table 17. Sample Core-to-L2 Frequencies

Core Frequency (MHz)	÷1	÷1.5	÷2	÷2.5	÷3
250	250	166	125	100	83
266	266	177	133	106	89
275	275	183	138	110	92
300	300	200	150	120	100
325	325	217	163	130	108
333	333	222	167	133	111
350	350	233	175	140	117
366	366	244	183	146	122

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603 orientations where connections are made along the length of the part.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, $L2OV_{DD}$, and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors:100–330 µF (AVX TPS tantalum or Sanyo OSCON).

8.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level through a resistor. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, $L2OV_{DD}$, and GND pins of the MPC755. Note that power must be supplied to $L2OV_{DD}$ even if the L2 interface of the MPC755 will not be used; it is recommended to connect $L2OV_{DD}$ to OV_{DD} and L2VSEL to BVSEL if the L2 interface is unused. (This requirement does not apply to the MPC745 since it has neither an L2 interface nor $L2OV_{DD}$ pins.)

8.5 Output Buffer DC Impedance

The MPC755 60x and L2 I/O drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to $(L2)OV_{DD}$ or GND. Then, the value of each resistor is varied until the pad voltage is $(L2)OV_{DD}/2$ (see Figure 22).

The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices.

Figure 22 describes the driver impedance measurement circuit described above.

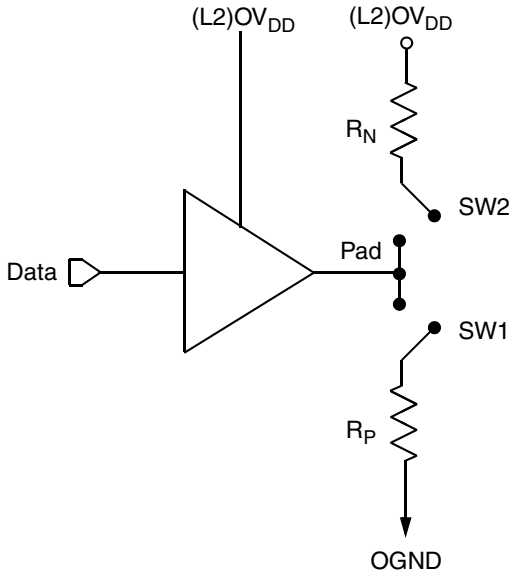


Figure 22. Driver Impedance Measurement Circuit

Alternately, the following is another method to determine the output impedance of the MPC755. A voltage source, V_{force}, is connected to the output of the MPC755 as shown in Figure 23. Data is held low, the voltage source is set to a value that is equal to (L2)OV_{DD}/2 and the current sourced by V_{force} is measured. The voltage drop across the pull-down device, which is equal to (L2)OV_{DD}/2, is divided by the measured current to determine the output impedance of the pull-down device, R_N. Similarly, the impedance of the pull-up device is determined by dividing the voltage drop of the pull-up, (L2)OV_{DD}/2, by the current sank by the pull-up when the data is high and V_{force} is equal to (L2)OV_{DD}/2. This method can be employed with either empirical data from a test setup or with data from simulation models, such as IBIS.

R_P and R_N are designed to be close to each other in value. Then $Z_0 = (R_P + R_N)/2$.

Figure 23 describes the alternate driver impedance measurement circuit.

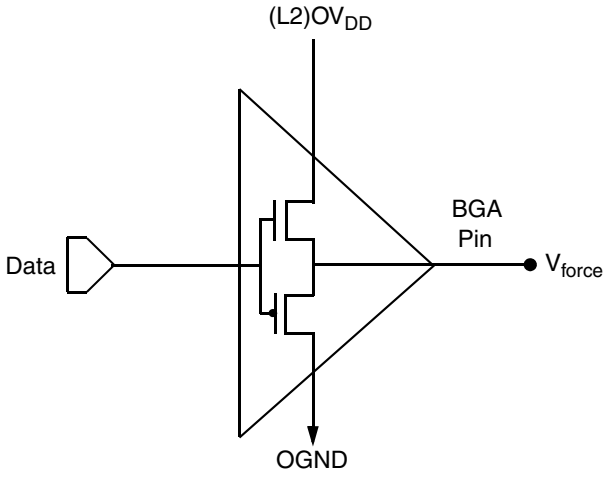


Figure 23. Alternate Driver Impedance Measurement Circuit

The board designer can choose between several types of heat sinks to place on the MPC755. There are several commercially-available heat sinks for the MPC755 provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

8.8.1 Internal Package Conduction Resistance

For the exposed-die packaging technology, shown in Table 4, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case (or top-of-die for exposed silicon) thermal resistance
- The die junction-to-ball thermal resistance

Figure 26 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.

Shin-Etsu MicroSi, Inc. 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

8.8.3 Heat Sink Selection Example

This section provides a heat sink selection example using one of the commercially-available heat sinks. For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) \times P_d$$

where:

T_j is the die-junction temperature
T_a is the inlet cabinet ambient temperature
T_r is the air temperature rise within the computer cabinet
θ_{jc} is the junction-to-case thermal resistance
θ_{int} is the adhesive or interface material thermal resistance
θ_{sa} is the heat sink base-to-ambient thermal resistance
P_d is the power dissipated by the device

During operation the die-junction temperatures (T_j) should be maintained less than the value specified in Table 3. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material (θ_{int}) is typically about 1°C/W. Assuming a T_a of 30°C, a T_r of 5°C, a CBGA package $R_{\theta jc} < 0.1$, and a power consumption (P_d) of 5.0 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 1.0°C/W + \theta_{sa}) \times 5.0\ W$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{sa}) versus airflow velocity is shown in Figure 28.

Assuming an air velocity of 0.5 m/s, we have an effective R_{sa} of 7°C/W, thus

$$T_j = 30°C + 5°C + (0.1°C/W + 1.0°C/W + 7°C/W) \times 5.0\ W,$$

resulting in a die-junction temperature of approximately 76°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, The Bergquist Company, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.

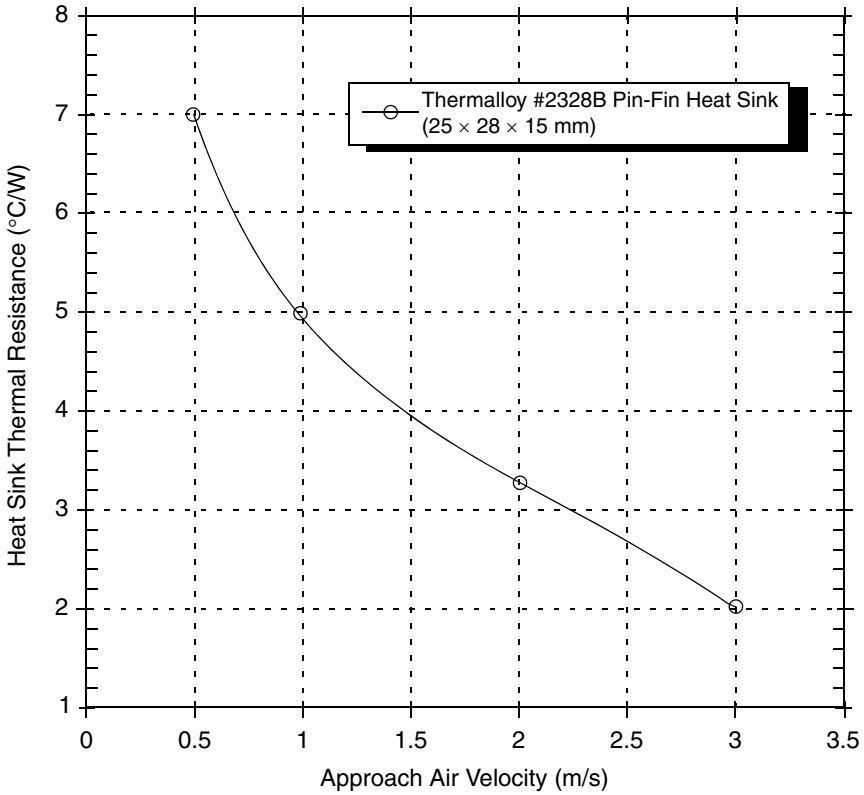


Figure 28. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs.

10 Ordering Information

Ordering information for the devices fully covered by this specification document is provided in Section 10.1, “Part Numbers Fully Addressed by This Document.” Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number. Section 10.2, “Part Numbers Not Fully Addressed by This Document,” lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specifications addendum.

10.1 Part Numbers Fully Addressed by This Document

Table 20 provides the Freescale part numbering nomenclature for the MPC755 and MPC745 devices fully addressed by this document.

Table 20. Part Numbering Nomenclature

MPC	*xxx*	*x*	*xx*	*nnn*	*x*	*x*
Product Code	**Part Identifier**	**Process Descriptor**	**Package [1]**	**Processor Frequency**	**Application Modifier**	**Revision Level**
XPC[2]	755 745	B = HiP4DP	PX = PBGA RX = CBGA	300 350	L: 2.0 V ± 100 mV 0° to 105°C	E: 2.8; PVR = 0008 3203
	755	C = HiP4DP		400		
MPC	755	B = HiP4DP		300 350		
		C = HiP4DP		350 400		
	745	B = HiP4DP	PX = PBGA	300 350		
	745	C = HiP4DP	PX = PBGA VT = PBGAPb-free BGA	350		
	755 745	B = HiP4DP	VT = PBGAPb-free BGA	300 350		
	755	C = HiP4DP		350 400		

Notes:

1. See Section 7, “Package Description,” for more information on available package types.
2. The X prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These are from a limited production volume of prototypes manufactured, tested, and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes

10.2 Part Numbers Not Fully Addressed by This Document

Devices not fully addressed in this document are described in separate hardware specification addendums which supplement and supersede this document, as described in the following tables.

Table 21. Part Numbers Addressed by XPC755B*xxnnn*T*x* Series Part Numbers (Document No. MPC755ECSO1AD)

XPC	755	B	*xx*	*nnn*	T	*x*

Product Code	Part Identifier	Process Descriptor	Package	Processor Frequency	Application Modifier	Revision Level
XPC	755	B = HiP4DP	RX = CBGA	350 400	T: 2.0 V ± 100 mV –40° to 105°C	D: 2.7; PVR = 0008 3203 E: 2.8; PVR = 0008 3203
MPC	755	C=HiP4DP	RX = CBGA	350	T: 2.0 V ± 100 mV –40° to 105°C	E: 2.8; PVR = 0008 3203

Table 22. Part Numbers Addressed by XPC755B*xxnnn*LD Series Part Numbers (Document No. MPC755ECSO2AD)

XPC	*xxx*	B	*xx*	*nnn*	L	D

Product Code	Part Identifier	Process Descriptor	Package	Processor Frequency	Application Modifier	Revision Level
XPC	755 745	B = HiP4DP	PX = PBGA RX = CBGA	300 350 400	L: 2.0 V ± 100 mV 0° to 105°C	D: 2.7; PVR = 0008 3203

Table 23. Part Numbers Addressed by XPC755*xxxnnn*LE Series Part Numbers (Document No. MPC755ECSO3AD)

XPC	755	*x*	*xx*	*nnn*	L	E

Product Code	Part Identifier	Process Descriptor	Package	Processor Frequency	Application Modifier	Revision Level
XPC	755	B = HiP4DP	RX = CBGA	400	L: 2.0 V ± 100 mV 0° to 105°C	E: 2.8; PVR = 0008 3203
			PX = PBGA			
		C = HiP4DP	RX = CBGA	450		

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