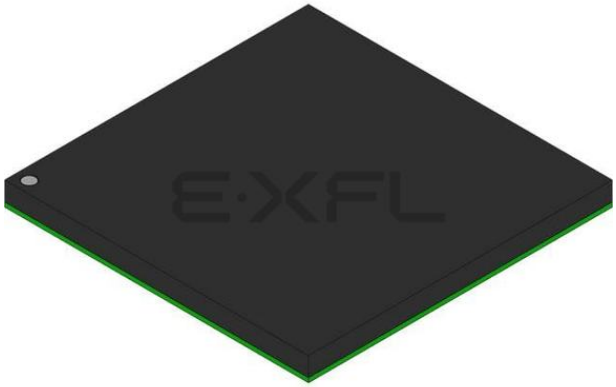

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	300MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BBGA, FCBGA
Supplier Device Package	360-FCPBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc755bvt300le

2 Features

This section summarizes features of the MPC755 implementation of the PowerPC architecture. Major features of the MPC755 are as follows:

- Branch processing unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving two speculations)
  - Up to one speculative stream in execution, one additional speculative stream in fetch
  - 512-entry branch history table (BHT) for dynamic prediction
  - 64-entry, four-way set-associative branch target instruction cache (BTIC) for eliminating branch delay slots
- Dispatch unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point)
  - Serialization control (predispatch, postdispatch, execution serialization)
- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - Six-entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization, and all instruction flow changes
- Fixed point units (FXUs) that share 32 GPRs for integer operands
  - Fixed Point Unit 1 (FXU1)—multiply, divide, shift, rotate, arithmetic, logical
  - Fixed Point Unit 2 (FXU2)—shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Floating-point unit and a 32-entry FPR file
  - Support for IEEE standard 754 single- and double-precision floating-point arithmetic
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Single-entry reservation station
  - Supports non-IEEE mode for time-critical operations
  - Three-cycle latency, one-cycle throughput, single-precision multiply-add

  - Selectable interface voltages of 2.5 and 3.3 V
  - Parity checking on both L2 address and data
- Memory management unit
  - 128-entry, two-way set-associative instruction TLB
  - 128-entry, two-way set-associative data TLB
  - Hardware reload for TLBs
  - Hardware or optional software tablewalk support
  - Eight instruction BATs and eight data BATs
  - Eight SPRGs, for assistance with software tablewalks
  - Virtual memory support for up to 4 exabytes (2^{52}) of virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
- Bus interface
  - Compatible with 60x processor interface
  - 32-bit address bus
  - 64-bit data bus, 32-bit mode selectable
  - Bus-to-core frequency multipliers of 2x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 10x supported
  - Selectable interface voltages of 2.5 and 3.3 V
  - Parity checking on both address and data buses
- Power management
  - Low-power design with thermal requirements very similar to MPC740/MPC750
  - Three static power saving modes: doze, nap, and sleep
  - Dynamic power management
- Integrated thermal management assist unit
  - On-chip thermal sensor and control logic
  - Thermal management interrupt for software regulation of junction temperature
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface

3 General Parameters

The following list provides a summary of the general parameters of the MPC755:

Technology	0.22 µm CMOS, six-layer metal
Die size	6.61 mm × 7.73 mm (51 mm^2)
Transistor count	6.75 million
Logic design	Fully-static

Packages	MPC745: Surface mount 255 plastic ball grid array (PBGA) MPC755: Surface mount 360 ceramic ball grid array (CBGA) Surface mount 360 plastic ball grid array (PBGA)
Core power supply	2.0 V ± 100 mV DC (nominal; some parts support core voltages down to 1.8 V; see Table 3 for recommended operating conditions)
I/O power supply	2.5 V ± 100 mV DC or 3.3 V ± 165 mV DC (input thresholds are configuration pin selectable)

4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC755.

4.1 DC Electrical Characteristics

Table 1 through Table 7 describe the MPC755 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Maximum Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 2.5	V	4
PLL supply voltage		AV_{DD}	–0.3 to 2.5	V	4
L2 DLL supply voltage		$L2AV_{DD}$	–0.3 to 2.5	V	4
Processor bus supply voltage		OV_{DD}	–0.3 to 3.6	V	3
L2 bus supply voltage		$L2OV_{DD}$	–0.3 to 3.6	V	3
Input voltage	Processor bus	V_{in}	–0.3 to OV_{DD} + 0.3 V	V	2, 5
	L2 bus	V_{in}	–0.3 to $L2OV_{DD}$ + 0.3 V	V	2, 5
	JTAG signals	V_{in}	–0.3 to 3.6	V	
Storage temperature range		T_{stg}	–55 to 150	°C	

Notes:

1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** V_{in} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.3 V at any time including during power-on reset.
3. **Caution:** $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 1.6 V during normal operation. During power-on reset and power-down sequences, $L2OV_{DD}/OV_{DD}$ may exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by up to 3.3 V for up to 20 ms, or by 2.5 V for up to 40 ms. Excursions beyond 3.3 V or 40 ms are not supported.
4. **Caution:** $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4 V during normal operation. During power-on reset and power-down sequences, $V_{DD}/AV_{DD}/L2AV_{DD}$ may exceed $L2OV_{DD}/OV_{DD}$ by up to 1.0 V for up to 20 ms, or by 0.7 V for up to 40 ms. Excursions beyond 1.0 V or 40 ms are not supported.
5. This is a DC specifications only. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

Table 3 provides the recommended operating conditions for the MPC755.

Table 3. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value				Unit	Notes
			300 MHz, 350 MHz		400 MHz			
			Min	Max	Min	Max		
Core supply voltage		V_{DD}	1.80	2.10	1.90	2.10	V	3
PLL supply voltage		AV_{DD}	1.80	2.10	1.90	2.10	V	3
L2 DLL supply voltage		$L2AV_{DD}$	1.80	2.10	1.90	2.10	V	3
Processor bus supply voltage	BVSEL = 1	OV_{DD}	2.375	2.625	2.375	2.625	V	2, 4
			3.135	3.465	3.135	3.465		5
L2 bus supply voltage	L2VSEL = 1	$L2OV_{DD}$	2.375	2.625	2.375	2.625	V	2, 4
			3.135	3.465	3.135	3.465		5
Input voltage	Processor bus	V_{in}	GND	OV_{DD}	GND	OV_{DD}	V	
	L2 bus	V_{in}	GND	$L2OV_{DD}$	GND	$L2OV_{DD}$	V	
	JTAG signals	V_{in}	GND	OV_{DD}	GND	OV_{DD}	V	
Die-junction temperature		T_j	0	105	0	105	°C	

Notes:

1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. Revisions prior to Rev. 2.8 (Rev. E) offered different I/O voltage support. For more information, refer to Section 10.2, “Part Numbers Not Fully Addressed by This Document.”
3. 2.0 V nominal.
4. 2.5 V nominal.
5. 3.3 V nominal.

Table 4 provides the package thermal characteristics for the MPC755 and MPC745. The MPC755 was initially sampled in a CBGA package, but production units are currently provided in both a CBGA and a PBGA package. Because of the better long-term device-to-board interconnect reliability of the PBGA package, Freescale recommends use of a PBGA package except where circumstances dictate use of a CBGA package. The MPC745 is offered in a PBGA package only.

Table 6. DC Electrical Specifications (continued)

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage [1]	Symbol	Min	Max	Unit	Notes
Capacitance, V_{in} = 0 V, f = 1 MHz		C_{in}	—	5.0	pF	3, 4

Notes:

1. Nominal voltages; see Table 3 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD} while $L2OV_{DD}$ is the reference for the L2 bus signals.
3. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK) and IEEE 1149.1 boundary scan (JTAG) signals.
4. Capacitance is periodically sampled rather than 100% tested.
5. The leakage is measured for nominal OV_{DD} and V_{DD}, or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or –5%).

Table 7 provides the power consumption for the MPC755.

Table 7. Power Consumption for MPC755

	Processor (CPU) Frequency			Unit	Notes
	300 MHz	350 MHz	400 MHz		
Full-Power Mode					
Typical	3.1	3.6	5.4	W	1, 3, 4
Maximum	4.5	6.0	8.0	W	1, 2
Doze Mode					
Maximum	1.8	2.0	2.3	W	1, 2, 4
Nap Mode					
Maximum	1.0	1.0	1.0	W	1, 2, 4
Sleep Mode					
Maximum	550	550	550	mW	1, 2, 4
Sleep Mode (PLL and DLL Disabled)					
Maximum	510	510	510	mW	1, 2

Notes:

1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O supply power (OV_{DD} and $L2OV_{DD}$) or PLL/DLL supply power (AV_{DD} and $L2AV_{DD}$). OV_{DD} and $L2OV_{DD}$ power is system dependent, but is typically <10% of V_{DD} power. Worst case power consumption for AV_{DD} = 15 mW and $L2AV_{DD}$ = 15 mW.
2. Maximum power is measured at nominal V_{DD} (see Table 3) while running an entirely cache-resident, contrived sequence of instructions which keep the execution units maximally busy.
3. Typical power is an average value measured at the nominal recommended V_{DD} (see Table 3) and 65°C in a system while running a typical code sequence.
4. Not 100% tested. Characterized and periodically sampled.

4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC755. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section 4.2.1, "Clock AC Specifications," and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:3] signals. Parts are sold by maximum processor core frequency; see Section 10, "Ordering Information."

4.2.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications as defined in Figure 3.

Table 8. Clock AC Timing Specifications

At recommended operating conditions (see Table 3)

Characteristic	Symbol	Maximum Processor Core Frequency						Unit	Notes
		300 MHz		350 MHz		400 MHz			
		Min	Max	Min	Max	Min	Max		
Processor frequency	f_{core}	200	300	200	350	200	400	MHz	1
VCO frequency	f_{VCO}	400	600	400	700	400	800	MHz	1
SYSCLK frequency	f_{SYSCLK}	25	100	25	100	25	100	MHz	1
SYSCLK cycle time	t_{SYSCLK}	10	40	10	40	10	40	ns	
SYSCLK rise and fall time	t_{KR}, t_{KF}	—	2.0	—	2.0	—	2.0	ns	2
	t_{KR}, t_{KF}	—	1.4	—	1.4	—	1.4	ns	2
SYSCLK duty cycle measured at $OV_{DD}/2$	t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	%	3
SYSCLK jitter		—	±150	—	±150	—	±150	ps	3, 4
Internal PLL relock time		—	100	—	100	—	100	μs	3, 5

Notes:

1. **Caution:** The SYSCLK frequency and PLL_CFG[0:3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:3] signal description in Section 8.1, "PLL Configuration," for valid PLL_CFG[0:3] settings.
2. Rise and fall times measurements are now specified in terms of slew rates, rather than time to account for selectable I/O bus interface levels. The minimum slew rate of 1 V/ns is equivalent to a 2 ns maximum rise/fall time measured at 0.4 and 2.4 V (OV_{DD} = 3.3 V) or a rise/fall time of 1 ns measured at 0.4 and 1.8 V (OV_{DD} = 2.5 V).
3. Timing is guaranteed by design and characterization.
4. This represents total input jitter—short term and long term combined—and is guaranteed by design.
5. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 4 provides the mode select input timing diagram for the MPC755.

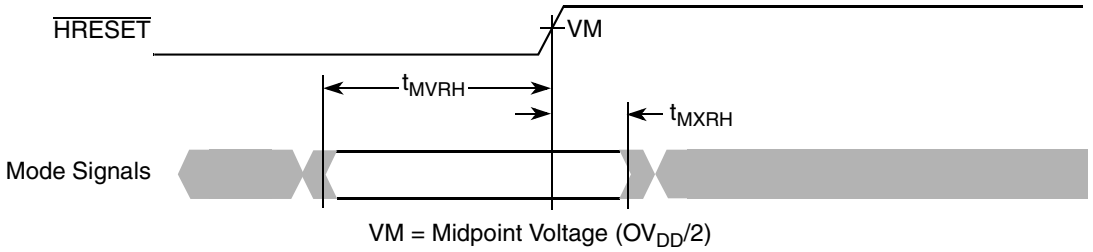


Figure 4. Mode Input Timing Diagram

Figure 5 provides the AC test load for the MPC755.

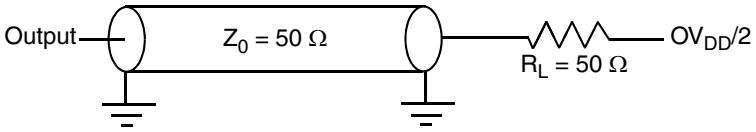


Figure 5. AC Test Load

SRAM. Note that revisions of the MPC755 prior to Rev. 2.8 (Rev. E) were limited in performance, and were typically limited to 175 MHz with similarly-rated SRAM. For more information, see Section 10.2, “Part Numbers Not Fully Addressed by This Document.”

Freescale is similarly limited by system constraints and cannot perform tests of the L2 interface on a socketed part on a functional tester at the maximum frequencies of Table 11. Therefore, functional operation and AC timing information are tested at core-to-L2 divisors of 2 or greater. Functionality of core-to-L2 divisors of 1 or 1.5 is verified at less than maximum rated frequencies.

L2 input and output signals are latched or enabled, respectively, by the internal L2CLK (which is SYSCLK multiplied up to the core frequency and divided down to the L2CLK frequency). In other words, the AC timings of Table 12 and Table 13 are entirely independent of L2SYNC_IN. In a closed loop system, where L2SYNC_IN is driven through the board trace by L2SYNC_OUT, L2SYNC_IN only controls the output phase of L2CLK_OUTA and L2CLK_OUTB which are used to latch or enable data at the SRAMs. However, since in a closed loop system L2SYNC_IN is held in phase alignment with the internal L2CLK, the signals of Table 12 and Table 13 are referenced to this signal rather than the not-externally-visible internal L2CLK. During manufacturing test, these times are actually measured relative to SYSCLK.

The L2SYNC_OUT signal is intended to be routed halfway out to the SRAMs and then returned to the L2SYNC_IN input of the MPC755 to synchronize L2CLK_OUT at the SRAM with the processor’s internal clock. L2CLK_OUT at the SRAM can be offset forward or backward in time by shortening or lengthening the routing of L2SYNC_OUT to L2SYNC_IN. See Freescale Application Note AN1794/D, *Backside L2 Timing Analysis for PCB Design Engineers*.

The L2CLK_OUTA and L2CLK_OUTB signals should not have more than two loads.

The L2CLK_OUT timing diagram is shown in Figure 7.

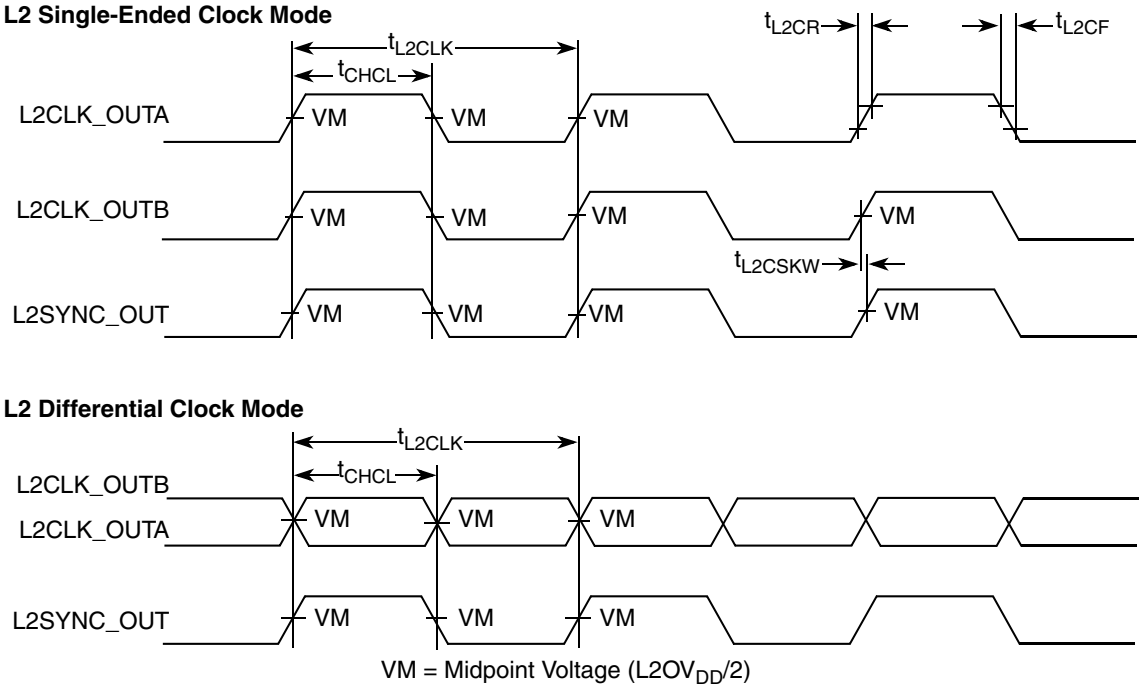


Figure 7. L2CLK_OUT Output Timing Diagram

4.2.4 L2 Bus AC Specifications

Table 12 provides the L2 bus interface AC timing specifications for the MPC755 as defined in Figure 8 and Figure 9 for the loading conditions described in Figure 10.

Table 12. L2 Bus Interface AC Timing Specifications

At recommended operating conditions (see Table 3)

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
L2SYNC_IN rise and fall time	t_{L2CR}, t_{L2CF}	—	1.0	ns	1
Setup times: Data and parity	t_{DVL2CH}	1.2	—	ns	2
Input hold times: Data and parity	t_{DXL2CH}	0	—	ns	2
Valid times: All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	t_{L2CHOV}	 — — — —	 3.1 3.2 3.3 3.7	ns	3, 4
Output hold times: All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	t_{L2CHOX}	 0.5 0.7 0.9 1.1	 — — — —	ns	3

6 Pinout Listings

Table 14 provides the pinout listing for the MPC745, 255 PBGA package.

Table 14. Pinout Listing for the MPC745, 255 PBGA Package

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
A[0:31]	C16, E4, D13, F2, D14, G1, D15, E2, D16, D4, E13, G2, E15, H1, E16, H2, F13, J1, F14, J2, F15, H3, F16, F4, G13, K1, G15, K2, H16, M1, J15, P1	High	I/O	OV_{DD}	
$\overline{\text{AACK}}$	L2	Low	Input	OV_{DD}	
$\overline{\text{ABB}}$	K4	Low	I/O	OV_{DD}	
AP[0:3]	C1, B4, B3, B2	High	I/O	OV_{DD}	
$\overline{\text{ARTRY}}$	J4	Low	I/O	OV_{DD}	
AV_{DD}	A10	—	—	2.0 V	
$\overline{\text{BG}}$	L1	Low	Input	OV_{DD}	
$\overline{\text{BR}}$	B6	Low	Output	OV_{DD}	
BVSEL	B1	High	Input	OV_{DD}	3, 4, 5
$\overline{\text{CI}}$	E1	Low	Output	OV_{DD}	
$\overline{\text{CKSTP\_IN}}$	D8	Low	Input	OV_{DD}	
$\overline{\text{CKSTP\_OUT}}$	A6	Low	Output	OV_{DD}	
CLK_OUT	D7	—	Output	OV_{DD}	
$\overline{\text{DBB}}$	J14	Low	I/O	OV_{DD}	
$\overline{\text{DBG}}$	N1	Low	Input	OV_{DD}	
$\overline{\text{DBDIS}}$	H15	Low	Input	OV_{DD}	
$\overline{\text{DBWO}}$	G4	Low	Input	OV_{DD}	
DH[0:31]	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P9, N9, T10, R9, T9, P8, N8, R8, T8, N7, R7, T7, P6, N6, R6, T6, R5, N5, T5, T4	High	I/O	OV_{DD}	
DL[0:31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P3, N3, N4, R3, T1, T2, P4, T3, R4	High	I/O	OV_{DD}	
DP[0:7]	M2, L3, N2, L4, R1, P2, M4, R2	High	I/O	OV_{DD}	
$\overline{\text{DRTRY}}$	G16	Low	Input	OV_{DD}	
$\overline{\text{GBL}}$	F1	Low	I/O	OV_{DD}	
GND	C5, C12, E3, E6, E8, E9, E11, E14, F5, F7, F10, F12, G6, G8, G9, G11, H5, H7, H10, H12, J5, J7, J10, J12, K6, K8, K9, K11, L5, L7, L10, L12, M3, M6, M8, M9, M11, M14, P5, P12	—	—	GND	
$\overline{\text{HRESET}}$	A7	Low	Input	OV_{DD}	

Table 14. Pinout Listing for the MPC745, 255 PBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
VOLTDET	F3	High	Output	—	6

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals; and V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL pin configuration of Table 2 and the voltage supplied. For actual recommended value of V_{in} or supply voltages, see Table 3.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. This pin must be pulled up to OV_{DD} for proper operation of the processor interface. To allow for future I/O voltage changes, provide the option to connect BVSEL independently to either OV_{DD} or GND.
4. Uses 1 of 15 existing no connects in the MPC740, 255 BGA package.
5. Internal pull-up on die.
6. Internally tied to GND in the MPC745, 255 BGA package to indicate to the power supply that a low-voltage processor is present. This signal is not a power supply input.

   Caution: This differs from the MPC755, 360 BGA package.

Table 15 provides the pinout listing for the MPC755, 360 PBGA and CBGA packages.

Table 15. Pinout Listing for the MPC755, 360 BGA Package

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
A[0:31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O	OV_{DD}	
$\overline{\text{AACK}}$	N3	Low	Input	OV_{DD}	
$\overline{\text{ABB}}$	L7	Low	I/O	OV_{DD}	
AP[0:3]	C4, C5, C6, C7	High	I/O	OV_{DD}	
$\overline{\text{ARTRY}}$	L6	Low	I/O	OV_{DD}	
AV_{DD}	A8	—	—	2.0 V	
$\overline{\text{BG}}$	H1	Low	Input	OV_{DD}	
$\overline{\text{BR}}$	E7	Low	Output	OV_{DD}	
BVSEL	W1	High	Input	OV_{DD}	3, 5, 6
$\overline{\text{CI}}$	C2	Low	Output	OV_{DD}	
$\overline{\text{CKSTP\_IN}}$	B8	Low	Input	OV_{DD}	
$\overline{\text{CKSTP\_OUT}}$	D7	Low	Output	OV_{DD}	
CLK_OUT	E3	—	Output	OV_{DD}	
$\overline{\text{DBB}}$	K5	Low	I/O	OV_{DD}	
$\overline{\text{DBDIS}}$	G1	Low	Input	OV_{DD}	
$\overline{\text{DBG}}$	K1	Low	Input	OV_{DD}	
$\overline{\text{DBWO}}$	D1	Low	Input	OV_{DD}	

Table 15. Pinout Listing for the MPC755, 360 BGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
DH[0:31]	W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5	High	I/O	OV_{DD}	
DL[0:31]	M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2	High	I/O	OV_{DD}	
DP[0:7]	L1, P2, M2, V2, M1, N2, T3, R1	High	I/O	OV_{DD}	
$\overline{\text{DRTRY}}$	H6	Low	Input	OV_{DD}	
$\overline{\text{GBL}}$	B1	Low	I/O	OV_{DD}	
GND	D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16	—	—	GND	
$\overline{\text{HRESET}}$	B6	Low	Input	OV_{DD}	
$\overline{\text{INT}}$	C11	Low	Input	OV_{DD}	
L1_TSTCLK	F8	High	Input	—	2
L2ADDR[16:0]	G18, H19, J13, J14, H17, H18, J16, J17, J18, J19, K15, K17, K18, M19, L19, L18, L17	High	Output	$L2OV_{DD}$	
$L2AV_{DD}$	L13	—	—	2.0 V	
$\overline{\text{L2CE}}$	P17	Low	Output	$L2OV_{DD}$	
L2CLK_OUTA	N15	—	Output	$L2OV_{DD}$	
L2CLK_OUTB	L16	—	Output	$L2OV_{DD}$	
L2DATA[0:63]	U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13	High	I/O	$L2OV_{DD}$	
L2DP[0:7]	V14, U16, T19, N18, H14, F17, C19, B15	High	I/O	$L2OV_{DD}$	
$L2OV_{DD}$	D15, E14, E16, H16, J15, L15, M16, P15, R14, R16, T15, F15	—	—	$L2OV_{DD}$	
L2SYNC_IN	L14	—	Input	$L2OV_{DD}$	
L2SYNC_OUT	M14	—	Output	$L2OV_{DD}$	
L2_TSTCLK	F7	High	Input	—	2
L2VSEL	A19	High	Input	$L2OV_{DD}$	1, 5, 6, 7
$\overline{\text{L2WE}}$	N16	Low	Output	$L2OV_{DD}$	

Table 15. Pinout Listing for the MPC755, 360 BGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
L2ZZ	G17	High	Output	$L2OV_{DD}$	
$\overline{\text{LSSD\_MODE}}$	F9	Low	Input	—	2
$\overline{\text{MCP}}$	B11	Low	Input	OV_{DD}	
NC (No Connect)	B3, B4, B5, W19, K9, K11 [4], K19 [4]	—	—	—	
OV_{DD}	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12	—	—	OV_{DD}	
PLL_CFG[0:3]	A4, A5, A6, A7	High	Input	OV_{DD}	
$\overline{\text{QACK}}$	B2	Low	Input	OV_{DD}	
$\overline{\text{QREQ}}$	J3	Low	Output	OV_{DD}	
$\overline{\text{RSRV}}$	D3	Low	Output	OV_{DD}	
$\overline{\text{SMI}}$	A12	Low	Input	OV_{DD}	
$\overline{\text{SRESET}}$	E10	Low	Input	OV_{DD}	
SYSCLK	H9	—	Input	OV_{DD}	
$\overline{\text{TA}}$	F1	Low	Input	OV_{DD}	
TBEN	A2	High	Input	OV_{DD}	
$\overline{\text{TBST}}$	A11	Low	I/O	OV_{DD}	
TCK	B10	High	Input	OV_{DD}	
TDI	B7	High	Input	OV_{DD}	6
TDO	D9	High	Output	OV_{DD}	
$\overline{\text{TEA}}$	J1	Low	Input	OV_{DD}	
$\overline{\text{TLBISYNC}}$	A3	Low	Input	OV_{DD}	
TMS	C8	High	Input	OV_{DD}	6
$\overline{\text{TRST}}$	A10	Low	Input	OV_{DD}	6
$\overline{\text{TS}}$	K7	Low	I/O	OV_{DD}	
TSIZ[0:2]	A9, B9, C9	High	Output	OV_{DD}	
TT[0:4]	C10, D11, B12, C12, F11	High	I/O	OV_{DD}	
$\overline{\text{WT}}$	C3	Low	Output	OV_{DD}	
V_{DD}	G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12	—	—	2.0 V	

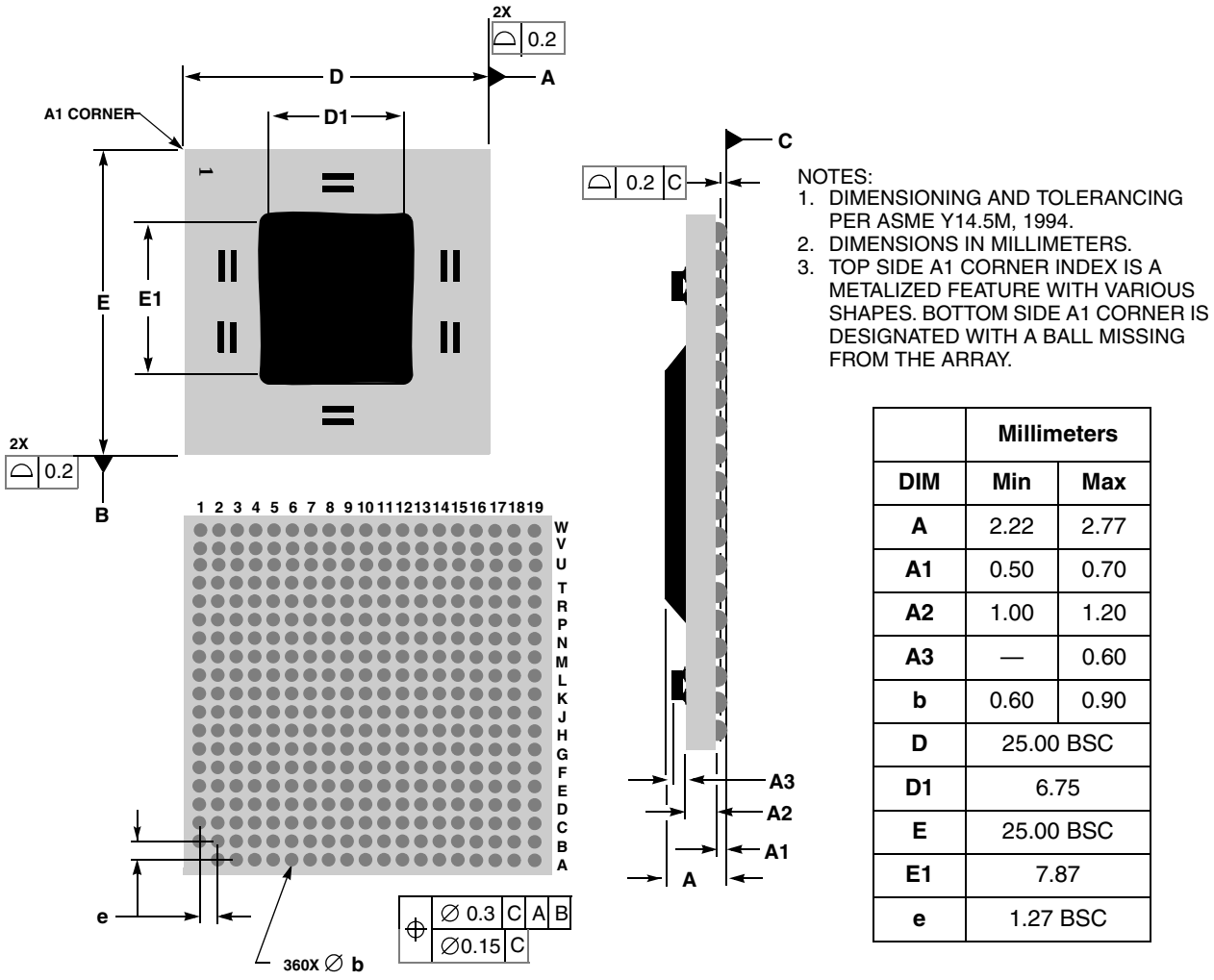
7.5 Package Parameters for the MPC755 PBGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead plastic ball grid array (PBGA).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.22 mm
Maximum module height	2.77 mm
Ball diameter	0.75 mm (29.5 mil)

7.6 Mechanical Dimensions for the MPC755

Figure 20 provides the mechanical dimensions and bottom surface nomenclature for the MPC755, 360 PBGA package.



	Millimeters	
DIM	Min	Max
A	2.22	2.77
A1	0.50	0.70
A2	1.00	1.20
A3	—	0.60
b	0.60	0.90
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	

Figure 20. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC755, 360 PBGA Package

Table 16. MPC755 Microprocessor PLL Configuration Example for 400 MHz Parts (continued)

PLL_CFG [0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus 33 MHz	Bus 50 MHz	Bus 66 MHz	Bus 75 MHz	Bus 80 MHz	Bus 100 MHz
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied					
1111	PLL off		PLL off, no core clocking occurs					

Notes:

1. PLL_CFG[0:3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the MPC755; see Section 4.2.1, "Clock AC Specifications," for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL off mode, no clocking occurs inside the MPC755 regardless of the SYSCLK input.

The MPC755 generates the clock for the external L2 synchronous data SRAMs by dividing the core clock frequency of the MPC755. The divided-down clock is then phase-adjusted by an on-chip delay-lock-loop (DLL) circuit and should be routed from the MPC755 to the external RAMs. A separate clock output, L2SYNC_OUT is sent out half the distance to the SRAMs and then returned as an input to the DLL on pin L2SYNC_IN so that the rising-edge of the clock as seen at the external RAMs can be aligned to the clocking of the internal latches in the L2 bus interface.

The core-to-L2 frequency divisor for the L2 PLL is selected through the L2CLK bits of the L2CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the MPC755 core, and the phase adjustment range that the L2 DLL supports. Table 17 shows various example L2 clock frequencies that can be obtained for a given set of core frequencies. The minimum L2 frequency target is 80 MHz.

Table 17. Sample Core-to-L2 Frequencies

Core Frequency (MHz)	÷1	÷1.5	÷2	÷2.5	÷3
250	250	166	125	100	83
266	266	177	133	106	89
275	275	183	138	110	92
300	300	200	150	120	100
325	325	217	163	130	108
333	333	222	167	133	111
350	350	233	175	140	117
366	366	244	183	146	122

Table 17. Sample Core-to-L2 Frequencies (continued)

Core Frequency (MHz)	÷1	÷1.5	÷2	÷2.5	÷3
375	375	250	188	150	125
400	400	266	200	160	133

Note: The core and L2 frequencies are for reference only. Some examples may represent core or L2 frequencies which are not useful, not supported, or not tested for by the MPC755; see Section 4.2.3, "L2 Clock AC Specifications," for valid L2CLK frequencies. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz.

8.2 PLL Power Supply Filtering

The AV_{DD} and $L2AV_{DD}$ power signals are provided on the MPC755 to provide power to the clock generation PLL and L2 cache DLL, respectively. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 21 using surface mount capacitors with minimum Effective Series Inductance (ESL) is recommended. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. An identical but separate circuit should be placed as close as possible to the $L2AV_{DD}$ pin. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 BGA footprint, without the inductance of vias. The $L2AV_{DD}$ pin may be more difficult to route, but is proportionately less critical.

Figure 21 shows the PLL power supply filter circuit.

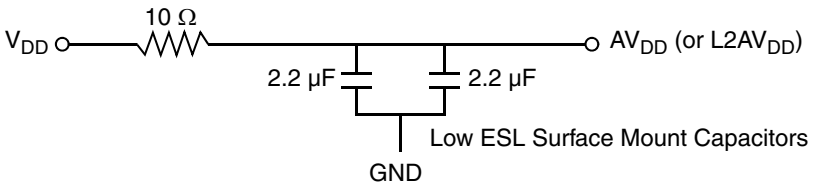


Figure 21. PLL Power Supply Filter Circuit

8.3 Decoupling Recommendations

Due to the MPC755 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC755 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC755 system, and the MPC755 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and $L2OV_{DD}$ pin of the MPC755. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, $(L2)OV_{DD}$, and GND power planes in the PCB, utilizing short traces to minimize inductance.

should be left unconnected by the system. If all parity generation is disabled through HID0, then all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

The L2 interface does not require pull-up resistors.

8.7 JTAG Configuration Signals

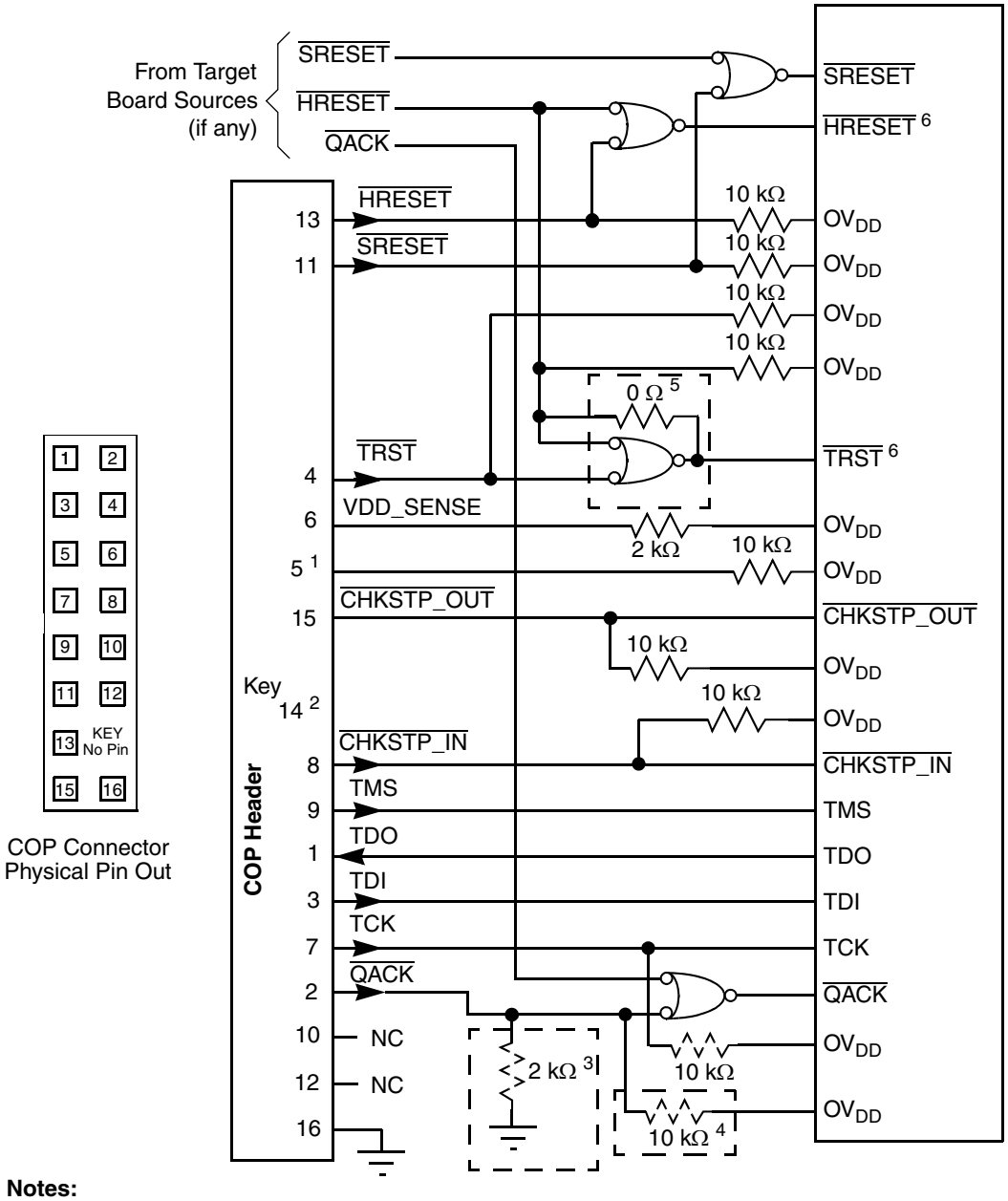
Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 24 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted ensuring that the JTAG scan chain is initialized during power-on. While Freescale recommends that the COP header be designed into the system as shown in Figure 24, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 24 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.



Notes:

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the MPC755. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively deassert $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0-Ω isolation resistor.
6. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.

Figure 24. JTAG Interface Connection

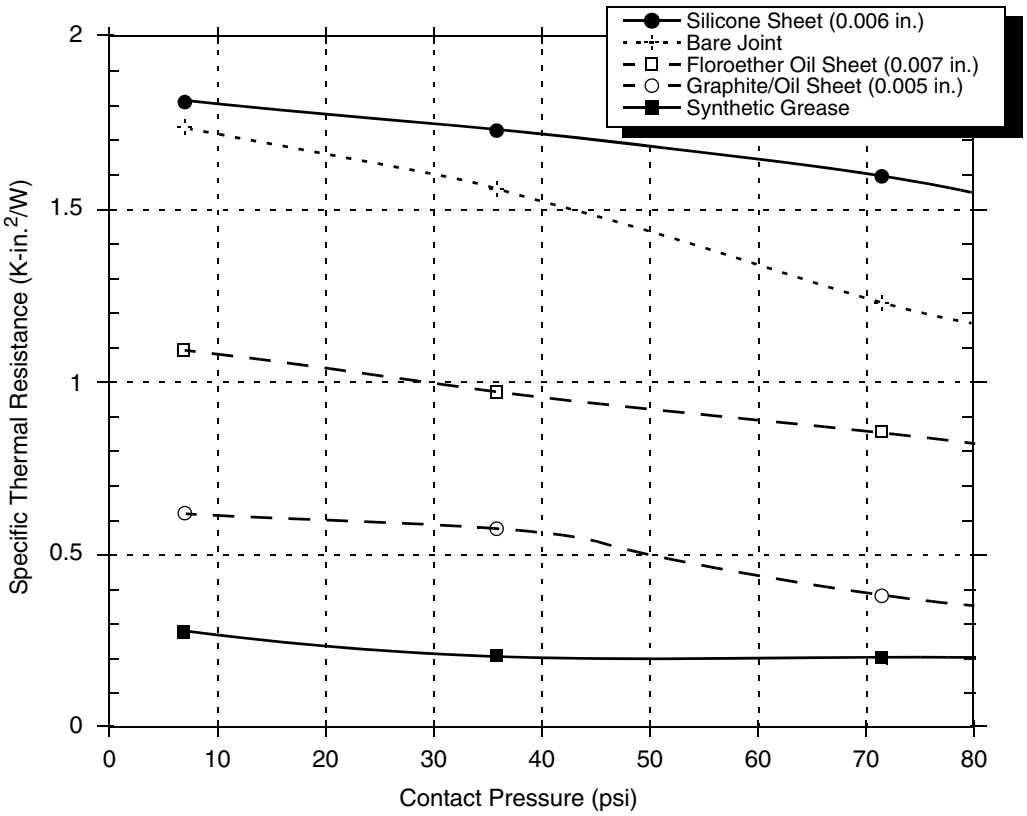


Figure 27. Thermal Performance of Select Thermal Interface Materials

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company — 800-347-4572
18930 West 78th St.
Chanhassen, MN 55317
Internet: www.bergquistcompany.com

Chomerics, Inc. — 781-935-4850
77 Dragon Ct.
Woburn, MA 01888-4014
Internet: www.chomerics.com

Dow-Corning Corporation — 800-248-2481
Dow-Corning Electronic Materials
2200 W. Salzburg Rd.
Midland, MI 48686-0997
Internet: www.dow.com

9 Document Revision History

Table 19 provides a revision history for this hardware specification.

Table 19. Document Revision History

Revision	Date	Substantive Change(s)
8	2/8/2006	Changed processor descriptor from ‘B’ to ‘C’ for 350 MHz devices and increased power specifications for full-power mode in Table 7.
7	4/05/2005	Removed phrase “for the ceramic ball grid array (CBGA) package” from Section 8.8; this information applies to devices in both CBGA and PBGA packages.
		Figure 24—updated COP Connector Diagram to recommend a weak pull-up resistor on TCK.
		Table 20—added MPC745BPXLE, MPC755BRXLE, MPC755BPXLE, MPC755CVTLE, MPC755BVTLE and MPC745BVTLE part numbers. These devices are fully addressed by this document.
		Corrected Revision Level in Table 23: Rev E devices are Rev 2.8, not 2.7.
		Added MPC755CRX400LE and MPC755CPX400LE to devices supported by this specification in Table 20.
		Removed “Advance Information” from title block on page 1.
6.1	1/21/2005	Updated document template.
6	—	Removed 450 MHz speed grade throughout document. These devices are no longer supported for new designs; see Section 1.10.2 for more information.
		Relaxed voltage sequencing requirements in Notes 3 and 4 of Table 1.
		Corrected Note 2 of Table 7.
		Changed processor descriptor from ‘B’ to ‘C’ for 400 MHz devices and increased power specifications for full-power mode in Table 7. XPC755Bxx400LE devices are no longer produced and are documented in a separate part number specification; see Section 1.10.2 for more information.
		Increased power specifications for sleep mode for all speed grades in Table 7.
		Removed ‘Sleep Mode (PLL and DLL Disabled)—Typical’ specification from Table 7; this is no longer tested or characterized.
		Added Note 4 to Table 7.
		Revised L2 clock duty cycle specification in Table 11 and changed Note 7.
		Corrected Note 3 in Table 20.
		Replaced Table 21 and added Tables 22 and 23.
5	—	Added Note 6 to Table 10; clarification only as this information is already documented in the *MPC750 RISC Microprocessor Family User’s Manual*.
		Revised Figure 24 and Section 1.8.7.
		Corrected Process Identifier for 450 MHz part in Table 20.
		Added XPC755BRX*nnn*T*x* series to Table 21.