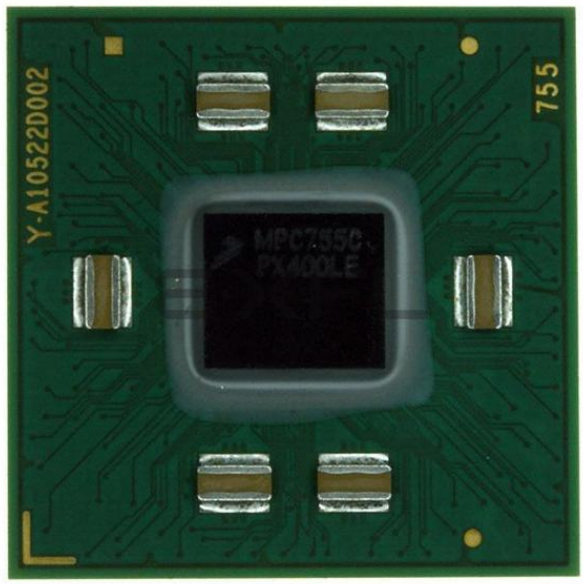

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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	350MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BBGA, FCBGA
Supplier Device Package	360-FCPBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc755cpx350le

  - Selectable interface voltages of 2.5 and 3.3 V
  - Parity checking on both L2 address and data
- Memory management unit
  - 128-entry, two-way set-associative instruction TLB
  - 128-entry, two-way set-associative data TLB
  - Hardware reload for TLBs
  - Hardware or optional software tablewalk support
  - Eight instruction BATs and eight data BATs
  - Eight SPRGs, for assistance with software tablewalks
  - Virtual memory support for up to 4 exabytes (2^{52}) of virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
- Bus interface
  - Compatible with 60x processor interface
  - 32-bit address bus
  - 64-bit data bus, 32-bit mode selectable
  - Bus-to-core frequency multipliers of 2x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 10x supported
  - Selectable interface voltages of 2.5 and 3.3 V
  - Parity checking on both address and data buses
- Power management
  - Low-power design with thermal requirements very similar to MPC740/MPC750
  - Three static power saving modes: doze, nap, and sleep
  - Dynamic power management
- Integrated thermal management assist unit
  - On-chip thermal sensor and control logic
  - Thermal management interrupt for software regulation of junction temperature
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface

3 General Parameters

The following list provides a summary of the general parameters of the MPC755:

Technology	0.22 µm CMOS, six-layer metal
Die size	6.61 mm × 7.73 mm (51 mm^2)
Transistor count	6.75 million
Logic design	Fully-static

Packages	MPC745: Surface mount 255 plastic ball grid array (PBGA) MPC755: Surface mount 360 ceramic ball grid array (CBGA) Surface mount 360 plastic ball grid array (PBGA)
Core power supply	2.0 V ± 100 mV DC (nominal; some parts support core voltages down to 1.8 V; see Table 3 for recommended operating conditions)
I/O power supply	2.5 V ± 100 mV DC or 3.3 V ± 165 mV DC (input thresholds are configuration pin selectable)

4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC755.

4.1 DC Electrical Characteristics

Table 1 through Table 7 describe the MPC755 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Maximum Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 2.5	V	4
PLL supply voltage		AV_{DD}	–0.3 to 2.5	V	4
L2 DLL supply voltage		$L2AV_{DD}$	–0.3 to 2.5	V	4
Processor bus supply voltage		OV_{DD}	–0.3 to 3.6	V	3
L2 bus supply voltage		$L2OV_{DD}$	–0.3 to 3.6	V	3
Input voltage	Processor bus	V_{in}	–0.3 to OV_{DD} + 0.3 V	V	2, 5
	L2 bus	V_{in}	–0.3 to $L2OV_{DD}$ + 0.3 V	V	2, 5
	JTAG signals	V_{in}	–0.3 to 3.6	V	
Storage temperature range		T_{stg}	–55 to 150	°C	

Notes:

1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** V_{in} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.3 V at any time including during power-on reset.
3. **Caution:** $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 1.6 V during normal operation. During power-on reset and power-down sequences, $L2OV_{DD}/OV_{DD}$ may exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by up to 3.3 V for up to 20 ms, or by 2.5 V for up to 40 ms. Excursions beyond 3.3 V or 40 ms are not supported.
4. **Caution:** $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4 V during normal operation. During power-on reset and power-down sequences, $V_{DD}/AV_{DD}/L2AV_{DD}$ may exceed $L2OV_{DD}/OV_{DD}$ by up to 1.0 V for up to 20 ms, or by 0.7 V for up to 40 ms. Excursions beyond 1.0 V or 40 ms are not supported.
5. This is a DC specifications only. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

Table 3 provides the recommended operating conditions for the MPC755.

Table 3. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value				Unit	Notes
			300 MHz, 350 MHz		400 MHz			
			Min	Max	Min	Max		
Core supply voltage		V_{DD}	1.80	2.10	1.90	2.10	V	3
PLL supply voltage		AV_{DD}	1.80	2.10	1.90	2.10	V	3
L2 DLL supply voltage		$L2AV_{DD}$	1.80	2.10	1.90	2.10	V	3
Processor bus supply voltage	BVSEL = 1	OV_{DD}	2.375	2.625	2.375	2.625	V	2, 4
			3.135	3.465	3.135	3.465		5
L2 bus supply voltage	L2VSEL = 1	$L2OV_{DD}$	2.375	2.625	2.375	2.625	V	2, 4
			3.135	3.465	3.135	3.465		5
Input voltage	Processor bus	V_{in}	GND	OV_{DD}	GND	OV_{DD}	V	
	L2 bus	V_{in}	GND	$L2OV_{DD}$	GND	$L2OV_{DD}$	V	
	JTAG signals	V_{in}	GND	OV_{DD}	GND	OV_{DD}	V	
Die-junction temperature		T_j	0	105	0	105	°C	

Notes:

1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. Revisions prior to Rev. 2.8 (Rev. E) offered different I/O voltage support. For more information, refer to Section 10.2, “Part Numbers Not Fully Addressed by This Document.”
3. 2.0 V nominal.
4. 2.5 V nominal.
5. 3.3 V nominal.

Table 4 provides the package thermal characteristics for the MPC755 and MPC745. The MPC755 was initially sampled in a CBGA package, but production units are currently provided in both a CBGA and a PBGA package. Because of the better long-term device-to-board interconnect reliability of the PBGA package, Freescale recommends use of a PBGA package except where circumstances dictate use of a CBGA package. The MPC745 is offered in a PBGA package only.

Table 6. DC Electrical Specifications (continued)

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage [1]	Symbol	Min	Max	Unit	Notes
Capacitance, V_{in} = 0 V, f = 1 MHz		C_{in}	—	5.0	pF	3, 4

Notes:

1. Nominal voltages; see Table 3 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD} while $L2OV_{DD}$ is the reference for the L2 bus signals.
3. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK) and IEEE 1149.1 boundary scan (JTAG) signals.
4. Capacitance is periodically sampled rather than 100% tested.
5. The leakage is measured for nominal OV_{DD} and V_{DD}, or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or –5%).

Table 7 provides the power consumption for the MPC755.

Table 7. Power Consumption for MPC755

	Processor (CPU) Frequency			Unit	Notes
	300 MHz	350 MHz	400 MHz		
Full-Power Mode					
Typical	3.1	3.6	5.4	W	1, 3, 4
Maximum	4.5	6.0	8.0	W	1, 2
Doze Mode					
Maximum	1.8	2.0	2.3	W	1, 2, 4
Nap Mode					
Maximum	1.0	1.0	1.0	W	1, 2, 4
Sleep Mode					
Maximum	550	550	550	mW	1, 2, 4
Sleep Mode (PLL and DLL Disabled)					
Maximum	510	510	510	mW	1, 2

Notes:

1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O supply power (OV_{DD} and $L2OV_{DD}$) or PLL/DLL supply power (AV_{DD} and $L2AV_{DD}$). OV_{DD} and $L2OV_{DD}$ power is system dependent, but is typically <10% of V_{DD} power. Worst case power consumption for AV_{DD} = 15 mW and $L2AV_{DD}$ = 15 mW.
2. Maximum power is measured at nominal V_{DD} (see Table 3) while running an entirely cache-resident, contrived sequence of instructions which keep the execution units maximally busy.
3. Typical power is an average value measured at the nominal recommended V_{DD} (see Table 3) and 65°C in a system while running a typical code sequence.
4. Not 100% tested. Characterized and periodically sampled.

Figure 4 provides the mode select input timing diagram for the MPC755.

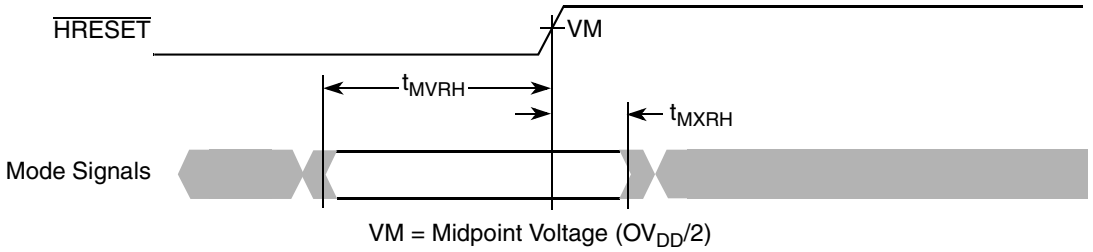


Figure 4. Mode Input Timing Diagram

Figure 5 provides the AC test load for the MPC755.

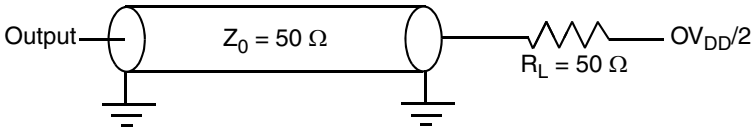


Figure 5. AC Test Load

Table 11. L2CLK Output AC Timing Specification

At recommended operating conditions (see Table 3)

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
L2CLK frequency	f_{L2CLK}	80	450	MHz	1, 4
L2CLK cycle time	t_{L2CLK}	2.5	12.5	ns	
L2CLK duty cycle	t_{CHCL}/t_{L2CLK}	45	55	%	2, 7
Internal DLL-relock time		640	—	L2CLK	3, 7
DLL capture window		0	10	ns	5, 7
L2CLK_OUT output-to-output skew	t_{L2CSKW}	—	50	ps	6, 7
L2CLK_OUT output jitter		—	±150	ps	6, 7

Notes:

1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB, L2CLK_OUT, and L2SYNC_OUT pins. The L2CLK frequency-to-core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. The maximum L2LCK frequency will be system dependent. L2CLK_OUTA and L2CLK_OUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The DLL-relock time is specified in terms of L2CLK periods. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in ns. Relock timing is guaranteed by design and characterization.
4. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz. This adds more delay to each tap of the DLL.
5. Allowable skew between L2SYNC_OUT and L2SYNC_IN.
6. This output jitter number represents the maximum delay of one tap forward or one tap back from the current DLL tap as the phase comparator seeks to minimize the phase difference between L2SYNC_IN and the internal L2CLK. This number must be comprehended in the L2 timing analysis. The input jitter on SYSCLK affects L2CLK_OUT and the L2 address/data/control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L2 timing analysis.
7. Guaranteed by design.

4.2.5 IEEE 1149.1 AC Timing Specifications

Table 13 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 12 through Figure 15.

Table 13. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions (see Table 3)

Parameter		Symbol	Min	Max	Unit	Notes
TCK frequency of operation		f_{TCLK}	0	16	MHz	
TCK cycle time		t_{TCLK}	62.5	—	ns	
TCK clock pulse width measured at 1.4 V		t_{JHJL}	31	—	ns	
TCK rise and fall times		t_{JR}, t_{JF}	0	2	ns	
$\overline{\text{TRST}}$ assert time		t_{TRST}	25	—	ns	2
Input setup times:	Boundary-scan data TMS, TDI	t_{DVJH} t_{IVJH}	4 0	— —	ns	3
Input hold times:	Boundary-scan data TMS, TDI	t_{DXJH} t_{IXJH}	15 12	— —	ns	3
Valid times:	Boundary-scan data TDO	t_{JLDV} t_{JLOV}	— —	4 4	ns	4
Output hold times:	Boundary-scan data TDO	t_{JLDH} t_{JLOH}	25 12	— —	ns	4
TCK to output high impedance:	Boundary-scan data TDO	t_{JLDZ} t_{JLOZ}	3 3	19 9	ns	4, 5

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 11). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal which must be asserted for this minimum time to be recognized.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 11 provides the AC test load for TDO and the boundary-scan outputs of the MPC755.

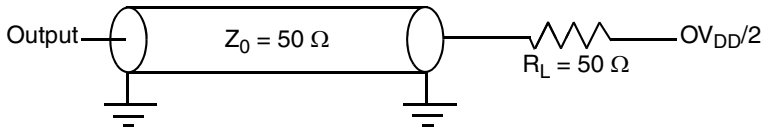


Figure 11. AC Test Load for the JTAG Interface

Figure 12 provides the JTAG clock input timing diagram.

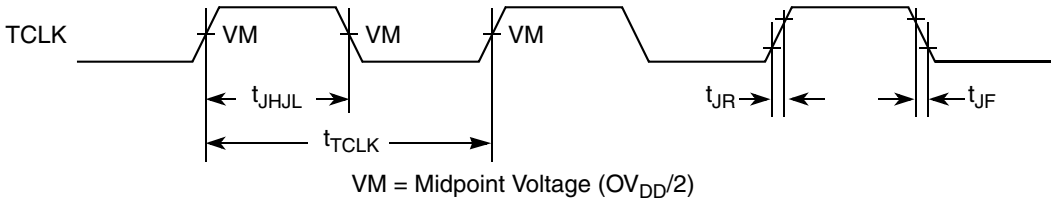


Figure 12. JTAG Clock Input Timing Diagram

Figure 13 provides the $\overline{\text{TRST}}$ timing diagram.

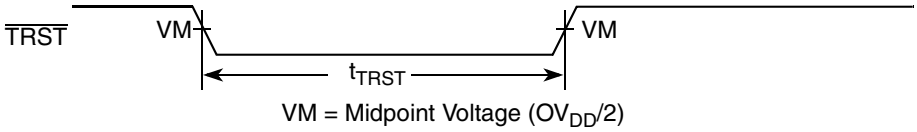


Figure 13. $\overline{\text{TRST}}$ Timing Diagram

Figure 14 provides the boundary-scan timing diagram.

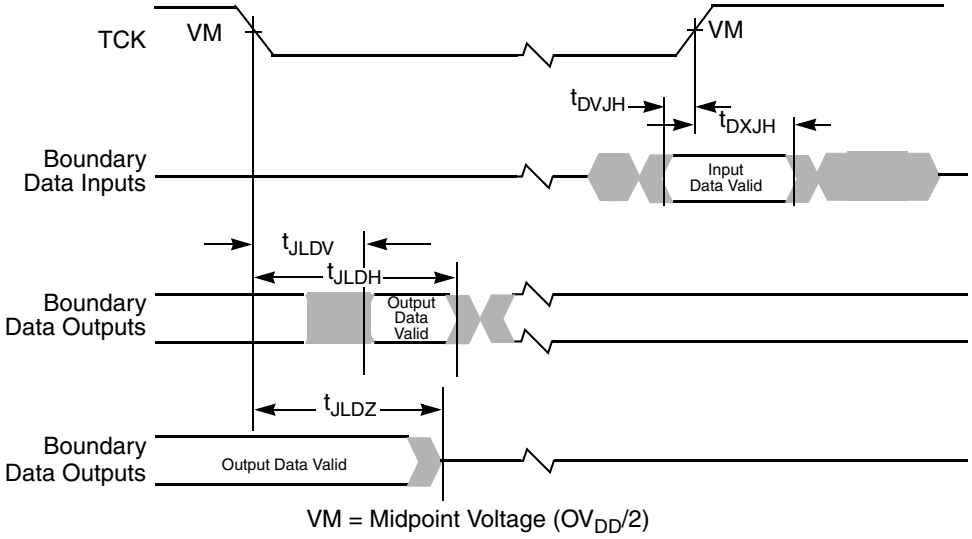
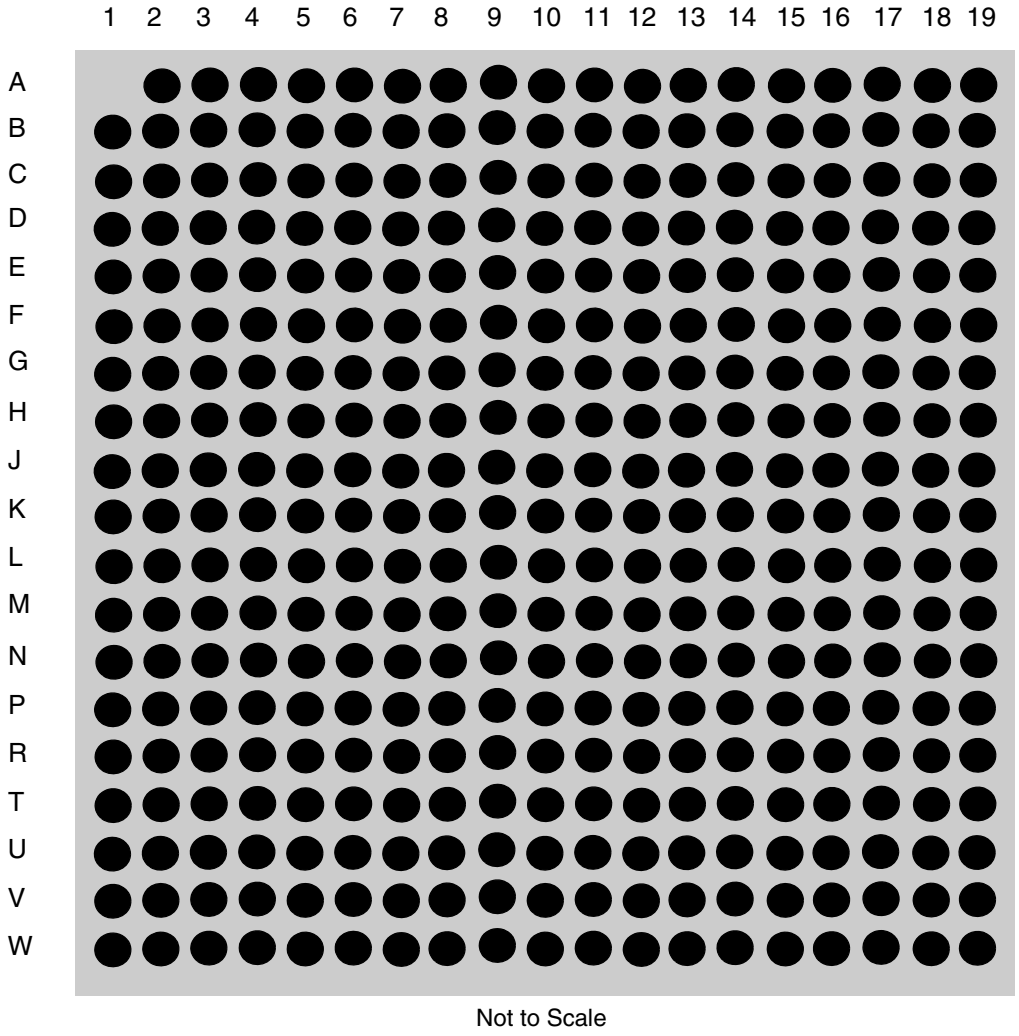


Figure 14. Boundary-Scan Timing Diagram

Figure 17 (in Part A) shows the pinout of the MPC755, 360 PBGA and 360 CBGA packages as viewed from the top surface. Part B shows the side profile of the PBGA and CBGA package to indicate the direction of the top surface view.

Part A



Part B

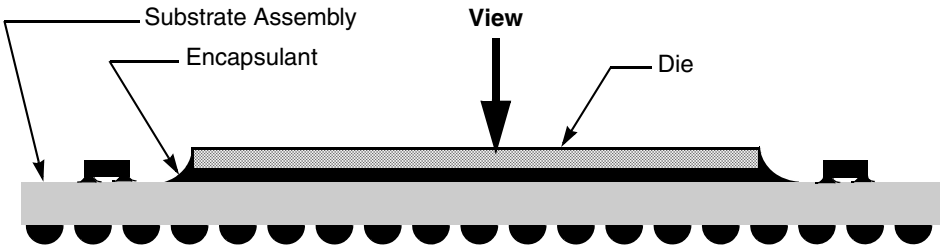


Figure 17. Pinout of the MPC755, 360 PBGA and CBGA Packages as Viewed from the Top Surface

6 Pinout Listings

Table 14 provides the pinout listing for the MPC745, 255 PBGA package.

Table 14. Pinout Listing for the MPC745, 255 PBGA Package

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
A[0:31]	C16, E4, D13, F2, D14, G1, D15, E2, D16, D4, E13, G2, E15, H1, E16, H2, F13, J1, F14, J2, F15, H3, F16, F4, G13, K1, G15, K2, H16, M1, J15, P1	High	I/O	OV_{DD}	
$\overline{\text{AACK}}$	L2	Low	Input	OV_{DD}	
$\overline{\text{ABB}}$	K4	Low	I/O	OV_{DD}	
AP[0:3]	C1, B4, B3, B2	High	I/O	OV_{DD}	
$\overline{\text{ARTRY}}$	J4	Low	I/O	OV_{DD}	
AV_{DD}	A10	—	—	2.0 V	
$\overline{\text{BG}}$	L1	Low	Input	OV_{DD}	
$\overline{\text{BR}}$	B6	Low	Output	OV_{DD}	
BVSEL	B1	High	Input	OV_{DD}	3, 4, 5
$\overline{\text{CI}}$	E1	Low	Output	OV_{DD}	
$\overline{\text{CKSTP\_IN}}$	D8	Low	Input	OV_{DD}	
$\overline{\text{CKSTP\_OUT}}$	A6	Low	Output	OV_{DD}	
CLK_OUT	D7	—	Output	OV_{DD}	
$\overline{\text{DBB}}$	J14	Low	I/O	OV_{DD}	
$\overline{\text{DBG}}$	N1	Low	Input	OV_{DD}	
$\overline{\text{DBDIS}}$	H15	Low	Input	OV_{DD}	
$\overline{\text{DBWO}}$	G4	Low	Input	OV_{DD}	
DH[0:31]	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P9, N9, T10, R9, T9, P8, N8, R8, T8, N7, R7, T7, P6, N6, R6, T6, R5, N5, T5, T4	High	I/O	OV_{DD}	
DL[0:31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P3, N3, N4, R3, T1, T2, P4, T3, R4	High	I/O	OV_{DD}	
DP[0:7]	M2, L3, N2, L4, R1, P2, M4, R2	High	I/O	OV_{DD}	
$\overline{\text{DRTRY}}$	G16	Low	Input	OV_{DD}	
$\overline{\text{GBL}}$	F1	Low	I/O	OV_{DD}	
GND	C5, C12, E3, E6, E8, E9, E11, E14, F5, F7, F10, F12, G6, G8, G9, G11, H5, H7, H10, H12, J5, J7, J10, J12, K6, K8, K9, K11, L5, L7, L10, L12, M3, M6, M8, M9, M11, M14, P5, P12	—	—	GND	
$\overline{\text{HRESET}}$	A7	Low	Input	OV_{DD}	

Table 15. Pinout Listing for the MPC755, 360 BGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
VOLTDET	K13	High	Output	$L2OV_{DD}$	8

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L2 cache controls ($\overline{L2CE}$, $\overline{L2WE}$, and L2ZZ); $L2OV_{DD}$ supplies power to the L2 cache interface (L2ADDR[0:16], L2DATA[0:63], L2DP[0:7], and L2SYNC_OUT) and the L2 control signals; and V_{DD} supplies power to the processor core and the PLL and DLL (after filtering to become AV_{DD} and $L2AV_{DD}$, respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL/L2VSEL pin configurations of Table 2 and the voltage supplied. For actual recommended value of V_{in} or supply voltages, see Table 3.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. This pin must be pulled up to OV_{DD} for proper operation of the processor interface. To allow for future I/O voltage changes, provide the option to connect BVSEL independently to either OV_{DD} or GND.
4. These pins are reserved for potential future use as additional L2 address pins.
5. Uses one of nine existing no connects in the MPC750, 360 BGA package.
6. Internal pull-up on die.
7. This pin must be pulled up to $L2OV_{DD}$ for proper operation of the processor interface. To allow for future I/O voltage changes, provide the option to connect L2VSEL independently to either $L2OV_{DD}$ or GND.
8. Internally tied to $L2OV_{DD}$ in the MPC755, 360 BGA package to indicate the power present at the L2 cache interface. This signal is not a power supply input.

   Caution: This differs from the MPC745, 255 BGA package.

7 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC745, 255 PBGA package, as well as the MPC755, 360 CBGA and PBGA packages. While both the MPC755 plastic and ceramic packages are described here, both packages are not guaranteed to be available at the same time. All new designs should allow for either ceramic or plastic BGA packages for this device. For more information on designing a common footprint for both plastic and ceramic package types, see the *Freescale Flip-Chip Plastic Ball Grid Array Presentation*. The MPC755 was initially sampled in a CBGA package, but production units are currently provided in both a CBGA and a PBGA package. Because of the better long-term device-to-board interconnect reliability of the PBGA package, Freescale recommends use of a PBGA package except where circumstances dictate use of a CBGA package.

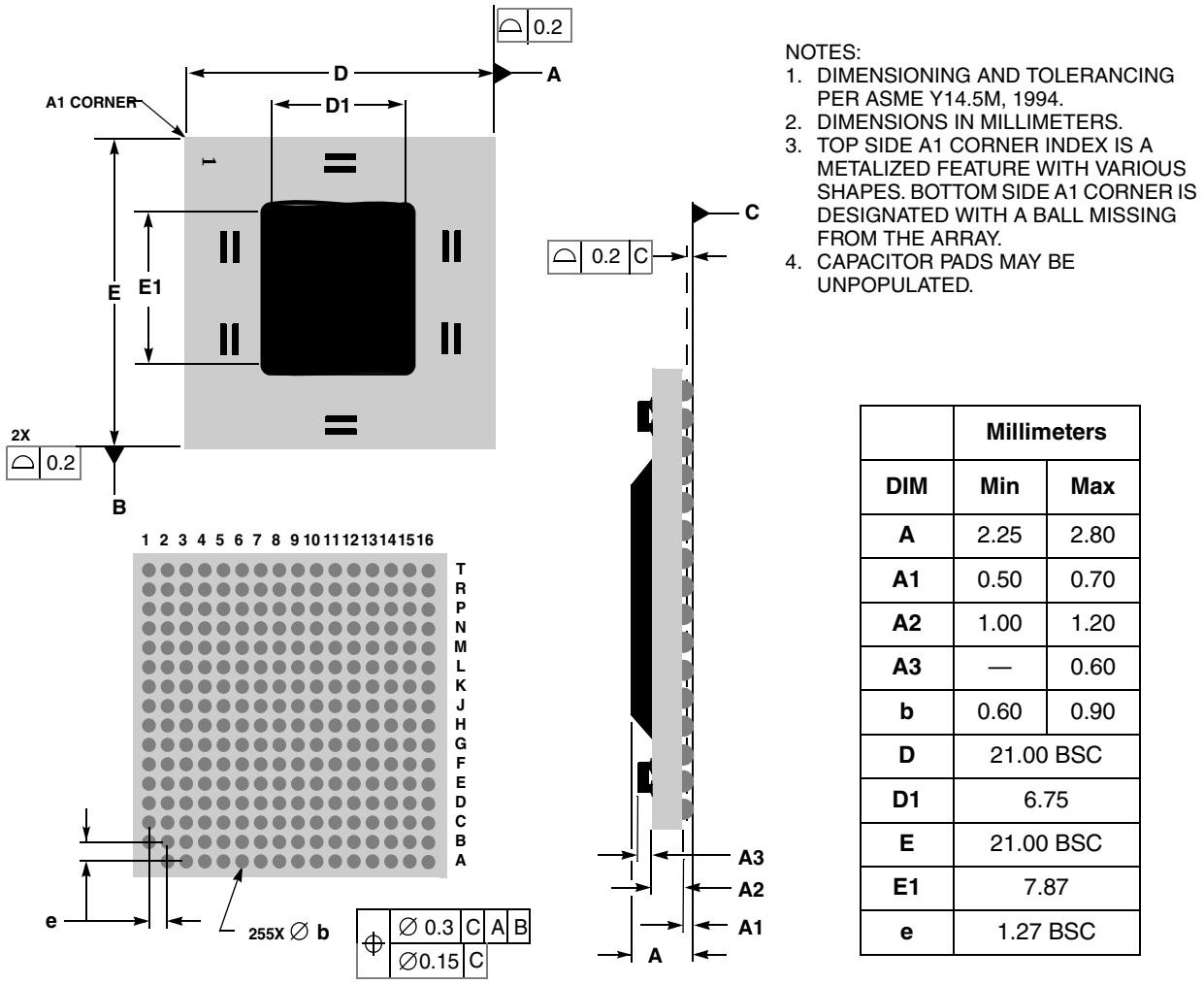
7.1 Package Parameters for the MPC745 PBGA

The package parameters are as provided in the following list. The package type is 21 × 21 mm, 255-lead plastic ball grid array (PBGA).

Package outline	21 × 21 mm
Interconnects	255 (16 × 16 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.25 mm
Maximum module height	2.80 mm
Ball diameter (typical)	0.75 mm (29.5 mil)

7.2 Mechanical Dimensions for the MPC745 PBGA

Figure 18 provides the mechanical dimensions and bottom surface nomenclature for the MPC745, 255 PBGA package.



	Millimeters	
DIM	Min	Max
A	2.25	2.80
A1	0.50	0.70
A2	1.00	1.20
A3	—	0.60
b	0.60	0.90
D	21.00 BSC	
D1	6.75	
E	21.00 BSC	
E1	7.87	
e	1.27 BSC	

Figure 18. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC745, 255 PBGA Package

8 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC755.

8.1 PLL Configuration

The MPC755 PLL is configured by the PLL_CFG[0:3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. These must be chosen such that they comply with Table 8. Table 16 shows the valid configurations of these signals and an example illustrating the core and VCO frequencies resulting from various PLL configurations and example bus frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the 400-MHz column in Table 8.

Table 16. MPC755 Microprocessor PLL Configuration Example for 400 MHz Parts

PLL_CFG [0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus 33 MHz	Bus 50 MHz	Bus 66 MHz	Bus 75 MHz	Bus 80 MHz	Bus 100 MHz
0100	2x	2x	—	—	—	—	—	200 (400)
1000	3x	2x	—	—	200 (400)	225 (450)	240 (480)	300 (600)
1110	3.5x	2x	—	—	233 (466)	263 (525)	280 (560)	350 (700)
1010	4x	2x	—	200 (400)	266 (533)	300 (600)	320 (640)	400 (800)
0111	4.5x	2x	—	225 (450)	300 (600)	338 (675)	360 (720)	—
1011	5x	2x	—	250 (500)	333 (666)	375 (750)	400 (800)	—
1001	5.5x	2x	—	275 (550)	366 (733)	—	—	—
1101	6x	2x	200 (400)	300 (600)	400 (800)	—	—	—
0101	6.5x	2x	216 (433)	325 (650)	—	—	—	—
0010	7x	2x	233 (466)	350 (700)	—	—	—	—
0001	7.5x	2x	250 (500)	375 (750)	—	—	—	—
1100	8x	2x	266 (533)	400 (800)	—	—	—	—
0110	10x	2x	333 (666)	—	—	—	—	—

Table 16. MPC755 Microprocessor PLL Configuration Example for 400 MHz Parts (continued)

PLL_CFG [0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus 33 MHz	Bus 50 MHz	Bus 66 MHz	Bus 75 MHz	Bus 80 MHz	Bus 100 MHz
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied					
1111	PLL off		PLL off, no core clocking occurs					

Notes:

1. PLL_CFG[0:3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the MPC755; see Section 4.2.1, "Clock AC Specifications," for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL off mode, no clocking occurs inside the MPC755 regardless of the SYSCLK input.

The MPC755 generates the clock for the external L2 synchronous data SRAMs by dividing the core clock frequency of the MPC755. The divided-down clock is then phase-adjusted by an on-chip delay-lock-loop (DLL) circuit and should be routed from the MPC755 to the external RAMs. A separate clock output, L2SYNC_OUT is sent out half the distance to the SRAMs and then returned as an input to the DLL on pin L2SYNC_IN so that the rising-edge of the clock as seen at the external RAMs can be aligned to the clocking of the internal latches in the L2 bus interface.

The core-to-L2 frequency divisor for the L2 PLL is selected through the L2CLK bits of the L2CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the MPC755 core, and the phase adjustment range that the L2 DLL supports. Table 17 shows various example L2 clock frequencies that can be obtained for a given set of core frequencies. The minimum L2 frequency target is 80 MHz.

Table 17. Sample Core-to-L2 Frequencies

Core Frequency (MHz)	÷1	÷1.5	÷2	÷2.5	÷3
250	250	166	125	100	83
266	266	177	133	106	89
275	275	183	138	110	92
300	300	200	150	120	100
325	325	217	163	130	108
333	333	222	167	133	111
350	350	233	175	140	117
366	366	244	183	146	122

The board designer can choose between several types of heat sinks to place on the MPC755. There are several commercially-available heat sinks for the MPC755 provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

8.8.1 Internal Package Conduction Resistance

For the exposed-die packaging technology, shown in Table 4, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case (or top-of-die for exposed silicon) thermal resistance
- The die junction-to-ball thermal resistance

Figure 26 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.

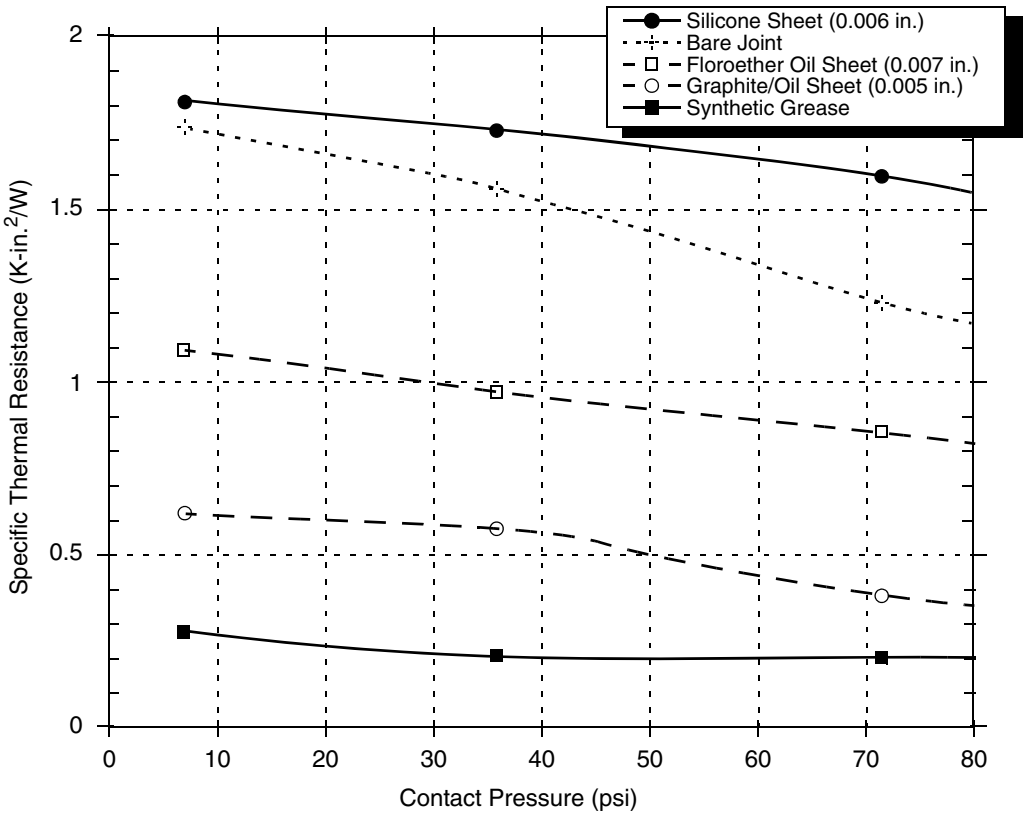


Figure 27. Thermal Performance of Select Thermal Interface Materials

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company — 800-347-4572
18930 West 78th St.
Chanhassen, MN 55317
Internet: www.bergquistcompany.com

Chomerics, Inc. — 781-935-4850
77 Dragon Ct.
Woburn, MA 01888-4014
Internet: www.chomerics.com

Dow-Corning Corporation — 800-248-2481
Dow-Corning Electronic Materials
2200 W. Salzburg Rd.
Midland, MI 48686-0997
Internet: www.dow.com

Shin-Etsu MicroSi, Inc. 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

8.8.3 Heat Sink Selection Example

This section provides a heat sink selection example using one of the commercially-available heat sinks. For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) \times P_d$$

where:

T_j is the die-junction temperature
T_a is the inlet cabinet ambient temperature
T_r is the air temperature rise within the computer cabinet
θ_{jc} is the junction-to-case thermal resistance
θ_{int} is the adhesive or interface material thermal resistance
θ_{sa} is the heat sink base-to-ambient thermal resistance
P_d is the power dissipated by the device

During operation the die-junction temperatures (T_j) should be maintained less than the value specified in Table 3. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material (θ_{int}) is typically about 1°C/W. Assuming a T_a of 30°C, a T_r of 5°C, a CBGA package $R_{\theta jc} < 0.1$, and a power consumption (P_d) of 5.0 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 1.0°C/W + \theta_{sa}) \times 5.0\ W$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{sa}) versus airflow velocity is shown in Figure 28.

Assuming an air velocity of 0.5 m/s, we have an effective R_{sa} of 7°C/W, thus

$$T_j = 30°C + 5°C + (0.1°C/W + 1.0°C/W + 7°C/W) \times 5.0\ W,$$

resulting in a die-junction temperature of approximately 76°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, The Bergquist Company, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.

Table 19. Document Revision History (continued)

Revision	Date	Substantive Change(s)
4	—	Added 450 MHz speed bin.
		Changed Table 16 to show 450 MHz part in example.
		Added row for 433 and 450 MHz core frequencies to Table 17.
		In Section 1.8.8, revised the heat sink vendor list.
		In Section 1.8.8.2, revised the interface vendor list.
3	—	Updated format and thermal resistance specifications of Table 4.
		Reformatted Tables 9, 10, 11, and 12.
		Added dimensions A3, D1, and E1 to Figures 18, 19, and 20.
		Revised Section 1.8.7 and Figure 25, removed Figure 26 and Table 19 (information now included in Figure 25).
		Reformatted Section 1.10.
		Clarified address bus and address attribute pull-up recommendations in Section 1.8.7.
		Clarified Table 2.
		Updated voltage sequencing requirements in Table 1 and removed Section 1.8.3.
2	—	1.8 V/2.0 V mode no longer supported; added 2.5 V support.
		Removed 1.8 V/2.0 V mode data from Tables 2, 3, and 6.
		Added 2.5 V mode data to Tables 2, 3, and 6.
		Extended recommended operating voltage (down to 1.8 V) for V_{DD}, AV_{DD}, and $L2AV_{DD}$ for 300 and 350 MHz parts in Table 3.
		Updated Table 7 and test conditions for power consumption specifications.
		Corrected Note 6 of Table 9 to include $\overline{\text{TLBISYNC}}$ as a mode-select signal.
		Updated AC timing specifications in Table 10.
		Updated AC timing specifications in Table 12.
		Corrected AC timing specifications in Table 13.
		Added L1_TSTCLK, L2_TSTCLK, and $\overline{\text{LSSD\_MODE}}$ pull-up requirements to Section 1.8.6.
		Corrected Figure 22.

10.2 Part Numbers Not Fully Addressed by This Document

Devices not fully addressed in this document are described in separate hardware specification addendums which supplement and supersede this document, as described in the following tables.

Table 21. Part Numbers Addressed by XPC755B*xxnnn*T*x* Series Part Numbers (Document No. MPC755ECSO1AD)

XPC	755	B	*xx*	*nnn*	T	*x*

Product Code	Part Identifier	Process Descriptor	Package	Processor Frequency	Application Modifier	Revision Level
XPC	755	B = HiP4DP	RX = CBGA	350 400	T: 2.0 V ± 100 mV –40° to 105°C	D: 2.7; PVR = 0008 3203 E: 2.8; PVR = 0008 3203
MPC	755	C=HiP4DP	RX = CBGA	350	T: 2.0 V ± 100 mV –40° to 105°C	E: 2.8; PVR = 0008 3203

Table 22. Part Numbers Addressed by XPC755B*xxnnn*LD Series Part Numbers (Document No. MPC755ECSO2AD)

XPC	*xxx*	B	*xx*	*nnn*	L	D

Product Code	Part Identifier	Process Descriptor	Package	Processor Frequency	Application Modifier	Revision Level
XPC	755 745	B = HiP4DP	PX = PBGA RX = CBGA	300 350 400	L: 2.0 V ± 100 mV 0° to 105°C	D: 2.7; PVR = 0008 3203

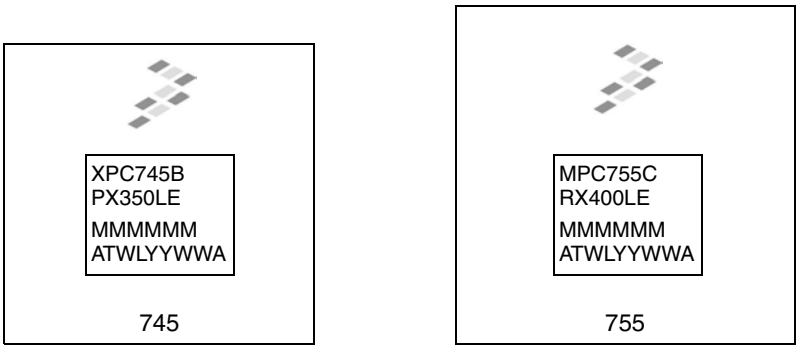
Table 23. Part Numbers Addressed by XPC755*xxxnnn*LE Series Part Numbers (Document No. MPC755ECSO3AD)

XPC	755	*x*	*xx*	*nnn*	L	E

Product Code	Part Identifier	Process Descriptor	Package	Processor Frequency	Application Modifier	Revision Level
XPC	755	B = HiP4DP	RX = CBGA	400	L: 2.0 V ± 100 mV 0° to 105°C	E: 2.8; PVR = 0008 3203
			PX = PBGA			
		C = HiP4DP	RX = CBGA	450		

10.3 Part Marking

Parts are marked as the example shown in Figure 29.



Notes:

MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 29. Part Marking for BGA Device