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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BBGA, FCBGA
Supplier Device Package	360-FCPBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc755cpx400le

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2 Features

This section summarizes features of the MPC755 implementation of the PowerPC architecture. Major features of the MPC755 are as follows:

- Branch processing unit
 - Four instructions fetched per clock
 - One branch processed per cycle (plus resolving two speculations)
 - Up to one speculative stream in execution, one additional speculative stream in fetch
 - 512-entry branch history table (BHT) for dynamic prediction
 - 64-entry, four-way set-associative branch target instruction cache (BTIC) for eliminating branch delay slots
- Dispatch unit
 - Full hardware detection of dependencies (resolved in the execution units)
 - Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point)
 - Serialization control (predispatch, postdispatch, execution serialization)
- Decode
 - Register file access
 - Forwarding control
 - Partial instruction decode
- Completion
 - Six-entry completion buffer
 - Instruction tracking and peak completion of two instructions per cycle
 - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization, and all instruction flow changes
- Fixed point units (FXUs) that share 32 GPRs for integer operands
 - Fixed Point Unit 1 (FXU1)-multiply, divide, shift, rotate, arithmetic, logical
 - Fixed Point Unit 2 (FXU2)—shift, rotate, arithmetic, logical
 - Single-cycle arithmetic, shifts, rotates, logical
 - Multiply and divide support (multi-cycle)
 - Early out multiply
- Floating-point unit and a 32-entry FPR file
 - Support for IEEE standard 754 single- and double-precision floating-point arithmetic
 - Hardware support for divide
 - Hardware support for denormalized numbers
 - Single-entry reservation station
 - Supports non-IEEE mode for time-critical operations
 - Three-cycle latency, one-cycle throughput, single-precision multiply-add



Features

- Three-cycle latency, one-cycle throughput, double-precision add
- Four-cycle latency, two-cycle throughput, double-precision multiply-add
- System unit
 - Executes CR logical instructions and miscellaneous system instructions
 - Special register transfer instructions
- Load/store unit
 - One-cycle load or store cache access (byte, half-word, word, double word)
 - Effective address generation
 - Hits under misses (one outstanding miss)
 - Single-cycle unaligned access within double-word boundary
 - Alignment, zero padding, sign extend for integer register file
 - Floating-point internal format conversion (alignment, normalization)
 - Sequencing for load/store multiples and string operations
 - Store gathering
 - Cache and TLB instructions
 - Big- and little-endian byte addressing supported
- Level 1 cache structure
 - 32K, 32-byte line, eight-way set-associative instruction cache (iL1)
 - 32K, 32-byte line, eight-way set-associative data cache (dL1)
 - Cache locking for both instruction and data caches, selectable by group of ways
 - Single-cycle cache access
 - Pseudo least-recently-used (PLRU) replacement
 - Copy-back or write-through data cache (on a page per page basis)
 - MEI data cache coherency maintained in hardware
 - Nonblocking instruction and data cache (one outstanding miss under hits)
 - No snooping of instruction cache
- Level 2 (L2) cache interface (not implemented on MPC745)
 - Internal L2 cache controller and tags; external data SRAMs
 - 256K, 512K, and 1 Mbyte two-way set-associative L2 cache support
 - Copy-back or write-through data cache (on a page basis, or for all L2)
 - Instruction-only mode and data-only mode
 - 64-byte (256K/512K) or 128-byte (1M) sectored line size
 - Supports flow through (register-buffer) synchronous BurstRAMs, pipelined (register-register) synchronous BurstRAMs (3-1-1-1 or strobeless 4-1-1-1) and pipelined (register-register) late write synchronous BurstRAMs
 - L2 configurable to cache, private memory, or split cache/private memory
 - Core-to-L2 frequency divisors of $\div 1$, $\div 1.5$, $\div 2$, $\div 2.5$, and $\div 3$ supported
 - 64-bit data bus





Figure 2 shows the allowable undershoot and overshoot voltage on the MPC755.

The MPC755 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC755 core voltage must always be provided at nominal 2.0 V (see Table 3 for actual recommended core voltage). Voltage to the L2 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 2. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL during operation. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or L2OV_{DD} power pins.

Figure 2. Overshoot/Undershoot Voltage

of t_{SYSCLK}

Table 2 describes the input threshold voltage setting.

Table 2.	Input	Threshold	Voltage Setting
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Part Revision	BVSEL Signal	Processor Bus Interface Voltage	L2VSEL Signal	L2 Bus Interface Voltage
E	0	Not Available	0	Not Available
	1	2.5 V/3.3 V	1	2.5 V/3.3 V

Caution: The input threshold selection must agree with the OV_{DD}/L2OV_{DD} voltages supplied.

Note: The input threshold settings above are different for all revisions prior to Rev. 2.8 (Rev. E). For more information, refer to Section 10.2, "Part Numbers Not Fully Addressed by This Document."

			Value			
Characteristic	Symbol	MPC755 CBGA	MPC755 PBGA	MPC745 PBGA	Unit	Notes
Junction-to-ambient thermal resistance, natural convection	$R_{ hetaJA}$	24	31	34	°C/W	1, 2
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{ hetaJMA}$	17	25	26	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{ hetaJMA}$	18	25	27	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{ hetaJMA}$	14	21	22	°C/W	1, 3
Junction-to-board thermal resistance	R_{\thetaJB}	8	17	17	°C/W	4
Junction-to-case thermal resistance	$R_{ extsf{ heta}JC}$	<0.1	<0.1	<0.1	°C/W	5

Table 4. Package Thermal Characteristics ⁶

Notes:

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

- 2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
- 3. Per JEDEC JESD51-6 with the board horizontal.
- 4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.
- 6. Refer to Section 8.8, "Thermal Management Information," for more details about thermal management.

The MPC755 incorporates a thermal management assist unit (TAU) composed of a thermal sensor, digital-to-analog converter, comparator, control logic, and dedicated special-purpose registers (SPRs). See the *MPC750 RISC Microprocessor Family User's Manual* for more information on the use of this feature. Specifications for the thermal sensor portion of the TAU are found in Table 5.



Figure 3 provides the SYSCLK input timing diagram.



VM = Midpoint Voltage (OV_{DD}/2)

Figure 3. SYSCLK Input Timing Diagram

4.2.2 **Processor Bus AC Specifications**

Table 9 provides the processor bus AC timing specifications for the MPC755 as defined in Figure 4 and Figure 6. Timing specifications for the L2 bus are provided in Section 4.2.3, "L2 Clock AC Specifications."

Table 9. Processor Bus Mode Selection AC Timing Specifications ¹

At recommended operating conditions (see Table 3)

Parameter	Symbol ²	All Spee	d Grades	Unit	Notes
Falameter	Symbol	Min	Max	Onit	
Mode select input setup to HRESET	t _{MVRH}	8	—	t _{sysclk}	3, 4, 5, 6, 7
HRESET to mode select input hold	t _{MXRH}	0	—	ns	3, 4, 6, 7, 8

Notes:

- All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 5). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
- 2. The symbology used for timing specifications herein follows the pattern of t_{(signal)(state)(reference)(state)} for inputs and t_{(reference)(state)(signal)(state)} for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK (K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH)—note the position of the reference and its state for inputs—and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
- 3. The setup and hold time is with respect to the rising edge of HRESET (see Figure 4).
- 4. This specification is for configuration mode select only. Also note that the HRESET must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
- 5. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
- 6. Mode select signals are BVSEL, L2VSEL, PLL_CFG[0:3], and TLBISYNC.
- 7. Guaranteed by design and characterization.
- 8. Bus mode select pins must remain stable during operation. Changing the logic states of BVSEL or L2VSEL during operation will cause the bus mode voltage selection to change. Changing the logic states of the PLL_CFG pins during operation will cause the PLL division ratio selection to change. Both of these conditions are considered outside the specification and are not supported. Once HRESET is negated the states of the bus mode selection pins must remain stable.



Table 11. L2CLK Output AC Timing Specification

At recommended operating conditions (see Table 3)

Baramatar	Symbol	All Spee	d Grades	Unit	Notos
Farameter	Symbol	Min	Max	Unit	Notes
L2CLK frequency	f _{L2CLK}	80	450	MHz	1, 4
L2CLK cycle time	t _{L2CLK}	2.5	12.5	ns	
L2CLK duty cycle	t _{CHCL} /t _{L2CLK}	45	55	%	2, 7
Internal DLL-relock time		640	_	L2CLK	3, 7
DLL capture window		0	10	ns	5, 7
L2CLK_OUT output-to-output skew	t _{L2CSKW}	_	50	ps	6, 7
L2CLK_OUT output jitter		—	±150	ps	6, 7

Notes:

- 1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB, L2CLK_OUT, and L2SYNC_OUT pins. The L2CLK frequency-to-core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. The maximum L2LCK frequency will be system dependent. L2CLK_OUTA and L2CLK_OUTB must have equal loading.
- 2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
- 3. The DLL-relock time is specified in terms of L2CLK periods. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in ns. Relock timing is guaranteed by design and characterization.
- 4. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz. This adds more delay to each tap of the DLL.
- 5. Allowable skew between L2SYNC_OUT and L2SYNC_IN.
- 6. This output jitter number represents the maximum delay of one tap forward or one tap back from the current DLL tap as the phase comparator seeks to minimize the phase difference between L2SYNC_IN and the internal L2CLK. This number must be comprehended in the L2 timing analysis. The input jitter on SYSCLK affects L2CLK_OUT and the L2 address/data/control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L2 timing analysis.
- 7. Guaranteed by design.

The L2CLK_OUT timing diagram is shown in Figure 7.





4.2.4 L2 Bus AC Specifications

Table 12 provides the L2 bus interface AC timing specifications for the MPC755 as defined in Figure 8 and Figure 9 for the loading conditions described in Figure 10.

Table 12. L2 Bus Interface AC Timing Specifications

At recommended operating conditions (see Table 3)

Parameter		Symbol	All Spee	II Speed Grades		Notes
	i arameter	Gymbol	Min	Мах	Onit	Notes
L2SYNC_IN rise and	fall time	t _{L2CR} , t _{L2CF}	_	1.0	ns	1
Setup times: Data and	d parity	t _{DVL2CH}	1.2	—	ns	2
Input hold times: Data and parity		t _{DXL2CH}	0	—	ns	2
Valid times:	All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	t _{l2CHOV}		3.1 3.2 3.3 3.7	ns	3, 4
Output hold times:	All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	t _{L2CHOX}	0.5 0.7 0.9 1.1	 	ns	3



Figure 12 provides the JTAG clock input timing diagram.



Figure 12. JTAG Clock Input Timing Diagram

Figure 13 provides the $\overline{\text{TRST}}$ timing diagram.



Figure 13. TRST Timing Diagram

Figure 14 provides the boundary-scan timing diagram.



Figure 14. Boundary-Scan Timing Diagram



Electrical and Thermal Characteristics

Figure 15 provides the test access port timing diagram.



Figure 15. Test Access Port Timing Diagram



Pinout Listings

Signal Name	Inal Name Pin Number		I/O	I/F Voltage ¹	Notes
INT	B15	Low	Input	OV _{DD}	
L1_TSTCLK	D11	High	Input	_	2
L2_TSTCLK	D12	High	Input	_	2
LSSD_MODE	B10	Low	Input	_	2
MCP	C13	Low	Input	OV _{DD}	
NC (No Connect)	B7, B8, C3, C6, C8, D5, D6, H4, J16, A4, A5, A2, A3, B5		_	_	
OV _{DD}	C7, E5, E7, E10, E12, G3, G5, G12, G14, K3, K5, K12, K14, M5, M7, M10, M12, P7, P10	_	—	2.5 V/3.3 V	
PLL_CFG[0:3]	A8, B9, A9, D9	High	Input	OV _{DD}	
QACK	D3	Low	Input	OV _{DD}	
QREQ	J3	Low	Output	OV _{DD}	
RSRV	D1	Low	Output	OV _{DD}	
SMI	A16	Low	Input	OV _{DD}	
SRESET	B14	Low	Input	OV _{DD}	
SYSCLK	C9	_	Input	OV _{DD}	
TA	H14	Low	Input	OV _{DD}	
TBEN	C2	High	Input	OV _{DD}	
TBST	A14	Low	I/O	OV _{DD}	
тск	C11	High	Input	OV _{DD}	
TDI	A11	High	Input	OV _{DD}	5
TDO	A12	High	Output	OV _{DD}	
TEA	H13	Low	Input	OV _{DD}	
TLBISYNC	C4	Low	Input	OV _{DD}	
TMS	B11	High	Input	OV _{DD}	5
TRST	C10	Low	Input	OV _{DD}	5
TS	J13	Low	I/O	OV _{DD}	
TSIZ[0:2]	A13, D10, B12	High	Output	OV _{DD}	
TT[0:4]	B13, A15, B16, C14, C15	High	I/O	OV _{DD}	
WT	D2	Low	Output	OV _{DD}	
V _{DD}	F6, F8, F9, F11, G7, G10, H6, H8, H9, H11, J6, J8, J9, J11, K7, K10, L6, L8, L9, L11	_		2.0 V	

Table 14. Pinout Listing for the MPC745, 255 PBGA Package (continued)



Table 15. Pinout Listing for the MPC755,	, 360 BGA Package (continued)
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Signal Name	Pin Number	Active	I/O	I/F Voltage ¹	Notes
VOLTDET	К13	High	Output	L2OV _{DD}	8

Notes:

- 1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L2 cache controls (L2CE, L2WE, and L2ZZ); L2OV_{DD} supplies power to the L2 cache interface (L2ADDR[0:16], L2DATA[0:63], L2DP[0:7], and L2SYNC_OUT) and the L2 control signals; and V_{DD} supplies power to the processor core and the PLL and DLL (after filtering to become AV_{DD} and L2AV_{DD}, respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL/L2VSEL pin configurations of Table 2 and the voltage supplied. For actual recommended value of V_{in} or supply voltages, see Table 3.
- 2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
- 3. This pin must be pulled up to OV_{DD} for proper operation of the processor interface. To allow for future I/O voltage changes, provide the option to connect BVSEL independently to either OV_{DD} or GND.
- 4. These pins are reserved for potential future use as additional L2 address pins.
- 5. Uses one of nine existing no connects in the MPC750, 360 BGA package.
- 6. Internal pull-up on die.
- 7. This pin must be pulled up to L2OV_{DD} for proper operation of the processor interface. To allow for future I/O voltage changes, provide the option to connect L2VSEL independently to either L2OV_{DD} or GND.
- Internally tied to L2OV_{DD} in the MPC755, 360 BGA package to indicate the power present at the L2 cache interface. This signal is not a power supply input.

Caution: This differs from the MPC745, 255 BGA package.

7 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC745, 255 PBGA package, as well as the MPC755, 360 CBGA and PBGA packages. While both the MPC755 plastic and ceramic packages are described here, both packages are not guaranteed to be available at the same time. All new designs should allow for either ceramic or plastic BGA packages for this device. For more information on designing a common footprint for both plastic and ceramic package types, see the *Freescale Flip-Chip Plastic Ball Grid Array Presentation*. The MPC755 was initially sampled in a CBGA package, but production units are currently provided in both a CBGA and a PBGA package. Because of the better long-term device-to-board interconnect reliability of the PBGA package, Freescale recommends use of a PBGA package except where circumstances dictate use of a CBGA package.



8 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC755.

8.1 PLL Configuration

The MPC755 PLL is configured by the PLL_CFG[0:3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. These must be chosen such that they comply with Table 8. Table 16 shows the valid configurations of these signals and an example illustrating the core and VCO frequencies resulting from various PLL configurations and example bus frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the 400-MHz column in Table 8.

	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)									
PLL_CFG [0:3]	Bus-to- Core Multiplier	Core-to- VCO Multiplier	Bus 33 MHz	Bus 50 MHz	Bus 66 MHz	Bus 75 MHz	Bus 80 MHz	Bus 100 MHz		
0100	2x	2x	—	—	—	—	—	200 (400)		
1000	Зx	2x	—	—	200 (400)	225 (450)	240 (480)	300 (600)		
1110	3.5x	2x	—	—	233 (466)	263 (525)	280 (560)	350 (700)		
1010	4x	2x	_	200 (400)	266 (533)	300 (600)	320 (640)	400 (800)		
0111	4.5x	2x	—	225 (450)	300 (600)	338 (675)	360 (720)	—		
1011	5x	2x	—	250 (500)	333 (666)	375 (750)	400 (800)	—		
1001	5.5x	2x	—	275 (550)	366 (733)	—	—	—		
1101	6x	2x	200 (400)	300 (600)	400 (800)	—	—	—		
0101	6.5x	2x	216 (433)	325 (650)	—	—	—	—		
0010	7x	2x	233 (466)	350 (700)	—	—	—	—		
0001	7.5x	2x	250 (500)	375 (750)	—	—	—	—		
1100	8x	2x	266 (533)	400 (800)	—	—	—	—		
0110	10x	2x	333 (666)	—	—	—	—	—		

Table 16. MPC755 Microprocessor PLL Configuration Example for 400 MHz Parts

Core Frequency (MHz)	÷1	÷1.5	÷2	÷2.5	÷3
375	375	250	188	150	125
400	400	266	200	160	133

Table 17. Sample Core-to-L2 Frequencies (continued)

Note: The core and L2 frequencies are for reference only. Some examples may represent core or L2 frequencies which are not useful, not supported, or not tested for by the MPC755; see Section 4.2.3, "L2 Clock AC Specifications," for valid L2CLK frequencies. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz.

8.2 PLL Power Supply Filtering

The AV_{DD} and $L2AV_{DD}$ power signals are provided on the MPC755 to provide power to the clock generation PLL and L2 cache DLL, respectively. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 21 using surface mount capacitors with minimum Effective Series Inductance (ESL) is recommended. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. An identical but separate circuit should be placed as close as possible to the $L2AV_{DD}$ pin. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 BGA footprint, without the inductance of vias. The $L2AV_{DD}$ pin may be more difficult to route, but is proportionately less critical.

Figure 21 shows the PLL power supply filter circuit.



Figure 21. PLL Power Supply Filter Circuit

8.3 Decoupling Recommendations

Due to the MPC755 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC755 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC755 system, and the MPC755 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , OV_{DD} , and $L2OV_{DD}$ pin of the MPC755. It is also recommended that these decoupling capacitors receive their power from separate V_{DD} , $(L2)OV_{DD}$, and GND power planes in the PCB, utilizing short traces to minimize inductance.



should be left unconnected by the system. If all parity generation is disabled through HID0, then all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

The L2 interface does not require pull-up resistors.

8.7 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the TRST signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying TRST to HRESET is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 24 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0- Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted ensuring that the JTAG scan chain is initialized during power-on. While Freescale recommends that the COP header be designed into the system as shown in Figure 24, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 24 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

System Design Information



Notes:

- 1. RUN/STOP, normally found on pin 5 of the COP header, is not implemented on the MPC755. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
- 2. Key location; pin 14 is not physically present on the COP header.
- 3. Component not populated. Populate only if debug tool does not drive QACK.
- 4. Populate only if debug tool uses an open-drain type output and does not actively deassert QACK.
- 5. If the JTAG interface is implemented, connect HRESET from the target source to TRST from the COP header though an AND gate to TRST of the part. If the JTAG interface is not implemented, connect HRESET from the target source to TRST of the part through a 0-Ω isolation resistor.
- 6. The COP port and target board should be able to independently assert HRESET and TRST to the processor in order to fully control the processor as shown above.

Figure 24. JTAG Interface Connection





Figure 27. Thermal Performance of Select Thermal Interface Materials

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company	800-347-4572
18930 West 78 th St.	
Chanhassen, MN 55317	
Internet: www.bergquistcompany.com	
Chomerics, Inc.	781-935-4850
77 Dragon Ct.	
Woburn, MA 01888-4014	
Internet: www.chomerics.com	
Dow-Corning Corporation	800-248-2481
Dow-Corning Electronic Materials	
2200 W. Salzburg Rd.	
Midland, MI 48686-0997	
Internet: www.dow.com	



Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com

Thermagon Inc. 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.thermagon.com 888-642-7674

888-246-9050

8.8.3 Heat Sink Selection Example

This section provides a heat sink selection example using one of the commercially-available heat sinks. For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_i = T_a + T_r + (\theta_{ic} + \theta_{int} + \theta_{sa}) \times P_d$$

where:

T_i is the die-junction temperature

T_a is the inlet cabinet ambient temperature

 T_r is the air temperature rise within the computer cabinet

 θ_{ic} is the junction-to-case thermal resistance

 θ_{int} is the adhesive or interface material thermal resistance

 θ_{sa} is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation the die-junction temperatures (T_j) should be maintained less than the value specified in Table 3. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material (θ_{int}) is typically about 1°C/W. Assuming a T_a of 30°C, a T_r of 5°C, a CBGA package $R_{\theta jc} < 0.1$, and a power consumption (P_d) of 5.0 W, the following expression for T_j is obtained:

Die-junction temperature: $T_i = 30^{\circ}C + 5^{\circ}C + (0.1^{\circ}C/W + 1.0^{\circ}C/W + \theta_{sa}) \times 5.0 W$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{sa}) versus airflow velocity is shown in Figure 28.

Assuming an air velocity of 0.5 m/s, we have an effective R_{sa} of 7°C/W, thus

 $T_i = 30^{\circ}C + 5^{\circ}C + (0.1^{\circ}C/W + 1.0^{\circ}C/W + 7^{\circ}C/W) \times 5.0 W,$

resulting in a die-junction temperature of approximately 76°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, The Bergquist Company, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.



Document Revision History

9 Document Revision History

Table 19 provides a revision history for this hardware specification.

Table 13. Document nevision mistory	Table	19.	Document	Revision	History
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Revision	Date	Substantive Change(s)					
8	2/8/2006	Changed processor descriptor from 'B' to 'C' for 350 MHz devices and increased power specifications for full-power mode in Table 7.					
7	4/05/2005	Removed phrase "for the ceramic ball grid array (CBGA) package" from Section 8.8; this information applies to devices in both CBGA and PBGA packages.					
		Figure 24—updated COP Connector Diagram to recommend a weak pull-up resistor on TCK.					
		Table 20—added MPC745BPXLE, MPC755BRXLE, MPC755BPXLE, MPC755CVTLE, MPC755BVTLE and MPC745BVTLE part numbers. These devices are fully addressed by this document.					
		Corrected Revision Level in Table 23: Rev E devices are Rev 2.8, not 2.7.					
		Added MPC755CRX400LE and MPC755CPX400LE to devices supported by this specification in Table 20.					
		Removed "Advance Information" from title block on page 1.					
6.1	1/21/2005	Updated document template.					
6	—	Removed 450 MHz speed grade throughout document. These devices are no longer supported for new designs; see Section 1.10.2 for more information.					
		Relaxed voltage sequencing requirements in Notes 3 and 4 of Table 1.					
		Corrected Note 2 of Table 7.					
		Changed processor descriptor from 'B' to 'C' for 400 MHz devices and increased power specifications for full-power mode in Table 7. XPC755Bxx400LE devices are no longer produced and are documented in a separate part number specification; see Section 1.10.2 for more information.					
		Increased power specifications for sleep mode for all speed grades in Table 7.					
		Removed 'Sleep Mode (PLL and DLL Disabled)—Typical' specification from Table 7; this is no longer tested or characterized.					
		Added Note 4 to Table 7.					
		Revised L2 clock duty cycle specification in Table 11 and changed Note 7.					
		Corrected Note 3 in Table 20.					
		Replaced Table 21 and added Tables 22 and 23.					
5	—	Added Note 6 to Table 10; clarification only as this information is already documented in the MPC750 RISC Microprocessor Family User's Manual.					
		Revised Figure 24 and Section 1.8.7.					
		Corrected Process Identifier for 450 MHz part in Table 20.					
		Added XPC755BRX <i>nnn</i> T <i>x</i> series to Table 21.					





10 Ordering Information

Ordering information for the devices fully covered by this specification document is provided in Section 10.1, "Part Numbers Fully Addressed by This Document." Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number. Section 10.2, "Part Numbers Not Fully Addressed by This Document," lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specifications addendum.

10.1 Part Numbers Fully Addressed by This Document

Table 20 provides the Freescale part numbering nomenclature for the MPC755 and MPC745 devices fully addressed by this document.

MPC	XXX	X	XX	nnn	X	X
Product Code	Part Identifier	Process Descriptor	Package ¹	Processor Frequency	Application Modifier	Revision Level
XPC ²	755 745	B = HiP4DP	PX = PBGA RX = CBGA	300 350	L: 2.0 V ± 100 mV 0° to 105°C	E: 2.8; PVR = 0008 3203
	755	C = HiP4DP		400		
MPC	755	B = HiP4DP		300 350		
		C = HiP4DP		350 400		
	745	B = HiP4DP	PX = PBGA	300 350		
	745	C = HiP4DP	PX = PBGA VT = PBGAPb- free BGA	350		
	755 745	B = HiP4DP	VT = PBGAPb- free BGA	300 350		
	755	C = HiP4DP		350 400		

Table 20. Part Numbering Nomenclature

Notes:

1. See Section 7, "Package Description," for more information on available package types.

2. The X prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These are from a limited production volume of prototypes manufactured, tested, and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes



Ordering Information

10.2 Part Numbers Not Fully Addressed by This Document

Devices not fully addressed in this document are described in separate hardware specification addendums which supplement and supersede this document, as described in the following tables.

Table 21. Part Numbers Addressed by XPC755BxxnnnTx Series Part Numbers (Document No. MPC755ECS01AD)

XPC	755	В	XX	nnn	т	X
Product Code	Part Identifier	Process Descriptor	Package	Processor Frequency	Application Modifier	Revision Level
XPC	755	B = HiP4DP	RX = CBGA	350 400	T: 2.0 V ± 100 mV −40° to 105°C	D: 2.7; PVR = 0008 3203 E: 2.8; PVR = 0008 3203
MPC	755	C=HiP4DP	RX = CBGA	350	T: 2.0 V ± 100 mV -40° to 105°C	E: 2.8; PVR = 0008 3203

Table 22. Part Numbers Addressed by XPC755BxxnnnLD Series Part Numbers (Document No. MPC755ECS02AD)

XPC	XXX	В	XX	nnn	L	D
Product Code	Part Identifier	Process Descriptor	Package	Processor Frequency	Application Modifier	Revision Level
XPC	755 745	B = HiP4DP	PX = PBGA RX = CBGA	300 350 400	L: 2.0 V ± 100 mV 0° to 105°C	D: 2.7; PVR = 0008 3203

Table 23. Part Numbers Addressed by XPC755xxxnnnLE Series Part Numbers (Document No. MPC755ECSO3AD)

XPC	755	X	XX	nnn	L	E
Product Code	Part Identifier	Process Descriptor	Package	Processor Frequency	Application Modifier	Revision Level
XPC	755	B = HiP4DP	RX = CBGA	400	L: $2.0 V \pm 100 mV$	E: 2.8; PVR = 0008 3203
			PX = PBGA	(= PBGA	0° to 105°C	
		C = HiP4DP	RX = CBGA	450		