Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	350MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-CBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc755crx350le

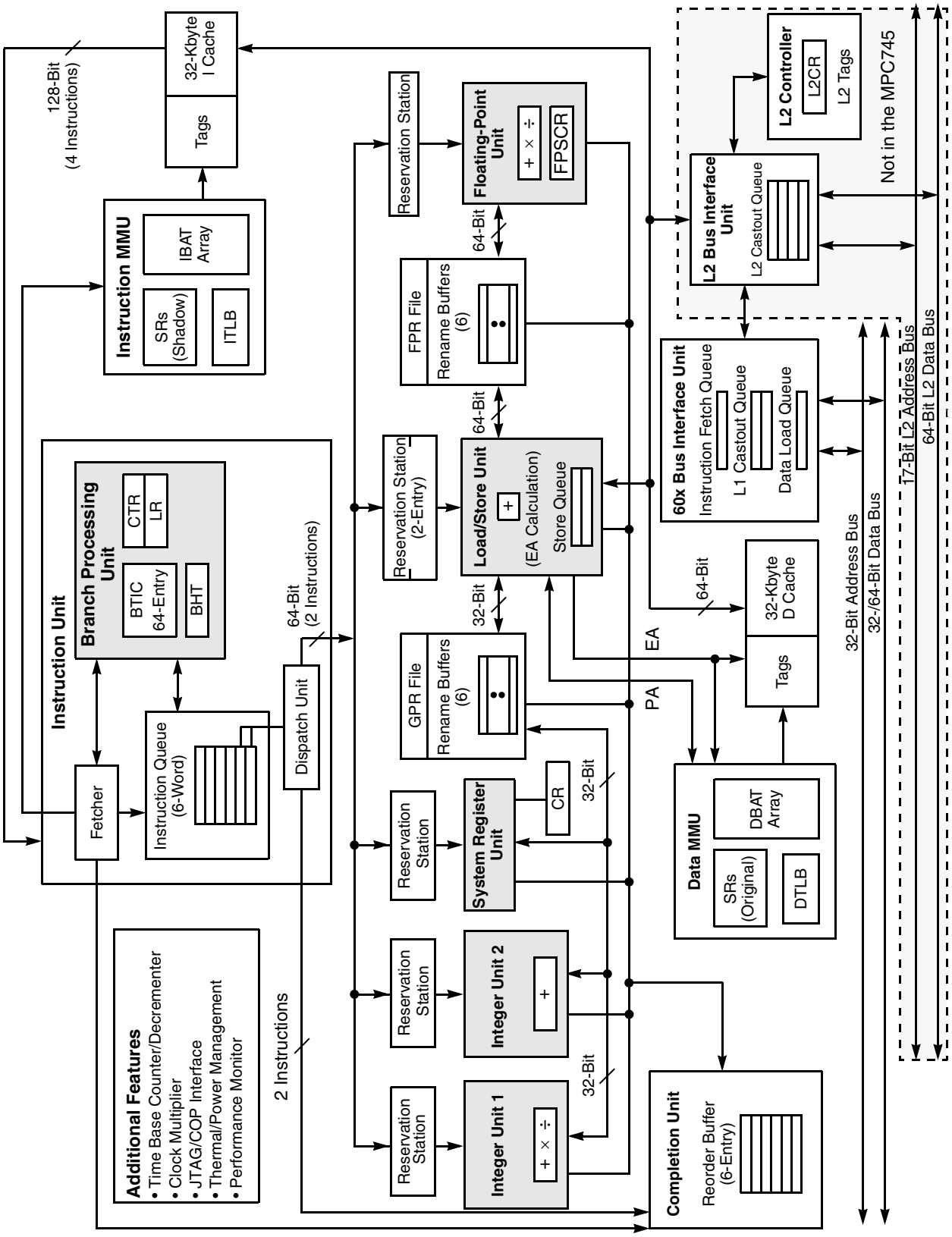


Figure 1. MPC755 Block Diagram

Packages	MPC745: Surface mount 255 plastic ball grid array (PBGA) MPC755: Surface mount 360 ceramic ball grid array (CBGA) Surface mount 360 plastic ball grid array (PBGA)
Core power supply	2.0 V ± 100 mV DC (nominal; some parts support core voltages down to 1.8 V; see Table 3 for recommended operating conditions)
I/O power supply	2.5 V ± 100 mV DC or 3.3 V ± 165 mV DC (input thresholds are configuration pin selectable)

4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC755.

4.1 DC Electrical Characteristics

Table 1 through Table 7 describe the MPC755 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Maximum Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 2.5	V	4
PLL supply voltage		AV_{DD}	–0.3 to 2.5	V	4
L2 DLL supply voltage		$L2AV_{DD}$	–0.3 to 2.5	V	4
Processor bus supply voltage		OV_{DD}	–0.3 to 3.6	V	3
L2 bus supply voltage		$L2OV_{DD}$	–0.3 to 3.6	V	3
Input voltage	Processor bus	V_{in}	–0.3 to OV_{DD} + 0.3 V	V	2, 5
	L2 bus	V_{in}	–0.3 to $L2OV_{DD}$ + 0.3 V	V	2, 5
	JTAG signals	V_{in}	–0.3 to 3.6	V	
Storage temperature range		T_{stg}	–55 to 150	°C	

Notes:

1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** V_{in} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.3 V at any time including during power-on reset.
3. **Caution:** $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 1.6 V during normal operation. During power-on reset and power-down sequences, $L2OV_{DD}/OV_{DD}$ may exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by up to 3.3 V for up to 20 ms, or by 2.5 V for up to 40 ms. Excursions beyond 3.3 V or 40 ms are not supported.
4. **Caution:** $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4 V during normal operation. During power-on reset and power-down sequences, $V_{DD}/AV_{DD}/L2AV_{DD}$ may exceed $L2OV_{DD}/OV_{DD}$ by up to 1.0 V for up to 20 ms, or by 0.7 V for up to 40 ms. Excursions beyond 1.0 V or 40 ms are not supported.
5. This is a DC specifications only. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

Figure 2 shows the allowable undershoot and overshoot voltage on the MPC755.

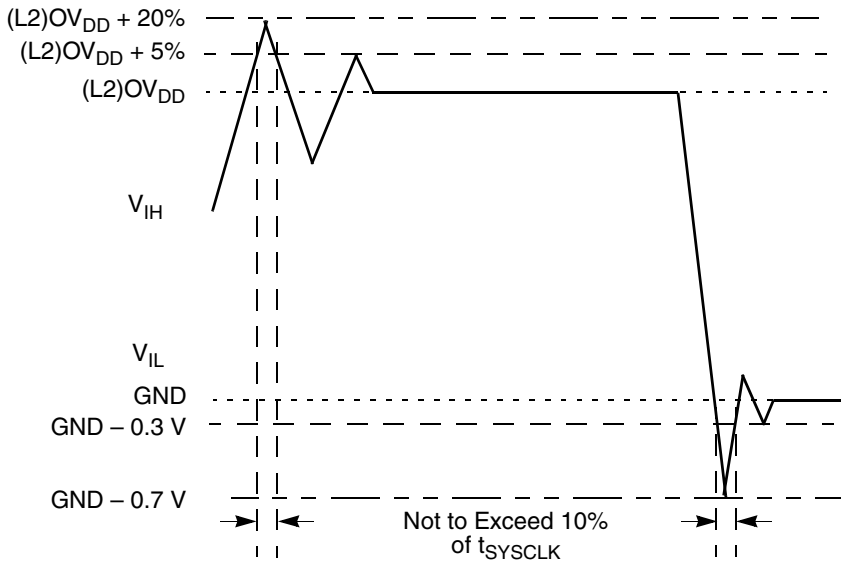


Figure 2. Overshoot/Undershoot Voltage

The MPC755 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC755 core voltage must always be provided at nominal 2.0 V (see Table 3 for actual recommended core voltage). Voltage to the L2 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 2. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL during operation. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

Table 2 describes the input threshold voltage setting.

Table 2. Input Threshold Voltage Setting

Part Revision	BVSEL Signal	Processor Bus Interface Voltage	L2VSEL Signal	L2 Bus Interface Voltage
E	0	Not Available	0	Not Available
	1	2.5 V/3.3 V	1	2.5 V/3.3 V

Caution: The input threshold selection must agree with the OV_{DD}/$L2OV_{DD}$ voltages supplied.

Note: The input threshold settings above are different for all revisions prior to Rev. 2.8 (Rev. E). For more information, refer to Section 10.2, "Part Numbers Not Fully Addressed by This Document."

Table 3 provides the recommended operating conditions for the MPC755.

Table 3. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value				Unit	Notes
			300 MHz, 350 MHz		400 MHz			
			Min	Max	Min	Max		
Core supply voltage		V_{DD}	1.80	2.10	1.90	2.10	V	3
PLL supply voltage		AV_{DD}	1.80	2.10	1.90	2.10	V	3
L2 DLL supply voltage		$L2AV_{DD}$	1.80	2.10	1.90	2.10	V	3
Processor bus supply voltage	BVSEL = 1	OV_{DD}	2.375	2.625	2.375	2.625	V	2, 4
			3.135	3.465	3.135	3.465		5
L2 bus supply voltage	L2VSEL = 1	$L2OV_{DD}$	2.375	2.625	2.375	2.625	V	2, 4
			3.135	3.465	3.135	3.465		5
Input voltage	Processor bus	V_{in}	GND	OV_{DD}	GND	OV_{DD}	V	
	L2 bus	V_{in}	GND	$L2OV_{DD}$	GND	$L2OV_{DD}$	V	
	JTAG signals	V_{in}	GND	OV_{DD}	GND	OV_{DD}	V	
Die-junction temperature		T_j	0	105	0	105	°C	

Notes:

1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. Revisions prior to Rev. 2.8 (Rev. E) offered different I/O voltage support. For more information, refer to Section 10.2, “Part Numbers Not Fully Addressed by This Document.”
3. 2.0 V nominal.
4. 2.5 V nominal.
5. 3.3 V nominal.

Table 4 provides the package thermal characteristics for the MPC755 and MPC745. The MPC755 was initially sampled in a CBGA package, but production units are currently provided in both a CBGA and a PBGA package. Because of the better long-term device-to-board interconnect reliability of the PBGA package, Freescale recommends use of a PBGA package except where circumstances dictate use of a CBGA package. The MPC745 is offered in a PBGA package only.

Table 4. Package Thermal Characteristics [6]

Characteristic	Symbol	Value			Unit	Notes
		MPC755 CBGA	MPC755 PBGA	MPC745 PBGA		
Junction-to-ambient thermal resistance, natural convection	$R_{\theta JA}$	24	31	34	°C/W	1, 2
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JMA}$	17	25	26	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	18	25	27	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	14	21	22	°C/W	1, 3
Junction-to-board thermal resistance	$R_{\theta JB}$	8	17	17	°C/W	4
Junction-to-case thermal resistance	$R_{\theta JC}$	<0.1	<0.1	<0.1	°C/W	5

Notes:

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.
6. Refer to Section 8.8, "Thermal Management Information," for more details about thermal management.

The MPC755 incorporates a thermal management assist unit (TAU) composed of a thermal sensor, digital-to-analog converter, comparator, control logic, and dedicated special-purpose registers (SPRs). See the *MPC750 RISC Microprocessor Family User's Manual* for more information on the use of this feature. Specifications for the thermal sensor portion of the TAU are found in Table 5.

Table 5. Thermal Sensor Specifications

At recommended operating conditions (see Table 3)

Characteristic	Min	Max	Unit	Notes
Temperature range	0	127	°C	1
Comparator settling time	20	—	µs	2, 3
Resolution	4	—	°C	3
Accuracy	–12	+12	°C	3

Notes:

1. The temperature is the junction temperature of the die. The thermal assist unit's raw output does not indicate an absolute temperature, but must be interpreted by software to derive the absolute junction temperature. For information about the use and calibration of the TAU, see Freescale Application Note AN1800/D, *Programming the Thermal Assist Unit in the MPC750 Microprocessor.*
2. The comparator settling time value must be converted into the number of CPU clocks that need to be written into the THRM3 SPR.
3. Guaranteed by design and characterization.

Table 6 provides the DC electrical characteristics for the MPC755.

Table 6. DC Electrical Specifications

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage [1]	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs except SYSCLK)	2.5	V_{IH}	1.6	(L2)OV_{DD} + 0.3	V	2, 3
	3.3	V_{IH}	2.0	(L2)OV_{DD} + 0.3	V	2, 3
Input low voltage (all inputs except SYSCLK)	2.5	V_{IL}	–0.3	0.6	V	2
	3.3	V_{IL}	–0.3	0.8	V	
SYSCLK input high voltage	2.5	KV_{IH}	1.8	OV_{DD} + 0.3	V	
	3.3	KV_{IH}	2.4	OV_{DD} + 0.3	V	
SYSCLK input low voltage	2.5	KV_{IL}	–0.3	0.4	V	
	3.3	KV_{IL}	–0.3	0.4	V	
Input leakage current, V_{in} = L2OV_{DD}/OV_{DD}		I_{in}	—	10	µA	2, 3
High-Z (off-state) leakage current, V_{in} = L2OV_{DD}/OV_{DD}		I_{TSI}	—	10	µA	2, 3, 5
Output high voltage, I_{OH} = –6 mA	2.5	V_{OH}	1.7	—	V	
	3.3	V_{OH}	2.4	—	V	
Output low voltage, I_{OL} = 6 mA	2.5	V_{OL}	—	0.45	V	
	3.3	V_{OL}	—	0.4	V	

4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC755. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section 4.2.1, "Clock AC Specifications," and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:3] signals. Parts are sold by maximum processor core frequency; see Section 10, "Ordering Information."

4.2.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications as defined in Figure 3.

Table 8. Clock AC Timing Specifications

At recommended operating conditions (see Table 3)

Characteristic	Symbol	Maximum Processor Core Frequency						Unit	Notes
		300 MHz		350 MHz		400 MHz			
		Min	Max	Min	Max	Min	Max		
Processor frequency	f_{core}	200	300	200	350	200	400	MHz	1
VCO frequency	f_{VCO}	400	600	400	700	400	800	MHz	1
SYSCLK frequency	f_{SYSCLK}	25	100	25	100	25	100	MHz	1
SYSCLK cycle time	t_{SYSCLK}	10	40	10	40	10	40	ns	
SYSCLK rise and fall time	t_{KR}, t_{KF}	—	2.0	—	2.0	—	2.0	ns	2
	t_{KR}, t_{KF}	—	1.4	—	1.4	—	1.4	ns	2
SYSCLK duty cycle measured at $OV_{DD}/2$	t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	%	3
SYSCLK jitter		—	±150	—	±150	—	±150	ps	3, 4
Internal PLL relock time		—	100	—	100	—	100	μs	3, 5

Notes:

1. **Caution:** The SYSCLK frequency and PLL_CFG[0:3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:3] signal description in Section 8.1, "PLL Configuration," for valid PLL_CFG[0:3] settings.
2. Rise and fall times measurements are now specified in terms of slew rates, rather than time to account for selectable I/O bus interface levels. The minimum slew rate of 1 V/ns is equivalent to a 2 ns maximum rise/fall time measured at 0.4 and 2.4 V (OV_{DD} = 3.3 V) or a rise/fall time of 1 ns measured at 0.4 and 1.8 V (OV_{DD} = 2.5 V).
3. Timing is guaranteed by design and characterization.
4. This represents total input jitter—short term and long term combined—and is guaranteed by design.
5. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 3 provides the SYSCLK input timing diagram.

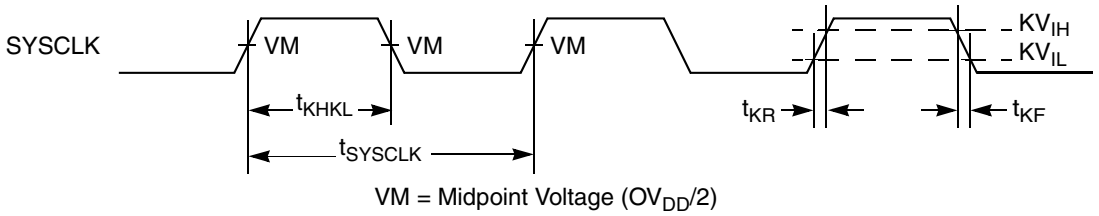


Figure 3. SYSCLK Input Timing Diagram

4.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC755 as defined in Figure 4 and Figure 6. Timing specifications for the L2 bus are provided in Section 4.2.3, "L2 Clock AC Specifications."

Table 9. Processor Bus Mode Selection AC Timing Specifications [1]

At recommended operating conditions (see Table 3)

Parameter	Symbol [2]	All Speed Grades		Unit	Notes
		Min	Max		
Mode select input setup to $\overline{\text{HRESET}}$	t_{MVRH}	8	—	t_{sysclk}	3, 4, 5, 6, 7
$\overline{\text{HRESET}}$ to mode select input hold	t_{MXRH}	0	—	ns	3, 4, 6, 7, 8

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 5). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK (K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH)—note the position of the reference and its state for inputs—and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 4).
4. This specification is for configuration mode select only. Also note that the $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
5. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
6. Mode select signals are BVSEL, L2VSEL, PLL_CFG[0:3], and $\overline{\text{TLBISYNC}}$.
7. Guaranteed by design and characterization.
8. Bus mode select pins must remain stable during operation. Changing the logic states of BVSEL or L2VSEL during operation will cause the bus mode voltage selection to change. Changing the logic states of the PLL_CFG pins during operation will cause the PLL division ratio selection to change. Both of these conditions are considered outside the specification and are not supported. Once $\overline{\text{HRESET}}$ is negated the states of the bus mode selection pins must remain stable.

Table 10. Processor Bus AC Timing Specifications [1]

At recommended operating conditions (see Table 3)

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
Setup times: All inputs	t_{IVKH}	2.5	—	ns	
Input hold times: $\overline{\text{TLBISYNC}}$, $\overline{\text{MCP}}$, $\overline{\text{SMI}}$	t_{IXKH}	0.6	—	ns	6
Input hold times: All inputs, except $\overline{\text{TLBISYNC}}$, $\overline{\text{MCP}}$, $\overline{\text{SMI}}$	t_{IXKH}	0.2	—	ns	6
Valid times: All outputs	t_{KHOV}	—	4.1	ns	
Output hold times: All outputs	t_{KHOX}	1.0	—	ns	
SYSCLK to output enable	t_{KHOE}	0.5	—	ns	2
SYSCLK to output high impedance (all except $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$)	t_{KHOZ}	—	6.0	ns	2
SYSCLK to $\overline{\text{ABB}}$, $\overline{\text{DBB}}$ high impedance after precharge	t_{KHABPZ}	—	1.0	t_{sysclk}	2, 3, 4
Maximum delay to $\overline{\text{ARTRY}}$ precharge	t_{KHARP}	—	1	t_{sysclk}	2, 3, 5
SYSCLK to $\overline{\text{ARTRY}}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{sysclk}	2, 3, 5

Notes:

1. Revisions prior to Rev. 2.8 (Rev. E) were limited in performance and did not conform to this specification. For more information, refer to Section 10.2, "Part Numbers Not Fully Addressed by This Document."
2. Guaranteed by design and characterization.
3. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. Per the 60x bus protocol, $\overline{\text{TS}}$, $\overline{\text{ABB}}$, and $\overline{\text{DBB}}$ are driven only by the currently active bus master. They are asserted low, then precharged high before returning to high-Z as shown in Figure 6. The nominal precharge width for $\overline{\text{TS}}$, $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ is $0.5 \times t_{sysclk}$, that is, less than the minimum t_{sysclk} period, to ensure that another master asserting $\overline{\text{TS}}$, $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
5. Per the 60x bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue since any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{sysclk}; that is, it should be high-Z as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z and precharge behavior is guaranteed by design.
6. $\overline{\text{MCP}}$ and $\overline{\text{SRESET}}$ must be held asserted for a minimum of two bus clock cycles; $\overline{\text{INT}}$ and $\overline{\text{SMI}}$ should be held asserted until the exception is taken; $\overline{\text{CKSTP\_IN}}$ must be held asserted until the system has been reset. See the *MPC750 RISC Microprocessor Family User's Manual* for more information.

SRAM. Note that revisions of the MPC755 prior to Rev. 2.8 (Rev. E) were limited in performance, and were typically limited to 175 MHz with similarly-rated SRAM. For more information, see Section 10.2, “Part Numbers Not Fully Addressed by This Document.”

Freescale is similarly limited by system constraints and cannot perform tests of the L2 interface on a socketed part on a functional tester at the maximum frequencies of Table 11. Therefore, functional operation and AC timing information are tested at core-to-L2 divisors of 2 or greater. Functionality of core-to-L2 divisors of 1 or 1.5 is verified at less than maximum rated frequencies.

L2 input and output signals are latched or enabled, respectively, by the internal L2CLK (which is SYSCLK multiplied up to the core frequency and divided down to the L2CLK frequency). In other words, the AC timings of Table 12 and Table 13 are entirely independent of L2SYNC_IN. In a closed loop system, where L2SYNC_IN is driven through the board trace by L2SYNC_OUT, L2SYNC_IN only controls the output phase of L2CLK_OUTA and L2CLK_OUTB which are used to latch or enable data at the SRAMs. However, since in a closed loop system L2SYNC_IN is held in phase alignment with the internal L2CLK, the signals of Table 12 and Table 13 are referenced to this signal rather than the not-externally-visible internal L2CLK. During manufacturing test, these times are actually measured relative to SYSCLK.

The L2SYNC_OUT signal is intended to be routed halfway out to the SRAMs and then returned to the L2SYNC_IN input of the MPC755 to synchronize L2CLK_OUT at the SRAM with the processor’s internal clock. L2CLK_OUT at the SRAM can be offset forward or backward in time by shortening or lengthening the routing of L2SYNC_OUT to L2SYNC_IN. See Freescale Application Note AN1794/D, *Backside L2 Timing Analysis for PCB Design Engineers*.

The L2CLK_OUTA and L2CLK_OUTB signals should not have more than two loads.

Table 11. L2CLK Output AC Timing Specification

At recommended operating conditions (see Table 3)

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
L2CLK frequency	f_{L2CLK}	80	450	MHz	1, 4
L2CLK cycle time	t_{L2CLK}	2.5	12.5	ns	
L2CLK duty cycle	t_{CHCL}/t_{L2CLK}	45	55	%	2, 7
Internal DLL-relock time		640	—	L2CLK	3, 7
DLL capture window		0	10	ns	5, 7
L2CLK_OUT output-to-output skew	t_{L2CSKW}	—	50	ps	6, 7
L2CLK_OUT output jitter		—	±150	ps	6, 7

Notes:

1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB, L2CLK_OUT, and L2SYNC_OUT pins. The L2CLK frequency-to-core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. The maximum L2LCK frequency will be system dependent. L2CLK_OUTA and L2CLK_OUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The DLL-relock time is specified in terms of L2CLK periods. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in ns. Relock timing is guaranteed by design and characterization.
4. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz. This adds more delay to each tap of the DLL.
5. Allowable skew between L2SYNC_OUT and L2SYNC_IN.
6. This output jitter number represents the maximum delay of one tap forward or one tap back from the current DLL tap as the phase comparator seeks to minimize the phase difference between L2SYNC_IN and the internal L2CLK. This number must be comprehended in the L2 timing analysis. The input jitter on SYSCLK affects L2CLK_OUT and the L2 address/data/control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L2 timing analysis.
7. Guaranteed by design.

4.2.5 IEEE 1149.1 AC Timing Specifications

Table 13 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 12 through Figure 15.

Table 13. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions (see Table 3)

Parameter		Symbol	Min	Max	Unit	Notes
TCK frequency of operation		f_{TCLK}	0	16	MHz	
TCK cycle time		t_{TCLK}	62.5	—	ns	
TCK clock pulse width measured at 1.4 V		t_{JHJL}	31	—	ns	
TCK rise and fall times		t_{JR}, t_{JF}	0	2	ns	
$\overline{\text{TRST}}$ assert time		t_{TRST}	25	—	ns	2
Input setup times:	Boundary-scan data TMS, TDI	t_{DVJH} t_{IVJH}	4 0	— —	ns	3
Input hold times:	Boundary-scan data TMS, TDI	t_{DXJH} t_{IXJH}	15 12	— —	ns	3
Valid times:	Boundary-scan data TDO	t_{JLDV} t_{JLOV}	— —	4 4	ns	4
Output hold times:	Boundary-scan data TDO	t_{JLDH} t_{JLOH}	25 12	— —	ns	4
TCK to output high impedance:	Boundary-scan data TDO	t_{JLDZ} t_{JLOZ}	3 3	19 9	ns	4, 5

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 11). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal which must be asserted for this minimum time to be recognized.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 11 provides the AC test load for TDO and the boundary-scan outputs of the MPC755.

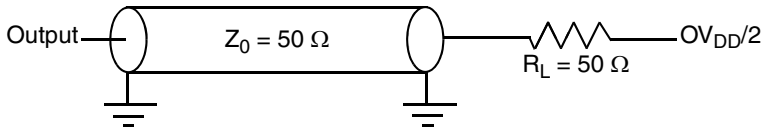


Figure 11. AC Test Load for the JTAG Interface

Table 14. Pinout Listing for the MPC745, 255 PBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
VOLTDET	F3	High	Output	—	6

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals; and V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL pin configuration of Table 2 and the voltage supplied. For actual recommended value of V_{in} or supply voltages, see Table 3.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. This pin must be pulled up to OV_{DD} for proper operation of the processor interface. To allow for future I/O voltage changes, provide the option to connect BVSEL independently to either OV_{DD} or GND.
4. Uses 1 of 15 existing no connects in the MPC740, 255 BGA package.
5. Internal pull-up on die.
6. Internally tied to GND in the MPC745, 255 BGA package to indicate to the power supply that a low-voltage processor is present. This signal is not a power supply input.

   Caution: This differs from the MPC755, 360 BGA package.

Table 15 provides the pinout listing for the MPC755, 360 PBGA and CBGA packages.

Table 15. Pinout Listing for the MPC755, 360 BGA Package

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
A[0:31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O	OV_{DD}	
$\overline{\text{AACK}}$	N3	Low	Input	OV_{DD}	
$\overline{\text{ABB}}$	L7	Low	I/O	OV_{DD}	
AP[0:3]	C4, C5, C6, C7	High	I/O	OV_{DD}	
$\overline{\text{ARTRY}}$	L6	Low	I/O	OV_{DD}	
AV_{DD}	A8	—	—	2.0 V	
$\overline{\text{BG}}$	H1	Low	Input	OV_{DD}	
$\overline{\text{BR}}$	E7	Low	Output	OV_{DD}	
BVSEL	W1	High	Input	OV_{DD}	3, 5, 6
$\overline{\text{CI}}$	C2	Low	Output	OV_{DD}	
$\overline{\text{CKSTP\_IN}}$	B8	Low	Input	OV_{DD}	
$\overline{\text{CKSTP\_OUT}}$	D7	Low	Output	OV_{DD}	
CLK_OUT	E3	—	Output	OV_{DD}	
$\overline{\text{DBB}}$	K5	Low	I/O	OV_{DD}	
$\overline{\text{DBDIS}}$	G1	Low	Input	OV_{DD}	
$\overline{\text{DBG}}$	K1	Low	Input	OV_{DD}	
$\overline{\text{DBWO}}$	D1	Low	Input	OV_{DD}	

Table 15. Pinout Listing for the MPC755, 360 BGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
L2ZZ	G17	High	Output	$L2OV_{DD}$	
$\overline{\text{LSSD\_MODE}}$	F9	Low	Input	—	2
$\overline{\text{MCP}}$	B11	Low	Input	OV_{DD}	
NC (No Connect)	B3, B4, B5, W19, K9, K11 [4], K19 [4]	—	—	—	
OV_{DD}	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12	—	—	OV_{DD}	
PLL_CFG[0:3]	A4, A5, A6, A7	High	Input	OV_{DD}	
$\overline{\text{QACK}}$	B2	Low	Input	OV_{DD}	
$\overline{\text{QREQ}}$	J3	Low	Output	OV_{DD}	
$\overline{\text{RSRV}}$	D3	Low	Output	OV_{DD}	
$\overline{\text{SMI}}$	A12	Low	Input	OV_{DD}	
$\overline{\text{SRESET}}$	E10	Low	Input	OV_{DD}	
SYSCLK	H9	—	Input	OV_{DD}	
$\overline{\text{TA}}$	F1	Low	Input	OV_{DD}	
TBEN	A2	High	Input	OV_{DD}	
$\overline{\text{TBST}}$	A11	Low	I/O	OV_{DD}	
TCK	B10	High	Input	OV_{DD}	
TDI	B7	High	Input	OV_{DD}	6
TDO	D9	High	Output	OV_{DD}	
$\overline{\text{TEA}}$	J1	Low	Input	OV_{DD}	
$\overline{\text{TLBISYNC}}$	A3	Low	Input	OV_{DD}	
TMS	C8	High	Input	OV_{DD}	6
$\overline{\text{TRST}}$	A10	Low	Input	OV_{DD}	6
$\overline{\text{TS}}$	K7	Low	I/O	OV_{DD}	
TSIZ[0:2]	A9, B9, C9	High	Output	OV_{DD}	
TT[0:4]	C10, D11, B12, C12, F11	High	I/O	OV_{DD}	
$\overline{\text{WT}}$	C3	Low	Output	OV_{DD}	
V_{DD}	G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12	—	—	2.0 V	

Table 15. Pinout Listing for the MPC755, 360 BGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
VOLTDET	K13	High	Output	$L2OV_{DD}$	8

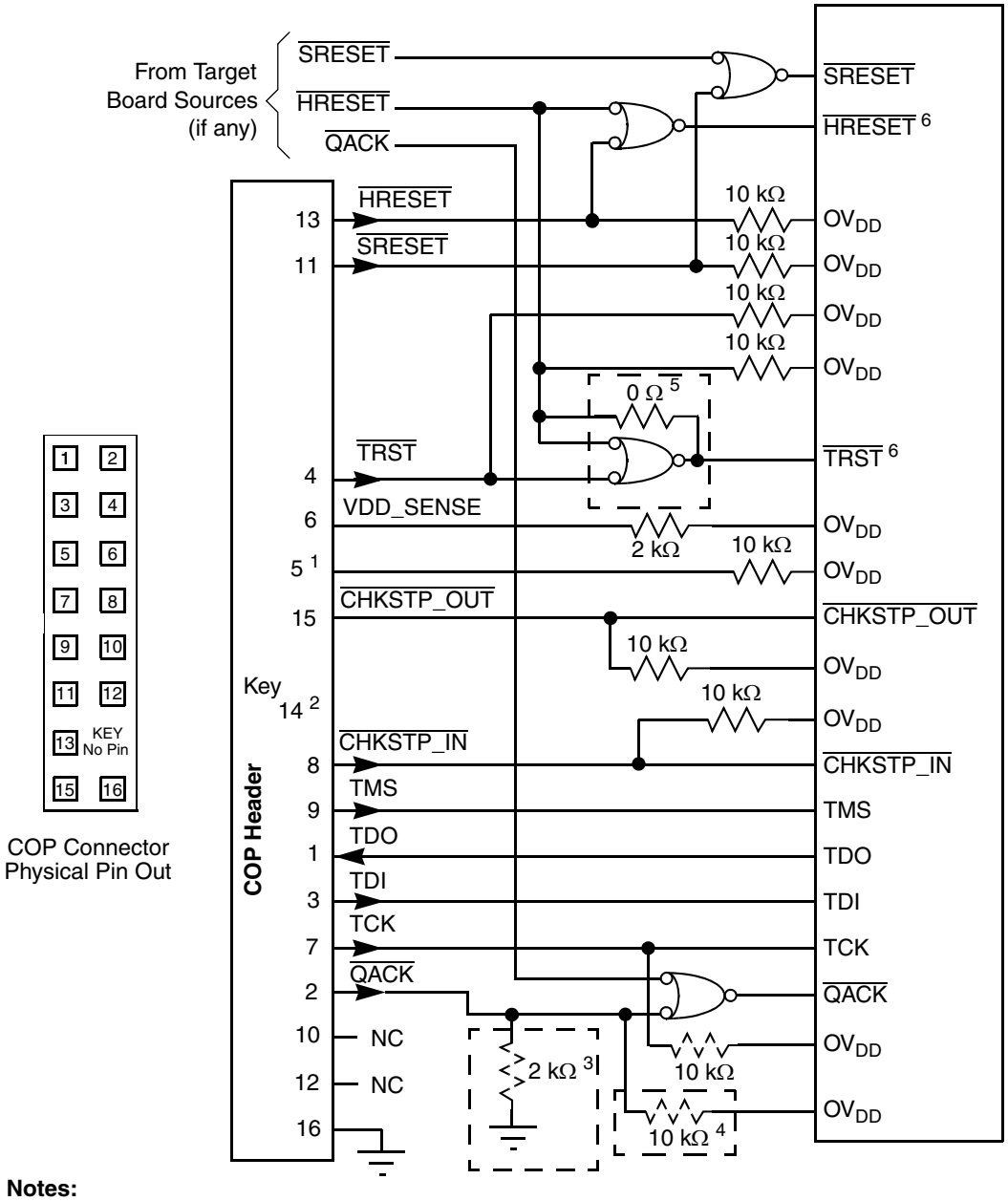
Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L2 cache controls ($\overline{L2CE}$, $\overline{L2WE}$, and L2ZZ); $L2OV_{DD}$ supplies power to the L2 cache interface (L2ADDR[0:16], L2DATA[0:63], L2DP[0:7], and L2SYNC_OUT) and the L2 control signals; and V_{DD} supplies power to the processor core and the PLL and DLL (after filtering to become AV_{DD} and $L2AV_{DD}$, respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL/L2VSEL pin configurations of Table 2 and the voltage supplied. For actual recommended value of V_{in} or supply voltages, see Table 3.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. This pin must be pulled up to OV_{DD} for proper operation of the processor interface. To allow for future I/O voltage changes, provide the option to connect BVSEL independently to either OV_{DD} or GND.
4. These pins are reserved for potential future use as additional L2 address pins.
5. Uses one of nine existing no connects in the MPC750, 360 BGA package.
6. Internal pull-up on die.
7. This pin must be pulled up to $L2OV_{DD}$ for proper operation of the processor interface. To allow for future I/O voltage changes, provide the option to connect L2VSEL independently to either $L2OV_{DD}$ or GND.
8. Internally tied to $L2OV_{DD}$ in the MPC755, 360 BGA package to indicate the power present at the L2 cache interface. This signal is not a power supply input.

   Caution: This differs from the MPC745, 255 BGA package.

7 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC745, 255 PBGA package, as well as the MPC755, 360 CBGA and PBGA packages. While both the MPC755 plastic and ceramic packages are described here, both packages are not guaranteed to be available at the same time. All new designs should allow for either ceramic or plastic BGA packages for this device. For more information on designing a common footprint for both plastic and ceramic package types, see the *Freescale Flip-Chip Plastic Ball Grid Array Presentation*. The MPC755 was initially sampled in a CBGA package, but production units are currently provided in both a CBGA and a PBGA package. Because of the better long-term device-to-board interconnect reliability of the PBGA package, Freescale recommends use of a PBGA package except where circumstances dictate use of a CBGA package.



Notes:

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the MPC755. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively deassert $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0-Ω isolation resistor.
6. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.

Figure 24. JTAG Interface Connection

There is no standardized way to number the COP header shown in Figure 24; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 25 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 24 is usually connected to the PCI bridge chip in a system and is an input to the MPC755 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC755 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is deasserted when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged via logic so that it also can be driven by the PCI bridge.

8.8 Thermal Management Information

This section provides thermal management information for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly; see Figure 25. This spring force should not exceed 5.5 pounds (2.5 kg) of force.

Figure 25 describes the package exploded cross-sectional view with several heat sink options.

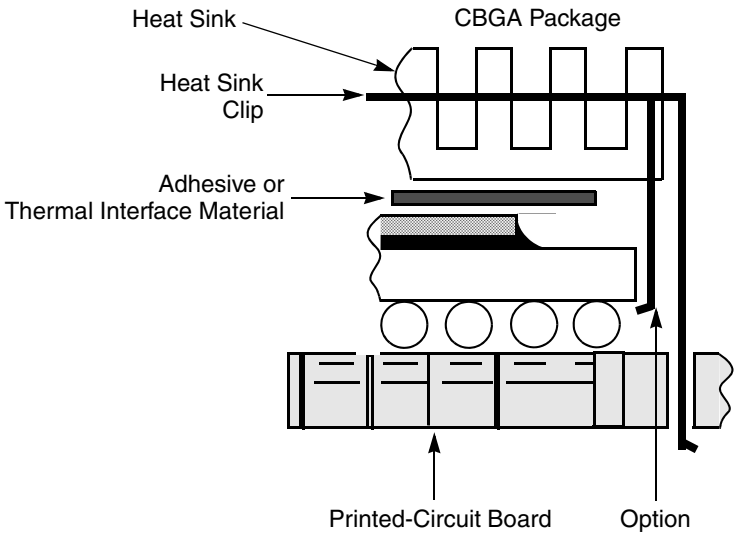


Figure 25. Package Exploded Cross-Sectional View with Several Heat Sink Options

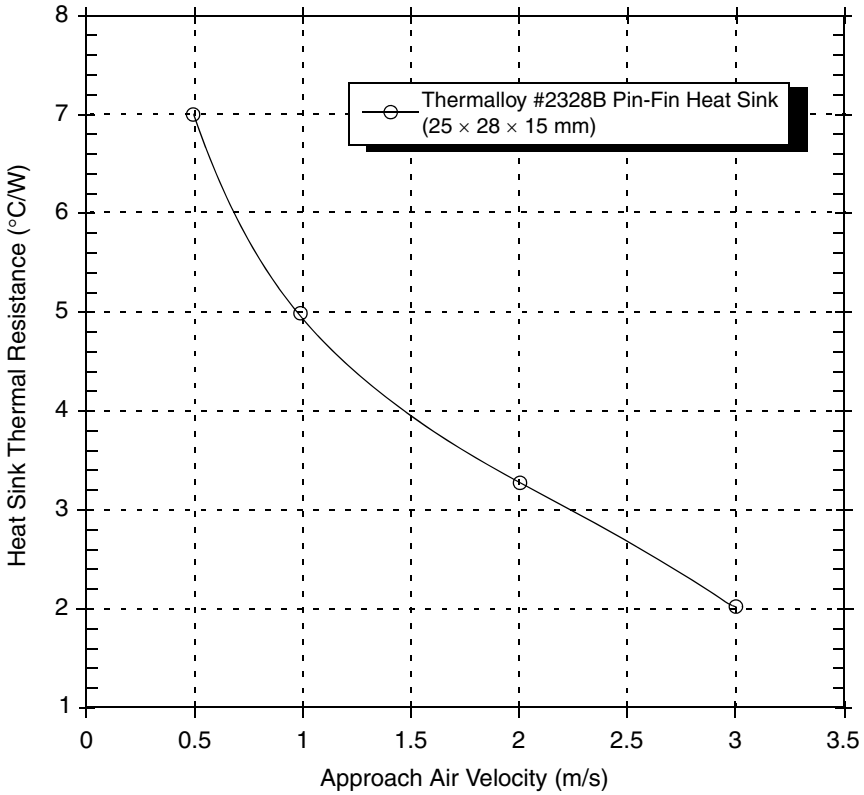


Figure 28. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs.

Table 19. Document Revision History (continued)

Revision	Date	Substantive Change(s)
4	—	Added 450 MHz speed bin.
		Changed Table 16 to show 450 MHz part in example.
		Added row for 433 and 450 MHz core frequencies to Table 17.
		In Section 1.8.8, revised the heat sink vendor list.
		In Section 1.8.8.2, revised the interface vendor list.
3	—	Updated format and thermal resistance specifications of Table 4.
		Reformatted Tables 9, 10, 11, and 12.
		Added dimensions A3, D1, and E1 to Figures 18, 19, and 20.
		Revised Section 1.8.7 and Figure 25, removed Figure 26 and Table 19 (information now included in Figure 25).
		Reformatted Section 1.10.
		Clarified address bus and address attribute pull-up recommendations in Section 1.8.7.
		Clarified Table 2.
		Updated voltage sequencing requirements in Table 1 and removed Section 1.8.3.
2	—	1.8 V/2.0 V mode no longer supported; added 2.5 V support.
		Removed 1.8 V/2.0 V mode data from Tables 2, 3, and 6.
		Added 2.5 V mode data to Tables 2, 3, and 6.
		Extended recommended operating voltage (down to 1.8 V) for V_{DD}, AV_{DD}, and $L2AV_{DD}$ for 300 and 350 MHz parts in Table 3.
		Updated Table 7 and test conditions for power consumption specifications.
		Corrected Note 6 of Table 9 to include $\overline{\text{TLBISYNC}}$ as a mode-select signal.
		Updated AC timing specifications in Table 10.
		Updated AC timing specifications in Table 12.
		Corrected AC timing specifications in Table 13.
		Added L1_TSTCLK, L2_TSTCLK, and $\overline{\text{LSSD\_MODE}}$ pull-up requirements to Section 1.8.6.
		Corrected Figure 22.

Table 19. Document Revision History (continued)

Revision	Date	Substantive Change(s)
1	—	Corrected errors in Section 1.2.
		Removed references to MPC745 CBGA package in Sections 1.3 and 1.4.
		Added airflow values for θ_{JA} to Table 5.
		Corrected V_{IH} maximum for 1.8 V mode in Table 6.
		Power consumption values added to Table 7.
		Corrected t_{MXRH} in Table 9, deleted Note 2 application note reference.
		Added Max f_{L2CLK} and Min t_{L2CLK} values to Table 11.
		Updated timing values in Table 12.
		Corrected Note 2 of Table 13.
		Changed Table 14 to reflect I/F voltages supported.
		Removed 133 and 150 MHz columns from Table 16.
		Added document reference to Section 1.7.
		Added $\overline{\text{DBB}}$ to list of signals requiring pull-ups in Section 1.8.7.
		Removed log entries from Table 20 for revisions prior to public release.
0	—	Product announced. Documentation made publicly available.