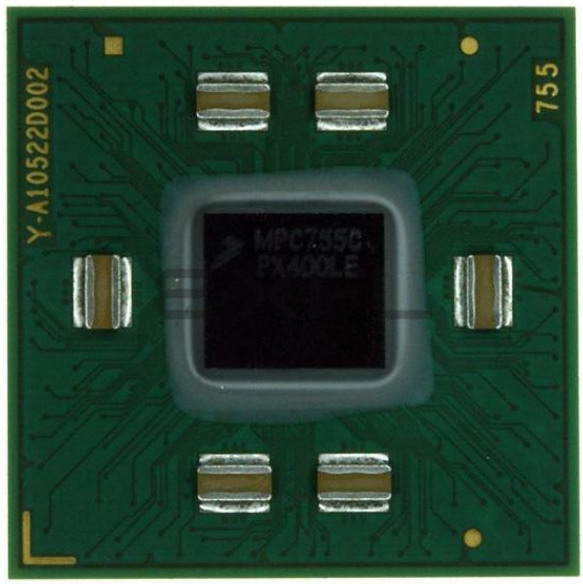


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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 400MHz |
| Co-Processors/DSP | - |
| RAM Controllers | - |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 360-BBGA, FCBGA |
| Supplier Device Package | 360-FCPBGA (25x25) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc755cvt400le |

  - Three-cycle latency, one-cycle throughput, double-precision add
  - Four-cycle latency, two-cycle throughput, double-precision multiply-add
- System unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions
- Load/store unit
  - One-cycle load or store cache access (byte, half-word, word, double word)
  - Effective address generation
  - Hits under misses (one outstanding miss)
  - Single-cycle unaligned access within double-word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations
  - Store gathering
  - Cache and TLB instructions
  - Big- and little-endian byte addressing supported
- Level 1 cache structure
  - 32K, 32-byte line, eight-way set-associative instruction cache (iL1)
  - 32K, 32-byte line, eight-way set-associative data cache (dL1)
  - Cache locking for both instruction and data caches, selectable by group of ways
  - Single-cycle cache access
  - Pseudo least-recently-used (PLRU) replacement
  - Copy-back or write-through data cache (on a page per page basis)
  - MEI data cache coherency maintained in hardware
  - Nonblocking instruction and data cache (one outstanding miss under hits)
  - No snooping of instruction cache
- Level 2 (L2) cache interface (not implemented on MPC745)
  - Internal L2 cache controller and tags; external data SRAMs
  - 256K, 512K, and 1 Mbyte two-way set-associative L2 cache support
  - Copy-back or write-through data cache (on a page basis, or for all L2)
  - Instruction-only mode and data-only mode
  - 64-byte (256K/512K) or 128-byte (1M) sectored line size
  - Supports flow through (register-buffer) synchronous BurstRAMs, pipelined (register-register) synchronous BurstRAMs (3-1-1-1 or strobeless 4-1-1-1) and pipelined (register-register) late write synchronous BurstRAMs
  - L2 configurable to cache, private memory, or split cache/private memory
  - Core-to-L2 frequency divisors of ÷1, ÷1.5, ÷2, ÷2.5, and ÷3 supported
  - 64-bit data bus

Figure 3 provides the SYSCLK input timing diagram.

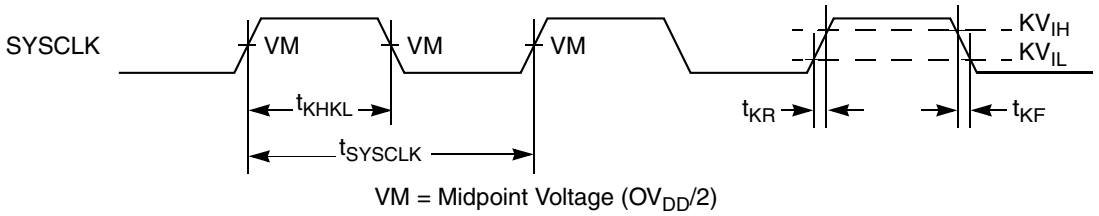



**Figure 3. SYSCLK Input Timing Diagram**

## 4.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC755 as defined in Figure 4 and Figure 6. Timing specifications for the L2 bus are provided in Section 4.2.3, "L2 Clock AC Specifications."

**Table 9. Processor Bus Mode Selection AC Timing Specifications [1]**

At recommended operating conditions (see Table 3)

| Parameter | Symbol [2] | All Speed Grades | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Mode select input setup to $\overline{\text{HRESET}}$ | $t_{MVRH}$ | 8 | — | $t_{sysclk}$ | 3, 4, 5, 6, 7 |
| $\overline{\text{HRESET}}$ to mode select input hold | $t_{MXRH}$ | 0 | — | ns | 3, 4, 6, 7, 8 |

**Notes:**

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 5). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{IVKH}$ symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And $t_{KHOV}$ symbolizes the time from SYSCLK (K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH)—note the position of the reference and its state for inputs—and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 4).
4. This specification is for configuration mode select only. Also note that the $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
5. $t_{sysclk}$ is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
6. Mode select signals are BVSEL, L2VSEL, PLL_CFG[0:3], and $\overline{\text{TLBISYNC}}$.
7. Guaranteed by design and characterization.
8. Bus mode select pins must remain stable during operation. Changing the logic states of BVSEL or L2VSEL during operation will cause the bus mode voltage selection to change. Changing the logic states of the PLL_CFG pins during operation will cause the PLL division ratio selection to change. Both of these conditions are considered outside the specification and are not supported. Once $\overline{\text{HRESET}}$ is negated the states of the bus mode selection pins must remain stable.

Figure 4 provides the mode select input timing diagram for the MPC755.

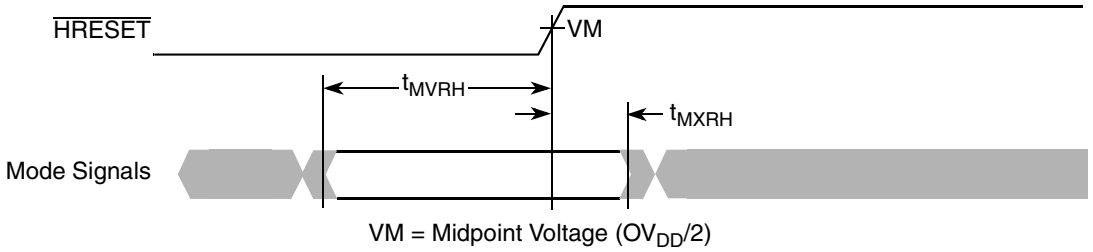



**Figure 4. Mode Input Timing Diagram**

Figure 5 provides the AC test load for the MPC755.

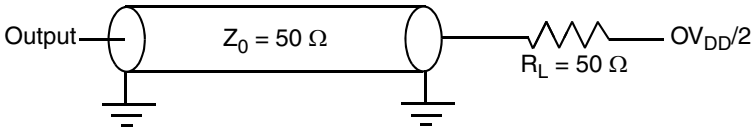



**Figure 5. AC Test Load**

## Table 11. L2CLK Output AC Timing Specification

At recommended operating conditions (see Table 3)

| Parameter | Symbol | All Speed Grades | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| L2CLK frequency | $f_{L2CLK}$ | 80 | 450 | MHz | 1, 4 |
| L2CLK cycle time | $t_{L2CLK}$ | 2.5 | 12.5 | ns | |
| L2CLK duty cycle | $t_{CHCL}/t_{L2CLK}$ | 45 | 55 | % | 2, 7 |
| Internal DLL-relock time | | 640 | — | L2CLK | 3, 7 |
| DLL capture window | | 0 | 10 | ns | 5, 7 |
| L2CLK_OUT output-to-output skew | $t_{L2CSKW}$ | — | 50 | ps | 6, 7 |
| L2CLK_OUT output jitter | | — | ±150 | ps | 6, 7 |

**Notes:**

1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB, L2CLK_OUT, and L2SYNC_OUT pins. The L2CLK frequency-to-core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. The maximum L2LCK frequency will be system dependent. L2CLK_OUTA and L2CLK_OUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The DLL-relock time is specified in terms of L2CLK periods. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in ns. Relock timing is guaranteed by design and characterization.
4. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz. This adds more delay to each tap of the DLL.
5. Allowable skew between L2SYNC_OUT and L2SYNC_IN.
6. This output jitter number represents the maximum delay of one tap forward or one tap back from the current DLL tap as the phase comparator seeks to minimize the phase difference between L2SYNC_IN and the internal L2CLK. This number must be comprehended in the L2 timing analysis. The input jitter on SYSCLK affects L2CLK_OUT and the L2 address/data/control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L2 timing analysis.
7. Guaranteed by design.

The L2CLK_OUT timing diagram is shown in Figure 7.

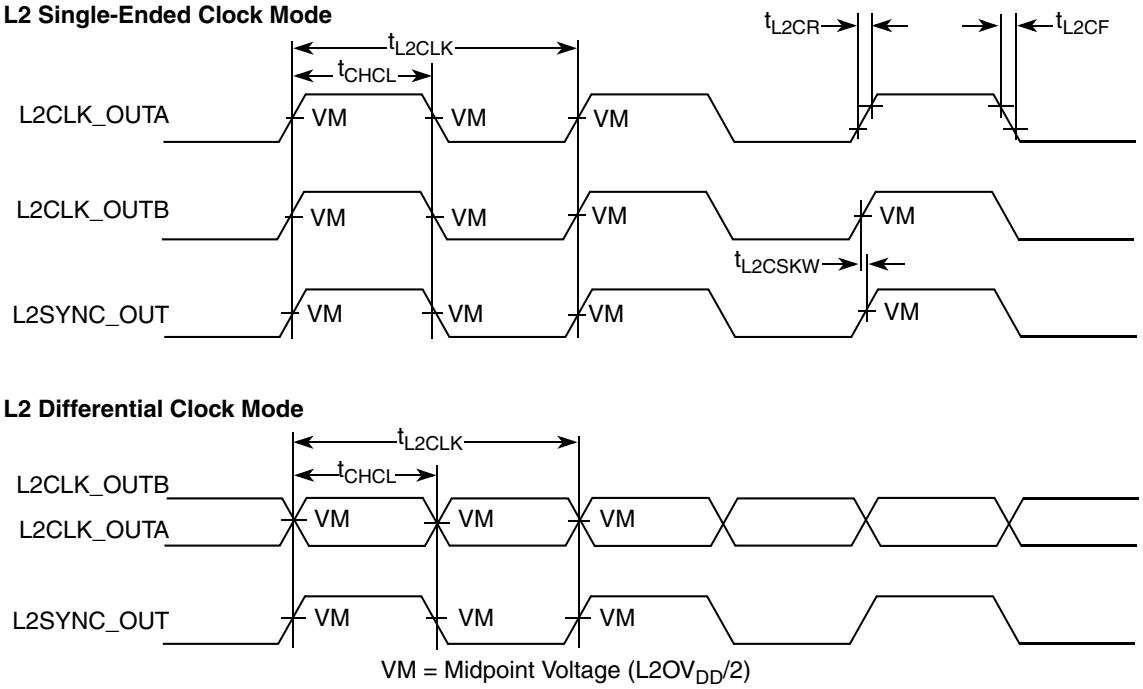



**Figure 7. L2CLK_OUT Output Timing Diagram**

## 4.2.4 L2 Bus AC Specifications

Table 12 provides the L2 bus interface AC timing specifications for the MPC755 as defined in Figure 8 and Figure 9 for the loading conditions described in Figure 10.

**Table 12. L2 Bus Interface AC Timing Specifications**

At recommended operating conditions (see Table 3)

| Parameter | Symbol | All Speed Grades | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| L2SYNC_IN rise and fall time | $t_{L2CR}$, $t_{L2CF}$ | — | 1.0 | ns | 1 |
| Setup times: Data and parity | $t_{DVL2CH}$ | 1.2 | — | ns | 2 |
| Input hold times: Data and parity | $t_{DXL2CH}$ | 0 | — | ns | 2 |
| Valid times:<br>All outputs when L2CR[14–15] = 00<br>All outputs when L2CR[14–15] = 01<br>All outputs when L2CR[14–15] = 10<br>All outputs when L2CR[14–15] = 11 | $t_{L2CHOV}$ | <br>—<br>—<br>—<br>— | <br>3.1<br>3.2<br>3.3<br>3.7 | ns | 3, 4 |
| Output hold times:<br>All outputs when L2CR[14–15] = 00<br>All outputs when L2CR[14–15] = 01<br>All outputs when L2CR[14–15] = 10<br>All outputs when L2CR[14–15] = 11 | $t_{L2CHOX}$ | <br>0.5<br>0.7<br>0.9<br>1.1 | <br>—<br>—<br>—<br>— | ns | 3 |

Figure 9 shows the L2 bus output timing diagrams for the MPC755.

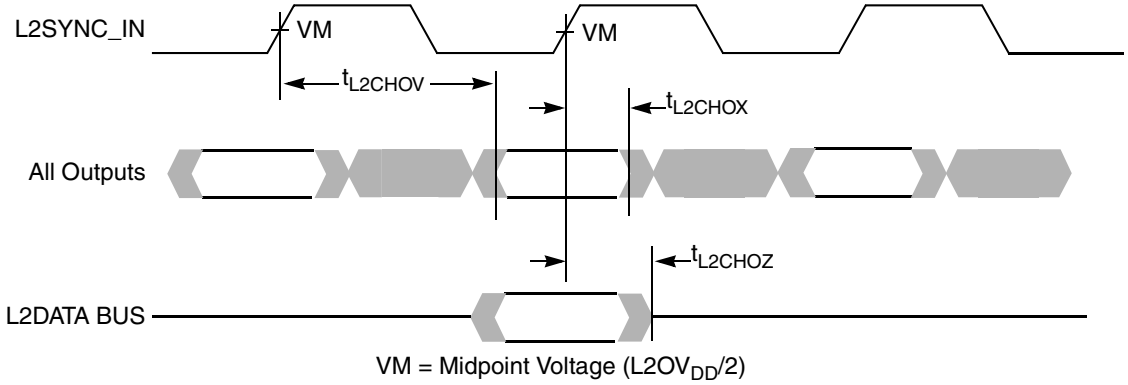



**Figure 9. L2 Bus Output Timing Diagrams**

Figure 10 provides the AC test load for L2 interface of the MPC755.

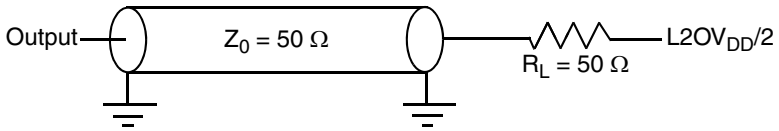



**Figure 10. AC Test Load for the L2 Interface**

### 4.2.5 IEEE 1149.1 AC Timing Specifications

Table 13 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 12 through Figure 15.

**Table 13. JTAG AC Timing Specifications (Independent of SYSCLK) [1]**

At recommended operating conditions (see Table 3)

| Parameter | | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| TCK frequency of operation | | $f_{TCLK}$ | 0 | 16 | MHz | |
| TCK cycle time | | $t_{TCLK}$ | 62.5 | — | ns | |
| TCK clock pulse width measured at 1.4 V | | $t_{JHJL}$ | 31 | — | ns | |
| TCK rise and fall times | | $t_{JR}$, $t_{JF}$ | 0 | 2 | ns | |
| $\overline{\text{TRST}}$ assert time | | $t_{TRST}$ | 25 | — | ns | 2 |
| Input setup times: | Boundary-scan data<br>TMS, TDI | $t_{DVJH}$<br>$t_{IVJH}$ | 4<br>0 | —<br>— | ns | 3 |
| Input hold times: | Boundary-scan data<br>TMS, TDI | $t_{DXJH}$<br>$t_{IXJH}$ | 15<br>12 | —<br>— | ns | 3 |
| Valid times: | Boundary-scan data<br>TDO | $t_{JLDV}$<br>$t_{JLOV}$ | —<br>— | 4<br>4 | ns | 4 |
| Output hold times: | Boundary-scan data<br>TDO | $t_{JLDH}$<br>$t_{JLOH}$ | 25<br>12 | —<br>— | ns | 4 |
| TCK to output high impedance: | Boundary-scan data<br>TDO | $t_{JLDZ}$<br>$t_{JLOZ}$ | 3<br>3 | 19<br>9 | ns | 4, 5 |

**Notes:**

1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 11). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal which must be asserted for this minimum time to be recognized.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 11 provides the AC test load for TDO and the boundary-scan outputs of the MPC755.

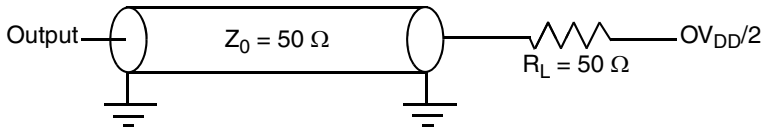
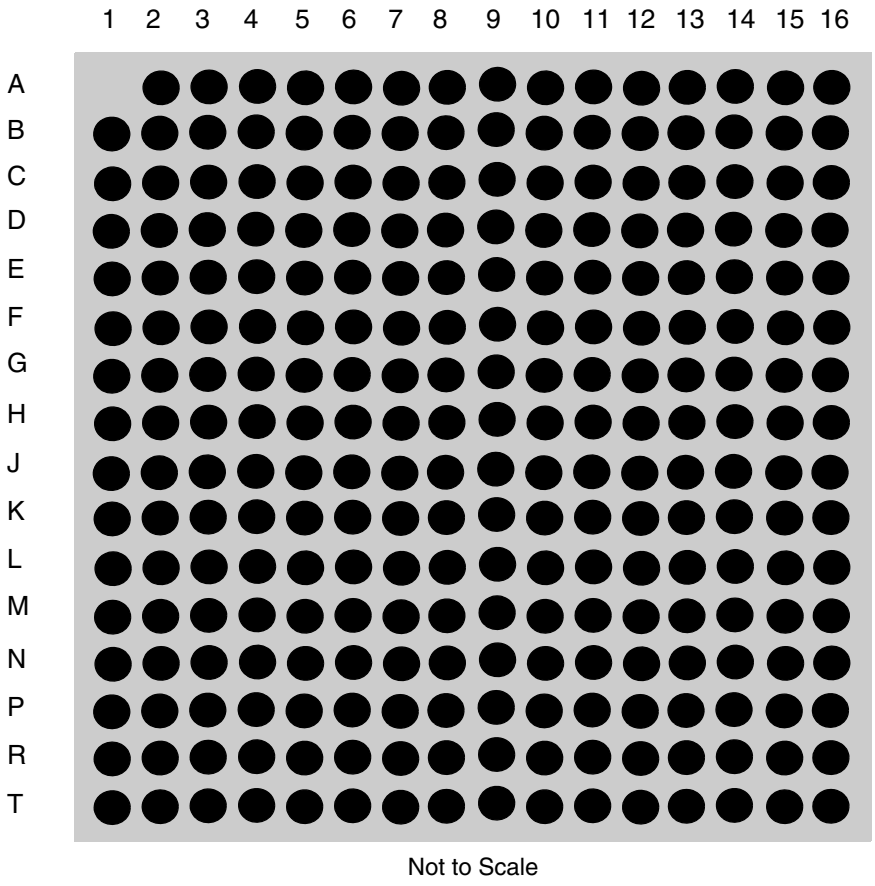



**Figure 11. AC Test Load for the JTAG Interface**

# 5 Pin Assignments

Figure 16 (in Part A) shows the pinout of the MPC745, 255 PBGA package as viewed from the top surface. Part B shows the side profile of the PBGA package to indicate the direction of the top surface view.

**Part A**




**Part B**

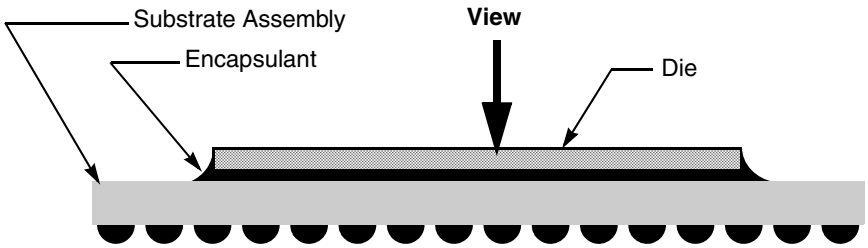



**Figure 16. Pinout of the MPC745, 255 PBGA Package as Viewed from the Top Surface**

**Table 14. Pinout Listing for the MPC745, 255 PBGA Package (continued)**

| Signal Name | Pin Number | Active | I/O | I/F Voltage [1] | Notes |
|---|---|---|---|---|---|
| $\overline{\text{INT}}$ | B15 | Low | Input | $OV_{DD}$ | |
| L1_TSTCLK | D11 | High | Input | — | 2 |
| L2_TSTCLK | D12 | High | Input | — | 2 |
| $\overline{\text{LSSD\_MODE}}$ | B10 | Low | Input | — | 2 |
| $\overline{\text{MCP}}$ | C13 | Low | Input | $OV_{DD}$ | |
| NC (No Connect) | B7, B8, C3, C6, C8, D5, D6, H4, J16, A4, A5, A2, A3, B5 | — | — | — | |
| $OV_{DD}$ | C7, E5, E7, E10, E12, G3, G5, G12, G14, K3, K5, K12, K14, M5, M7, M10, M12, P7, P10 | — | — | 2.5 V/3.3 V | |
| PLL_CFG[0:3] | A8, B9, A9, D9 | High | Input | $OV_{DD}$ | |
| $\overline{\text{QACK}}$ | D3 | Low | Input | $OV_{DD}$ | |
| $\overline{\text{QREQ}}$ | J3 | Low | Output | $OV_{DD}$ | |
| $\overline{\text{RSRV}}$ | D1 | Low | Output | $OV_{DD}$ | |
| $\overline{\text{SMI}}$ | A16 | Low | Input | $OV_{DD}$ | |
| $\overline{\text{SRESET}}$ | B14 | Low | Input | $OV_{DD}$ | |
| SYSCLK | C9 | — | Input | $OV_{DD}$ | |
| $\overline{\text{TA}}$ | H14 | Low | Input | $OV_{DD}$ | |
| TBEN | C2 | High | Input | $OV_{DD}$ | |
| $\overline{\text{TBST}}$ | A14 | Low | I/O | $OV_{DD}$ | |
| TCK | C11 | High | Input | $OV_{DD}$ | |
| TDI | A11 | High | Input | $OV_{DD}$ | 5 |
| TDO | A12 | High | Output | $OV_{DD}$ | |
| $\overline{\text{TEA}}$ | H13 | Low | Input | $OV_{DD}$ | |
| $\overline{\text{TLBISYNC}}$ | C4 | Low | Input | $OV_{DD}$ | |
| TMS | B11 | High | Input | $OV_{DD}$ | 5 |
| $\overline{\text{TRST}}$ | C10 | Low | Input | $OV_{DD}$ | 5 |
| $\overline{\text{TS}}$ | J13 | Low | I/O | $OV_{DD}$ | |
| TSIZ[0:2] | A13, D10, B12 | High | Output | $OV_{DD}$ | |
| TT[0:4] | B13, A15, B16, C14, C15 | High | I/O | $OV_{DD}$ | |
| $\overline{\text{WT}}$ | D2 | Low | Output | $OV_{DD}$ | |
| $V_{DD}$ | F6, F8, F9, F11, G7, G10, H6, H8, H9, H11, J6, J8, J9, J11, K7, K10, L6, L8, L9, L11 | — | — | 2.0 V | |

**Table 14. Pinout Listing for the MPC745, 255 PBGA Package (continued)**

| Signal Name | Pin Number | Active | I/O | I/F Voltage [1] | Notes |
|---|---|---|---|---|---|
| VOLTDET | F3 | High | Output | — | 6 |

**Notes:**

1. $OV_{DD}$ supplies power to the processor bus, JTAG, and all control signals; and $V_{DD}$ supplies power to the processor core and the PLL (after filtering to become $AV_{DD}$). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL pin configuration of Table 2 and the voltage supplied. For actual recommended value of $V_{in}$ or supply voltages, see Table 3.
2. These are test signals for factory use only and must be pulled up to $OV_{DD}$ for normal machine operation.
3. This pin must be pulled up to $OV_{DD}$ for proper operation of the processor interface. To allow for future I/O voltage changes, provide the option to connect BVSEL independently to either $OV_{DD}$ or GND.
4. Uses 1 of 15 existing no connects in the MPC740, 255 BGA package.
5. Internal pull-up on die.
6. Internally tied to GND in the MPC745, 255 BGA package to indicate to the power supply that a low-voltage processor is present. This signal is not a power supply input.

   **Caution:** This differs from the MPC755, 360 BGA package.

Table 15 provides the pinout listing for the MPC755, 360 PBGA and CBGA packages.

**Table 15. Pinout Listing for the MPC755, 360 BGA Package**

| Signal Name | Pin Number | Active | I/O | I/F Voltage [1] | Notes |
|---|---|---|---|---|---|
| A[0:31] | A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2 | High | I/O | $OV_{DD}$ | |
| $\overline{\text{AACK}}$ | N3 | Low | Input | $OV_{DD}$ | |
| $\overline{\text{ABB}}$ | L7 | Low | I/O | $OV_{DD}$ | |
| AP[0:3] | C4, C5, C6, C7 | High | I/O | $OV_{DD}$ | |
| $\overline{\text{ARTRY}}$ | L6 | Low | I/O | $OV_{DD}$ | |
| $AV_{DD}$ | A8 | — | — | 2.0 V | |
| $\overline{\text{BG}}$ | H1 | Low | Input | $OV_{DD}$ | |
| $\overline{\text{BR}}$ | E7 | Low | Output | $OV_{DD}$ | |
| BVSEL | W1 | High | Input | $OV_{DD}$ | 3, 5, 6 |
| $\overline{\text{CI}}$ | C2 | Low | Output | $OV_{DD}$ | |
| $\overline{\text{CKSTP\_IN}}$ | B8 | Low | Input | $OV_{DD}$ | |
| $\overline{\text{CKSTP\_OUT}}$ | D7 | Low | Output | $OV_{DD}$ | |
| CLK_OUT | E3 | — | Output | $OV_{DD}$ | |
| $\overline{\text{DBB}}$ | K5 | Low | I/O | $OV_{DD}$ | |
| $\overline{\text{DBDIS}}$ | G1 | Low | Input | $OV_{DD}$ | |
| $\overline{\text{DBG}}$ | K1 | Low | Input | $OV_{DD}$ | |
| $\overline{\text{DBWO}}$ | D1 | Low | Input | $OV_{DD}$ | |

**Table 15. Pinout Listing for the MPC755, 360 BGA Package (continued)**

| Signal Name | Pin Number | Active | I/O | I/F Voltage [1] | Notes |
|---|---|---|---|---|---|
| DH[0:31] | W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5 | High | I/O | $OV_{DD}$ | |
| DL[0:31] | M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2 | High | I/O | $OV_{DD}$ | |
| DP[0:7] | L1, P2, M2, V2, M1, N2, T3, R1 | High | I/O | $OV_{DD}$ | |
| $\overline{\text{DRTRY}}$ | H6 | Low | Input | $OV_{DD}$ | |
| $\overline{\text{GBL}}$ | B1 | Low | I/O | $OV_{DD}$ | |
| GND | D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16 | — | — | GND | |
| $\overline{\text{HRESET}}$ | B6 | Low | Input | $OV_{DD}$ | |
| $\overline{\text{INT}}$ | C11 | Low | Input | $OV_{DD}$ | |
| L1_TSTCLK | F8 | High | Input | — | 2 |
| L2ADDR[16:0] | G18, H19, J13, J14, H17, H18, J16, J17, J18, J19, K15, K17, K18, M19, L19, L18, L17 | High | Output | $L2OV_{DD}$ | |
| $L2AV_{DD}$ | L13 | — | — | 2.0 V | |
| $\overline{\text{L2CE}}$ | P17 | Low | Output | $L2OV_{DD}$ | |
| L2CLK_OUTA | N15 | — | Output | $L2OV_{DD}$ | |
| L2CLK_OUTB | L16 | — | Output | $L2OV_{DD}$ | |
| L2DATA[0:63] | U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13 | High | I/O | $L2OV_{DD}$ | |
| L2DP[0:7] | V14, U16, T19, N18, H14, F17, C19, B15 | High | I/O | $L2OV_{DD}$ | |
| $L2OV_{DD}$ | D15, E14, E16, H16, J15, L15, M16, P15, R14, R16, T15, F15 | — | — | $L2OV_{DD}$ | |
| L2SYNC_IN | L14 | — | Input | $L2OV_{DD}$ | |
| L2SYNC_OUT | M14 | — | Output | $L2OV_{DD}$ | |
| L2_TSTCLK | F7 | High | Input | — | 2 |
| L2VSEL | A19 | High | Input | $L2OV_{DD}$ | 1, 5, 6, 7 |
| $\overline{\text{L2WE}}$ | N16 | Low | Output | $L2OV_{DD}$ | |

**Table 15. Pinout Listing for the MPC755, 360 BGA Package (continued)**

| Signal Name | Pin Number | Active | I/O | I/F Voltage [1] | Notes |
|---|---|---|---|---|---|
| VOLTDET | K13 | High | Output | $L2OV_{DD}$ | 8 |

**Notes:**

1. $OV_{DD}$ supplies power to the processor bus, JTAG, and all control signals except the L2 cache controls ($\overline{L2CE}$, $\overline{L2WE}$, and L2ZZ); $L2OV_{DD}$ supplies power to the L2 cache interface (L2ADDR[0:16], L2DATA[0:63], L2DP[0:7], and L2SYNC_OUT) and the L2 control signals; and $V_{DD}$ supplies power to the processor core and the PLL and DLL (after filtering to become $AV_{DD}$ and $L2AV_{DD}$, respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL/L2VSEL pin configurations of Table 2 and the voltage supplied. For actual recommended value of $V_{in}$ or supply voltages, see Table 3.
2. These are test signals for factory use only and must be pulled up to $OV_{DD}$ for normal machine operation.
3. This pin must be pulled up to $OV_{DD}$ for proper operation of the processor interface. To allow for future I/O voltage changes, provide the option to connect BVSEL independently to either $OV_{DD}$ or GND.
4. These pins are reserved for potential future use as additional L2 address pins.
5. Uses one of nine existing no connects in the MPC750, 360 BGA package.
6. Internal pull-up on die.
7. This pin must be pulled up to $L2OV_{DD}$ for proper operation of the processor interface. To allow for future I/O voltage changes, provide the option to connect L2VSEL independently to either $L2OV_{DD}$ or GND.
8. Internally tied to $L2OV_{DD}$ in the MPC755, 360 BGA package to indicate the power present at the L2 cache interface. This signal is not a power supply input.

   **Caution:** This differs from the MPC745, 255 BGA package.

# 7 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC745, 255 PBGA package, as well as the MPC755, 360 CBGA and PBGA packages. While both the MPC755 plastic and ceramic packages are described here, both packages are not guaranteed to be available at the same time. All new designs should allow for either ceramic or plastic BGA packages for this device. For more information on designing a common footprint for both plastic and ceramic package types, see the *Freescale Flip-Chip Plastic Ball Grid Array Presentation*. The MPC755 was initially sampled in a CBGA package, but production units are currently provided in both a CBGA and a PBGA package. Because of the better long-term device-to-board interconnect reliability of the PBGA package, Freescale recommends use of a PBGA package except where circumstances dictate use of a CBGA package.

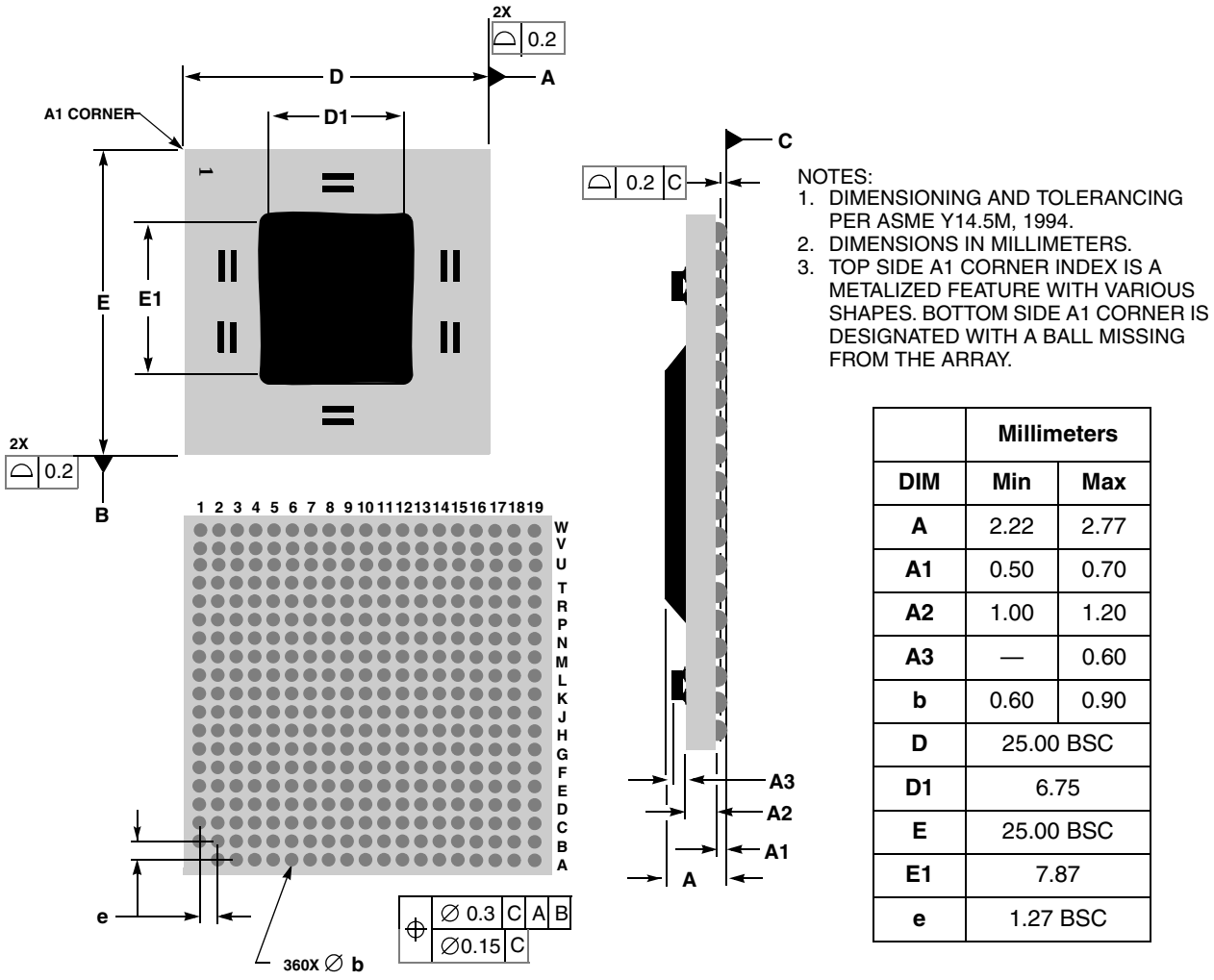
## 7.5 Package Parameters for the MPC755 PBGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead plastic ball grid array (PBGA).

| | |
|---|---|
| Package outline | 25 × 25 mm |
| Interconnects | 360 (19 × 19 ball array – 1) |
| Pitch | 1.27 mm (50 mil) |
| Minimum module height | 2.22 mm |
| Maximum module height | 2.77 mm |
| Ball diameter | 0.75 mm (29.5 mil) |

## 7.6 Mechanical Dimensions for the MPC755

Figure 20 provides the mechanical dimensions and bottom surface nomenclature for the MPC755, 360 PBGA package.




| | Millimeters | |
|---|---|---|
| DIM | Min | Max |
| A | 2.22 | 2.77 |
| A1 | 0.50 | 0.70 |
| A2 | 1.00 | 1.20 |
| A3 | — | 0.60 |
| b | 0.60 | 0.90 |
| D | 25.00 BSC | |
| D1 | 6.75 | |
| E | 25.00 BSC | |
| E1 | 7.87 | |
| e | 1.27 BSC | |

**Figure 20. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC755, 360 PBGA Package**

There is no standardized way to number the COP header shown in Figure 24; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 25 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 24 is usually connected to the PCI bridge chip in a system and is an input to the MPC755 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC755 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is deasserted when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged via logic so that it also can be driven by the PCI bridge.

## 8.8 Thermal Management Information

This section provides thermal management information for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly; see Figure 25. This spring force should not exceed 5.5 pounds (2.5 kg) of force.

Figure 25 describes the package exploded cross-sectional view with several heat sink options.

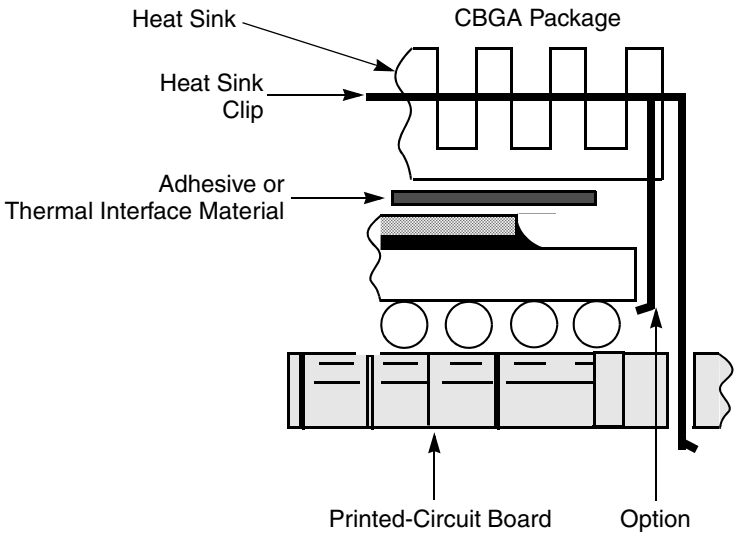



**Figure 25. Package Exploded Cross-Sectional View with Several Heat Sink Options**

The board designer can choose between several types of heat sinks to place on the MPC755. There are several commercially-available heat sinks for the MPC755 provided by the following vendors:

| | |
|---|---|
| Aavid Thermalloy<br>80 Commercial St.<br>Concord, NH 03301<br>Internet: www.aavidthermalloy.com | 603-224-9988 |
| Alpha Novatech<br>473 Sapena Ct. #15<br>Santa Clara, CA 95054<br>Internet: www.alphanovatech.com | 408-749-7601 |
| International Electronic Research Corporation (IERC)<br>413 North Moss St.<br>Burbank, CA 91502<br>Internet: www.ctscorp.com | 818-842-7277 |
| Tyco Electronics<br>Chip Coolers™<br>P.O. Box 3668<br>Harrisburg, PA 17105-3668<br>Internet: www.chipcoolers.com | 800-522-6752 |
| Wakefield Engineering<br>33 Bridge St.<br>Pelham, NH 03076<br>Internet: www.wakefield.com | 603-635-5102 |

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

### 8.8.1 Internal Package Conduction Resistance

For the exposed-die packaging technology, shown in Table 4, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case (or top-of-die for exposed silicon) thermal resistance
- The die junction-to-ball thermal resistance

Figure 26 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.

Shin-Etsu MicroSi, Inc. 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

### 8.8.3 Heat Sink Selection Example

This section provides a heat sink selection example using one of the commercially-available heat sinks. For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) \times P_d$$

where:

$T_j$ is the die-junction temperature
$T_a$ is the inlet cabinet ambient temperature
$T_r$ is the air temperature rise within the computer cabinet
$\theta_{jc}$ is the junction-to-case thermal resistance
$\theta_{int}$ is the adhesive or interface material thermal resistance
$\theta_{sa}$ is the heat sink base-to-ambient thermal resistance
$P_d$ is the power dissipated by the device

During operation the die-junction temperatures ($T_j$) should be maintained less than the value specified in Table 3. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature ($T_a$) may range from 30° to 40°C. The air temperature rise within a cabinet ($T_r$) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($\theta_{int}$) is typically about 1°C/W. Assuming a $T_a$ of 30°C, a $T_r$ of 5°C, a CBGA package $R_{\theta jc} < 0.1$, and a power consumption ($P_d$) of 5.0 W, the following expression for $T_j$ is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 1.0°C/W + \theta_{sa}) \times 5.0\ W$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance ($\theta_{sa}$) versus airflow velocity is shown in Figure 28.

Assuming an air velocity of 0.5 m/s, we have an effective $R_{sa}$ of 7°C/W, thus

$$T_j = 30°C + 5°C + (0.1°C/W + 1.0°C/W + 7°C/W) \times 5.0\ W,$$

resulting in a die-junction temperature of approximately 76°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, The Bergquist Company, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.

# 9 Document Revision History

Table 19 provides a revision history for this hardware specification.

**Table 19. Document Revision History**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 8 | 2/8/2006 | Changed processor descriptor from ‘B’ to ‘C’ for 350 MHz devices and increased power specifications for full-power mode in Table 7. |
| 7 | 4/05/2005 | Removed phrase “for the ceramic ball grid array (CBGA) package” from Section 8.8; this information applies to devices in both CBGA and PBGA packages. |
| | | Figure 24—updated COP Connector Diagram to recommend a weak pull-up resistor on TCK. |
| | | Table 20—added MPC745BPXLE, MPC755BRXLE, MPC755BPXLE, MPC755CVTLE, MPC755BVTLE and MPC745BVTLE part numbers. These devices are fully addressed by this document. |
| | | Corrected Revision Level in Table 23: Rev E devices are Rev 2.8, not 2.7. |
| | | Added MPC755CRX400LE and MPC755CPX400LE to devices supported by this specification in Table 20. |
| | | Removed “Advance Information” from title block on page 1. |
| 6.1 | 1/21/2005 | Updated document template. |
| 6 | — | Removed 450 MHz speed grade throughout document. These devices are no longer supported for new designs; see Section 1.10.2 for more information. |
| | | Relaxed voltage sequencing requirements in Notes 3 and 4 of Table 1. |
| | | Corrected Note 2 of Table 7. |
| | | Changed processor descriptor from ‘B’ to ‘C’ for 400 MHz devices and increased power specifications for full-power mode in Table 7. XPC755Bxx400LE devices are no longer produced and are documented in a separate part number specification; see Section 1.10.2 for more information. |
| | | Increased power specifications for sleep mode for all speed grades in Table 7. |
| | | Removed ‘Sleep Mode (PLL and DLL Disabled)—Typical’ specification from Table 7; this is no longer tested or characterized. |
| | | Added Note 4 to Table 7. |
| | | Revised L2 clock duty cycle specification in Table 11 and changed Note 7. |
| | | Corrected Note 3 in Table 20. |
| | | Replaced Table 21 and added Tables 22 and 23. |
| 5 | — | Added Note 6 to Table 10; clarification only as this information is already documented in the *MPC750 RISC Microprocessor Family User’s Manual*. |
| | | Revised Figure 24 and Section 1.8.7. |
| | | Corrected Process Identifier for 450 MHz part in Table 20. |
| | | Added XPC755BRX*nnn*T*x* series to Table 21. |

**Table 19. Document Revision History (continued)**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 1 | — | Corrected errors in Section 1.2. |
| | | Removed references to MPC745 CBGA package in Sections 1.3 and 1.4. |
| | | Added airflow values for $\theta_{JA}$ to Table 5. |
| | | Corrected $V_{IH}$ maximum for 1.8 V mode in Table 6. |
| | | Power consumption values added to Table 7. |
| | | Corrected $t_{MXRH}$ in Table 9, deleted Note 2 application note reference. |
| | | Added Max $f_{L2CLK}$ and Min $t_{L2CLK}$ values to Table 11. |
| | | Updated timing values in Table 12. |
| | | Corrected Note 2 of Table 13. |
| | | Changed Table 14 to reflect I/F voltages supported. |
| | | Removed 133 and 150 MHz columns from Table 16. |
| | | Added document reference to Section 1.7. |
| | | Added $\overline{\text{DBB}}$ to list of signals requiring pull-ups in Section 1.8.7. |
| | | Removed log entries from Table 20 for revisions prior to public release. |
| 0 | — | Product announced. Documentation made publicly available. |

# 10 Ordering Information

Ordering information for the devices fully covered by this specification document is provided in Section 10.1, “Part Numbers Fully Addressed by This Document.” Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number. Section 10.2, “Part Numbers Not Fully Addressed by This Document,” lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specifications addendum.

## 10.1 Part Numbers Fully Addressed by This Document

Table 20 provides the Freescale part numbering nomenclature for the MPC755 and MPC745 devices fully addressed by this document.

**Table 20. Part Numbering Nomenclature**

| MPC | *xxx* | *x* | *xx* | *nnn* | *x* | *x* |
|---|---|---|---|---|---|---|
| **Product Code** | **Part Identifier** | **Process Descriptor** | **Package [1]** | **Processor Frequency** | **Application Modifier** | **Revision Level** |
| XPC[2] | 755<br>745 | B = HiP4DP | PX = PBGA<br>RX = CBGA | 300<br>350 | L: 2.0 V ± 100 mV<br>0° to 105°C | E: 2.8; PVR = 0008 3203 |
| | 755 | C = HiP4DP | | 400 | | |
| MPC | 755 | B = HiP4DP | | 300<br>350 | | |
| | | C = HiP4DP | | 350<br>400 | | |
| | 745 | B = HiP4DP | PX = PBGA | 300<br>350 | | |
| | 745 | C = HiP4DP | PX = PBGA<br>VT = PBGAPb-free BGA | 350 | | |
| | 755<br>745 | B = HiP4DP | VT = PBGAPb-free BGA | 300<br>350 | | |
| | 755 | C = HiP4DP | | 350<br>400 | | |

**Notes:**

1. See Section 7, “Package Description,” for more information on available package types.
2. The X prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These are from a limited production volume of prototypes manufactured, tested, and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes

## 10.2 Part Numbers Not Fully Addressed by This Document

Devices not fully addressed in this document are described in separate hardware specification addendums which supplement and supersede this document, as described in the following tables.

**Table 21. Part Numbers Addressed by XPC755B*xxnnn*T*x* Series Part Numbers (Document No. MPC755ECSO1AD)**

| XPC | 755 | B | *xx* | *nnn* | T | *x* |
|---|---|---|---|---|---|---|

| Product Code | Part Identifier | Process Descriptor | Package | Processor Frequency | Application Modifier | Revision Level |
|---|---|---|---|---|---|---|
| XPC | 755 | B = HiP4DP | RX = CBGA | 350<br>400 | T: 2.0 V ± 100 mV<br>–40° to 105°C | D: 2.7; PVR = 0008 3203<br>E: 2.8; PVR = 0008 3203 |
| MPC | 755 | C=HiP4DP | RX = CBGA | 350 | T: 2.0 V ± 100 mV<br>–40° to 105°C | E: 2.8; PVR = 0008 3203 |

**Table 22. Part Numbers Addressed by XPC755B*xxnnn*LD Series Part Numbers (Document No. MPC755ECSO2AD)**

| XPC | *xxx* | B | *xx* | *nnn* | L | D |
|---|---|---|---|---|---|---|

| Product Code | Part Identifier | Process Descriptor | Package | Processor Frequency | Application Modifier | Revision Level |
|---|---|---|---|---|---|---|
| XPC | 755<br>745 | B = HiP4DP | PX = PBGA<br>RX = CBGA | 300<br>350<br>400 | L: 2.0 V ± 100 mV<br>0° to 105°C | D: 2.7; PVR = 0008 3203 |

**Table 23. Part Numbers Addressed by XPC755*xxxnnn*LE Series Part Numbers (Document No. MPC755ECSO3AD)**

| XPC | 755 | *x* | *xx* | *nnn* | L | E |
|---|---|---|---|---|---|---|

| Product Code | Part Identifier | Process Descriptor | Package | Processor Frequency | Application Modifier | Revision Level |
|---|---|---|---|---|---|---|
| XPC | 755 | B = HiP4DP | RX = CBGA | 400 | L: 2.0 V ± 100 mV<br>0° to 105°C | E: 2.8; PVR = 0008 3203 |
| | | | PX = PBGA | | | |
| | | C = HiP4DP | RX = CBGA | 450 | | |