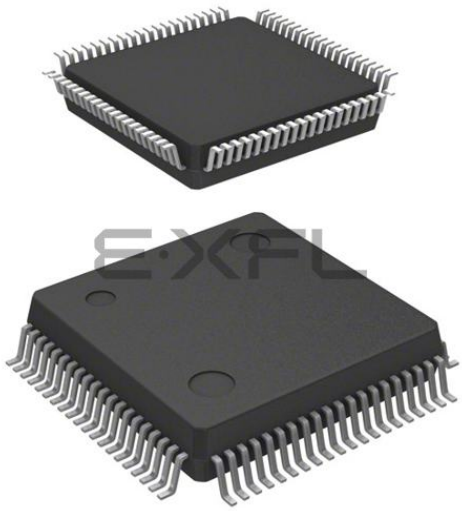

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	4MHz
Connectivity	I²C, IrDA, SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	52KB (52K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 3x10b, 2x14b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38086rh4v

Item	Page	Revision (See Manual for Details)
9.3.4 Pin Functions	176	Description amended

• P42/TXD31/IrTXD/TMOFH pin

TMOFH	0				1
SPC31	0		1		x
TE	x		x		x
IrE	x		0	1	x
PCR42	0	1	x	x	x
Pin Function	P42 input pin	P42 output pin	TXD31 output pin*	IrTXD output pin*	TMOFH output pin

[Legend] x: Don't care.

Note: * If SPC31 is set to 1 and TE is cleared to 0, the mark state is entered, 1 is output from the TXD32 output pin, and 0 is output from the IrTXD pin.

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• P40/SCK31/TMIF pin

TMIF	0					1
CKE1	0			1		x
CKE0	0		1	0	1	x
COM	0		1	x	x	x
PCR40	0	1	x	x	x	x
Pin Function	P40 input pin	P40 output pin	SCK31 output pin	SCK31 input pin	Setting prohibited	TMIF input pin

[Legend] x: Don't care.

9.8.4 Pin Functions	192	Description amended

• P92/$\overline{\text{IRQ4}}$ pin

IRQ4	0		1	
PCR92	0	1	0	1
Pin Function	P92 input pin	P92 output pin	$\overline{\text{IRQ4}}$ input pin	Setting prohibited

9.9.3 Pin Functions	194, 195	Replaced
9.10.3 Pin Functions	198	Description amended

• PB2/AN2/$\overline{\text{IRQ3}}$ pin

IRQ3	0		1
CH3 to CH0	Other than B'0110	B'0110	x
Pin Function	PB2 input pin	AN2 input pin	$\overline{\text{IRQ3}}$ input pin

[Legend] x: Don't care.

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• PB1/AN1/$\overline{\text{IRQ1}}$ pin

IRQ1	0		1
CH3 to CH0	Other than B'0101	B'0101	x
Pin Function	PB1 input pin	AN1 input pin	$\overline{\text{IRQ1}}$ input pin

[Legend] x: Don't care.

Type	Symbol	Pin No. FP-80A, TFP-80C	Pin No. TLP-85V	Pad No.*[1]	Pad No.*[2]	I/O	Functions
ΔΣ A/D converter	ACOM	66	C7	67	66	Output	Pins for stabilizing analog block voltage of the ΔΣ A/D converter. A capacitor should be connected between ΔΣ A/D converter and GND.
	REF	65	A7	66	65	Output	Output pins for internal reference voltage of the ΔΣ A/D converter. These pins output internal reference voltage.
	Vref	65	A7	66	65	Input	External reference voltage pins of the ΔΣ A/D converter. These pins input reference voltage.
	Ain2	64	B8	65	64	Input	Analog input pins for the ΔΣ A/D converter.
	Ain1	63	B9	64	63	Input	Analog input pins for the ΔΣ A/D converter.
I^2C bus interface 2 (IIC2)	SDA	6	D3	6	6	I/O	IIC data I/O pins.
	SCL	7	D2	7	7	I/O	IIC clock I/O pins.
LCD controller/ driver	COM1 to COM4	27 to 30	J4, K5, H5, J6	28 to 31	27 to 30	Output	LCD common output pins.
	SEG1 to SEG8	31 to 38	J5, H6, H7, K6, J7, J8, K7, H8	32 to 39	31 to 38	Output	LCD segment output pins.
	SEG9 to SEG16	39 to 46	K9, K8, J10 H10, J9, H9, G8	40 to 47	39 to 46	Output	
	SEG17 to SEG24	47 to 54	G9, F10, F8, E9, F9, E8, D8, E10	48 to 55	47 to 54	Output	
	SEG25 to SEG32	55 to 62	D9, C9, D10, C8, B10, C10, A9, A8	56 to 63	55 to 62	Output	

2.2 Register Configuration

The H8/300H CPU has the internal registers shown in figure 2.2. There are two types of registers; general registers and control registers. The control registers are a 24-bit program counter (PC), and an 8-bit condition-code register (CCR).

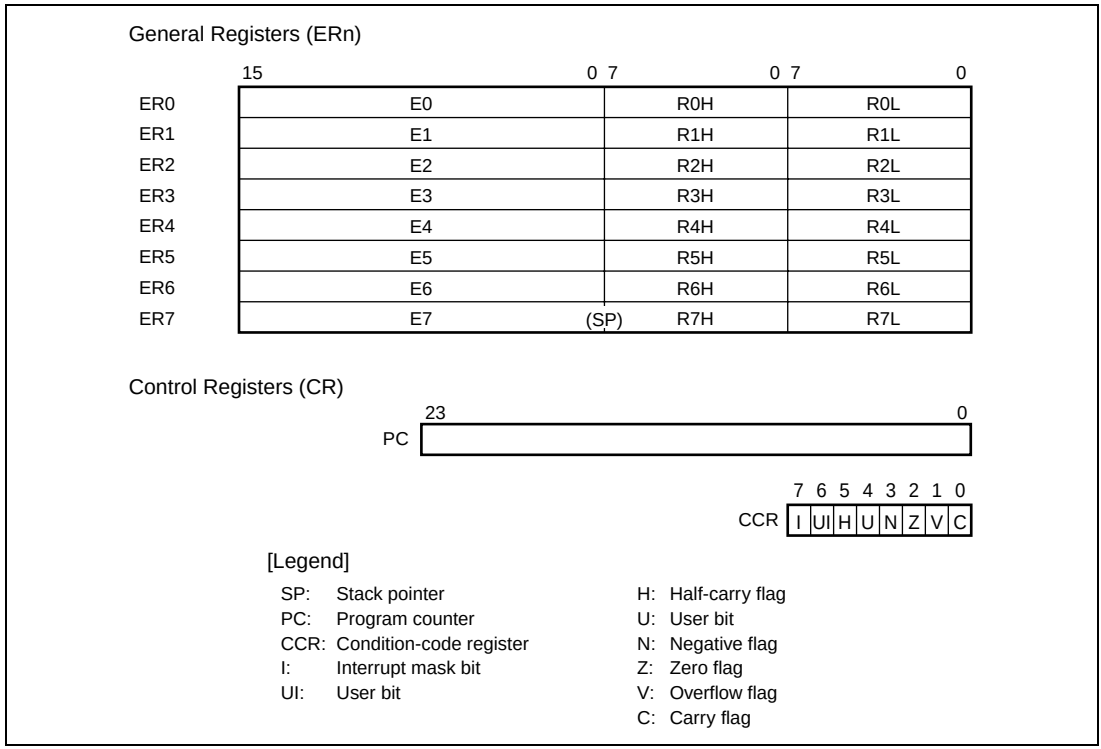


Figure 2.2 CPU Registers

Table 2.3 Arithmetic Operations Instructions (1)

Instruction	Size*	Function
ADD SUB	B/W/L	Rd ± Rs → Rd, Rd ± #IMM → Rd Performs addition or subtraction on data in two general registers, or on immediate data and data in a general register (immediate byte data cannot be subtracted from byte data in a general register. Use the SUBX or ADD instruction.)
ADDX SUBX	B	Rd ± Rs ± C → Rd, Rd ± #IMM ± C → Rd Performs addition or subtraction with carry on byte data in two general registers, or on immediate data and data in a general register.
INC DEC	B/W/L	Rd ± 1 → Rd, Rd ± 2 → Rd Increments or decrements a general register by 1 or 2. (Byte operands can be incremented or decremented by 1 only.)
ADDS SUBS	L	Rd ± 1 → Rd, Rd ± 2 → Rd, Rd ± 4 → Rd Adds or subtracts the value 1, 2, or 4 to or from data in a 32-bit register.
DAA DAS	B	Rd (decimal adjust) → Rd Decimal-adjusts an addition or subtraction result in a general register by referring to the CCR to produce 4-bit BCD data.
MULXU	B/W	Rd × Rs → Rd Performs unsigned multiplication on data in two general registers: either 8 bits × 8 bits → 16 bits or 16 bits × 16 bits → 32 bits.
MULXS	B/W	Rd × Rs → Rd Performs signed multiplication on data in two general registers: either 8 bits × 8 bits → 16 bits or 16 bits × 16 bits → 32 bits.
DIVXU	B/W	Rd ÷ Rs → Rd Performs unsigned division on data in two general registers: either 16 bits ÷ 8 bits → 8-bit quotient and 8-bit remainder or 32 bits ÷ 16 bits → 16-bit quotient and 16-bit remainder.

Note: * Refers to the operand size.
B: Byte
W: Word
L: Longword

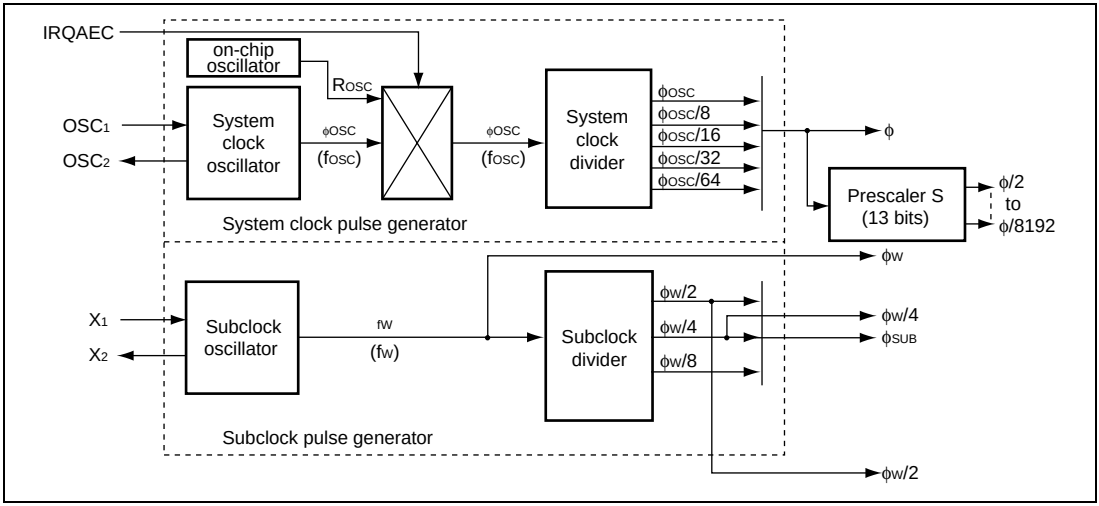


Figure 5.1 Block Diagram of Clock Pulse Generators (Masked ROM Version) (2)

The basic clock signals that drive the CPU and on-chip peripheral modules are ϕ and ϕ_{SUB}. The system clock is divided by prescaler S to become a clock signal from $\phi/8192$ to $\phi/2$. Both the system clock and subclock signals are provided to the on-chip peripheral modules.

Since the on-chip oscillator is available for the masked ROM version, the reference clock can be selected to be output from the on-chip oscillator or system clock oscillator by the input level of the IRQAEC pin.

6.1.2 System Control Register 2 (SYSCR2)

SYSCR2 controls the power-down modes, as well as SYSCR1.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.
4	NESEL	1	R/W	Noise Elimination Sampling Frequency Select The subclock pulse generator generates the watch clock signal (ϕ_w) and the system clock pulse generator generates the oscillator clock (ϕ_{osc}). This bit selects the sampling frequency of ϕ_{osc} when ϕ_w is sampled. When ϕ_{osc} = 2 to 10 MHz, clear this bit to 0. Set it to 1 if the internal oscillator is used. 0: Sampling rate is ϕ_{osc}/16. 1: Sampling rate is ϕ_{osc}/4.
3	DTON	0	R/W	Direct Transfer on Flag Selects the mode to which the transition is made after the SLEEP instruction is executed with bits SSBY, TMA3, and LSON in SYSCR1 and bit MSON in SYSCR2. For details, see table 6.2.
2	MSON	0	R/W	Medium Speed on Flag After standby, watch, or sleep mode is cleared, this bit selects active (high-speed) or active (medium-speed) mode. 0: Operation in active (high-speed) mode 1: Operation in active (medium-speed) mode
1	SA1	0	R/W	Subactive Mode Clock Select 1 and 0
0	SA0	0	R/W	Select the operating clock frequency in subactive and subsleep modes. The values of SA1 and SA0 do not change if they are written to in subactive mode. 00: ϕ_w/8 01: ϕ_w/4 1X: ϕ_w/2

[Legend] X: Don't care.

12.3.4 Timer Interrupt Enable Register (TIER)

TIER controls enabling or disabling of interrupt requests for each channel. The TPU has a total of two TIER registers, one for each channel.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R/W	Reserved This bit is readable/writable.
6	—	1	—	Reserved This bit is always read as 1 and cannot be modified.
5	—	0	—	Reserved The write value should always be 0.
4	TCIEV	0	R/W	Overflow Interrupt Enable Enables or disables interrupt requests (TCIV) by the TCFV flag when the TCFV flag in TSR is set to 1. 0: Interrupt requests (TCIV) by TCFV disabled 1: Interrupt requests (TCIV) by TCFV enabled
3, 2	—	All 0	—	Reserved These bits are always read as 0 and cannot be modified.
1	TGIEB	0	R/W	TGR Interrupt Enable B Enables or disables interrupt requests (TGIB) by the TGFB bit when the TGFB bit in TSR is set to 1. 0: Interrupt requests (TGIB) by TGFB bit disabled 1: Interrupt requests (TGIB) by TGFB bit enabled
0	TGIEA	0	R/W	TGR Interrupt Enable A Enables or disables interrupt requests (TGIA) by the TGFA bit when the TGFA bit in TSR is set to 1. 0: Interrupt requests (TGIA) by TGFA bit disabled 1: Interrupt requests (TGIA) by TGFA bit enabled

Note: Ndr and Ncm above must be set so that Ndr < Ncm. If the settings do not satisfy this condition, the output of the event counter PWM is fixed low.

Table 13.2 Examples of Event Counter PWM Operation

Conditions: fosc = 4 MHz, fϕ = 4 MHz, high-speed active mode, ECPWCR value (Ncm) = H'7A11, ECPWDR value (Ndr) = H'16E3

Clock Source Selection	Clock Source Cycle (T)*	ECPWCR Value (Ncm)	ECPWDR Value (Ndr)	toff = (T × (Ndr + 1)) – tcyc	tcm = T × (Ncm + 1)	ton = tcm – toff
ϕ/2	0.5 µs	H'7A11	H'16E3	2.92975 ms	15.625 ms	12.69525 ms
ϕ/4	1 µs	D'31249	D'5859	5.85975 ms	31.25 ms	25.39025 ms
ϕ/8	2 µs			11.71975 ms	62.5 ms	50.78025 ms
ϕ/16	4 µs			23.43975 ms	125.0 ms	101.56025 ms
ϕ/32	8 µs			46.87975 ms	250.0 ms	203.12025 ms
ϕ/64	16 µs			93.75975 ms	500.0 ms	406.24025 ms

Note: * toff minimum width

13.4.5 Operation of Clock Input Enable/Disable Function

The clock input to the event counter can be controlled by the IRQAEC pin when ECPWME in AEGSR is 0, and by the event counter PWM output, IECPWM when ECPWME in AEGSR is 1. As this function forcibly terminates the clock input by each signal, a maximum error of one count will occur depending on the IRQAEC or IECPWM timing. Figure 13.5 shows an example of the operation.

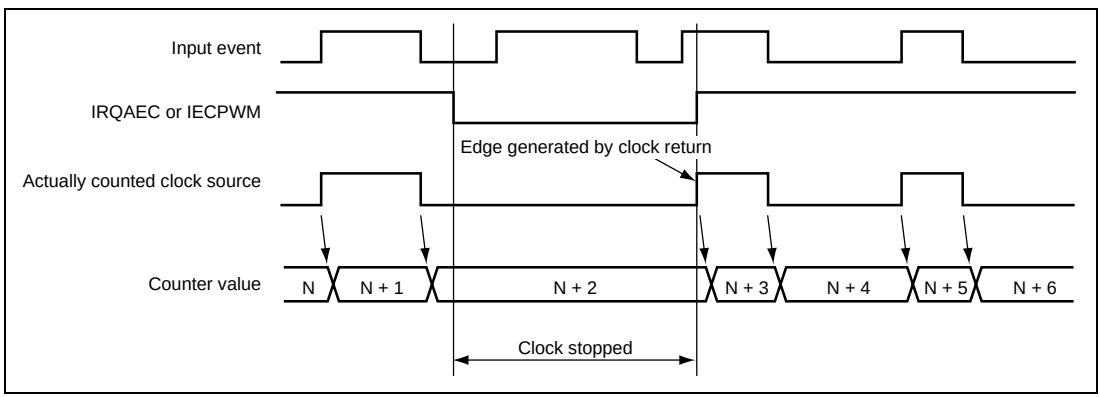


Figure 13.5 Example of Clock Control Operation

14.2.2 Timer Control/Status Register WD2 (TCSRWD2)

TCSRWD2 performs the TCSRWD2 write control, mode switching, and interrupt control. TCSRWD2 must be rewritten by using the MOV instruction. The bit manipulation instruction cannot be used to change the setting value.

Bit	Bit Name	Initial Value	R/W	Description
7	OVF	0	R/(W)*[1]	Overflow Flag Indicates that TCWD has overflowed (changes from H'FF to H'00). [Setting condition] When TCWD overflows (changes from H'FF to H'00) When internal reset request generation is selected in watchdog timer mode, this bit is cleared automatically by the internal reset after it has been set. [Clearing condition] • When TCSRWD2 is read when OVF = 1, then 0 is written to OVF*[4]
6	B5WI	1	R/(W)*[2]	Bit 5 Write Inhibit The WT/$\overline{IT}$ bit can be written only when the write value of the B5WI bit is 0. This bit is always read as 1.
5	WT/$\overline{IT}$	0	R/(W)*[3]	Timer Mode Select Selects whether the WDT is used as a watchdog timer or interval timer. 0: Watchdog timer mode 1: Interval timer mode
4	B3WI	1	R/(W)*[2]	Bit 3 Write Inhibit The IEOVF bit can be written only when the write value of the B3WI bit is 0. This bit is always read as 1.
3	IEOVF	0	R/(W)*[3]	Overflow Interrupt Enable Enables or disables an overflow interrupt request in interval timer mode. 0: Disables an overflow interrupt 1: Enables an overflow interrupt

14.3.2 Interval Timer Mode

Figure 14.3 shows the operation in interval timer mode. To use the WDT as an interval timer, set the WT/$\overline{IT}$ bit in TCSRWD2 to 1.

When the WDT is used as an interval timer, an interval timer interrupt request is generated each time the TCNT overflows. Therefore, an interval timer interrupt can be generated at intervals.

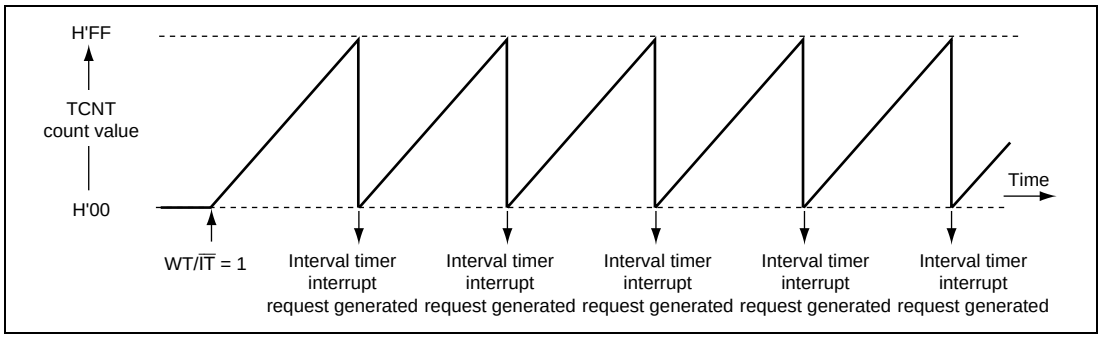


Figure 14.3 Interval Timer Mode Operation

14.3.3 Timing of Overflow Flag (OVF) Setting

Figure 14.4 shows the timing of the OVF flag setting. The OVF flag in TCSRWD2 is set to 1 if TCNT overflows. At the same time, a reset signal is output in watchdog timer mode and an interval timer interrupt is generated in interval timer mode.

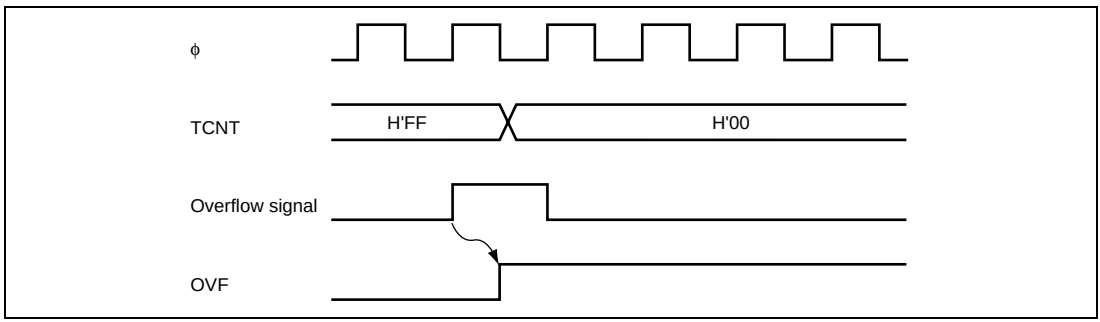


Figure 14.4 Timing of OVF Flag Setting

15.5.3 Serial Data Transmission

Figure 15.10 shows an example of SCI3 operation for transmission in clocked synchronous mode. In serial transmission, the SCI3 operates as described below.

1. The SCI3 monitors the TDRE flag in SSR, and if the flag is 0, the SCI recognizes that data has been written to TDR, and transfers the data from TDR to TSR.
2. The SCI3 sets the TDRE flag to 1 and starts transmission. If the TIE bit in SCR is set to 1 at this time, a TXI31 (TXI32) interrupt request is generated.
3. 8-bit data is sent from the TXD31 (TXD32) pin synchronized with the output clock when output clock mode has been specified, and synchronized with the input clock when use of an external clock has been specified. Serial data is transmitted sequentially from the LSB (bit 0), from the TXD31 (TXD32) pin.
4. The SCI checks the TDRE flag at the timing for sending the MSB (bit 7).
5. If the TDRE flag is cleared to 0, data is transferred from TDR to TSR, and serial transmission of the next frame is started.
6. If the TDRE flag is set to 1, the TEND flag in SSR is set to 1, and the TDRE flag maintains the output state of the last bit. If the TEIE bit in SCR is set to 1 at this time, a TEI31 (TEI32) is generated.
7. The SCK31 (SCK32) pin is fixed high.

Figure 15.11 shows a sample flowchart for serial data transmission. Even if the TDRE flag is cleared to 0, transmission will not start while a receive error flag (OER, FER, or PER) is set to 1. Make sure that the receive error flags are cleared to 0 before starting transmission.

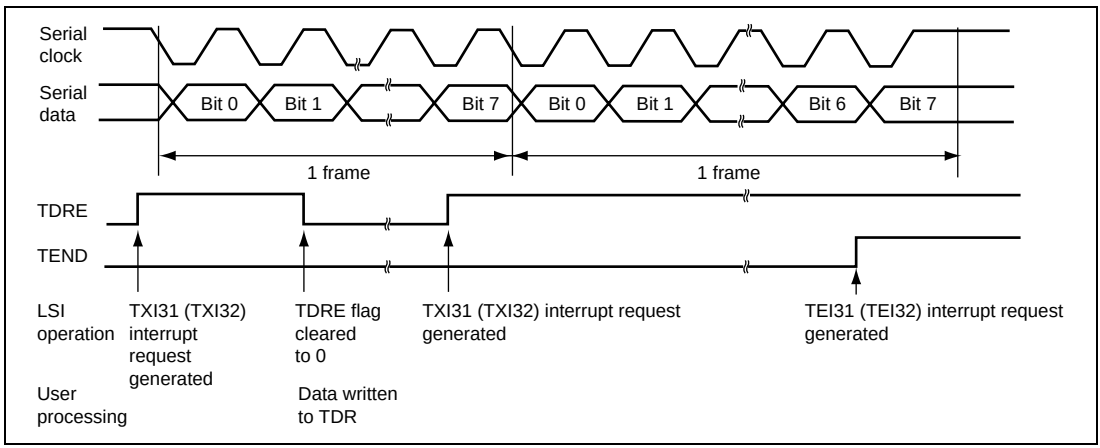


Figure 15.10 Example of SCI3 Operation in Transmission in Clocked Synchronous Mode

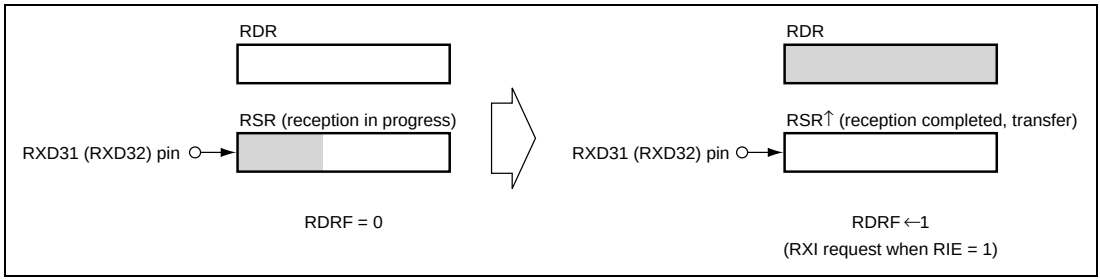


Figure 15.17 (a) RDRF Setting and RXI Interrupt

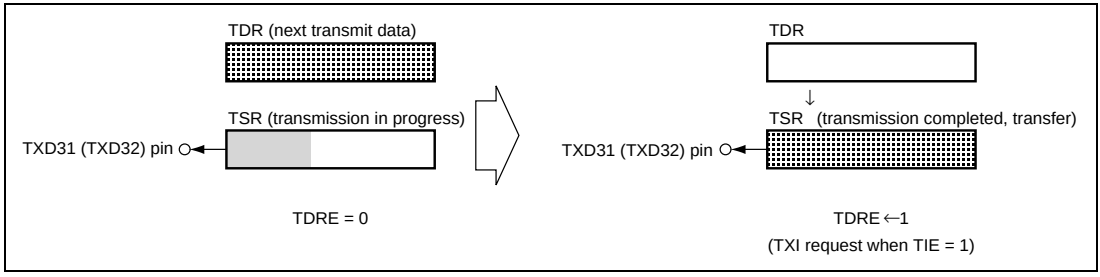


Figure 15.17 (b) TDRE Setting and TXI Interrupt

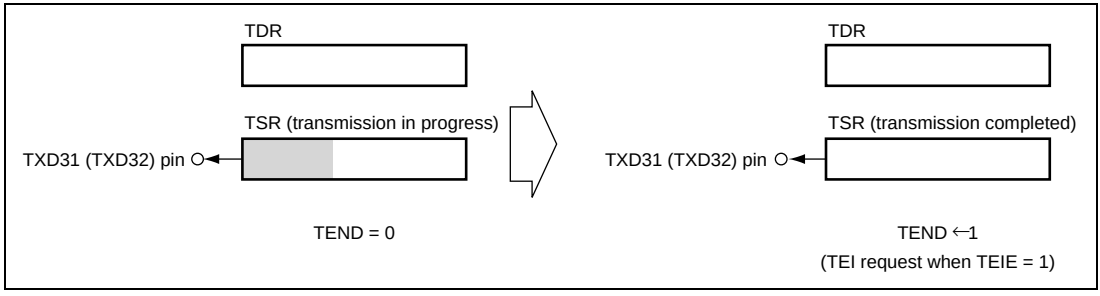


Figure 15.17 (c) TEND Setting and TEI Interrupt

15.8.4 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI3 operates on a basic clock with a frequency of 16 times the transfer rate. In reception, the SCI3 samples the falling edge of the start bit using the basic clock, and performs internal synchronization. Receive data is latched internally at the rising edge of the 8th pulse of the basic clock as shown in figure 15.18.

Thus, the reception margin in asynchronous mode is given by formula (1) below.

$$M = \left\{ (0.5 - \frac{1}{2N}) - \frac{D - 0.5}{N} - (L - 0.5)\,F \right\} \times 100(\%) \quad \text{... Formula (1)}$$

Where N: Ratio of bit rate to clock (N = 16)
D: Clock duty (D = 0.5 to 1.0)
L: Frame length (L = 9 to 12)
F: Absolute value of clock rate deviation

Assuming values of F (absolute value of clock rate deviation) = 0 and D (clock duty) = 0.5 in formula (1), the reception margin can be given by the formula.

$$M = \{0.5 - 1/(2 \times 16)\} \times 100\ [\%] = 46.875\%$$

However, this is only the computed value, and a margin of 20% to 30% should be allowed for in system design.

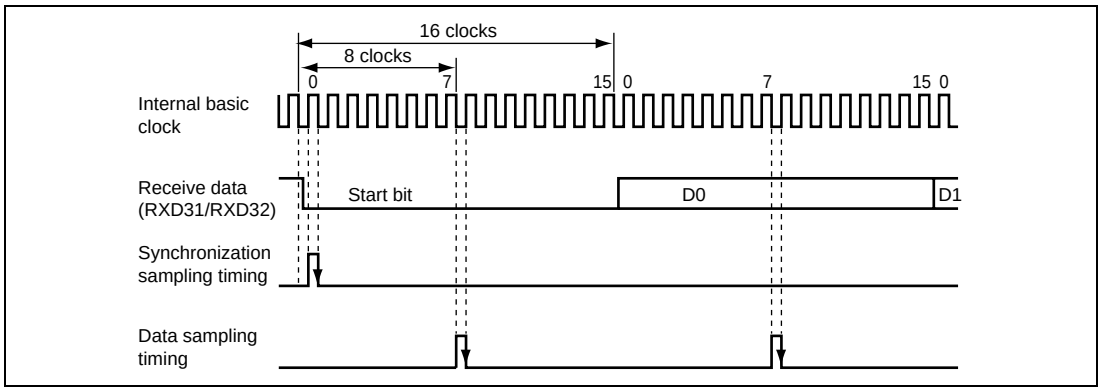
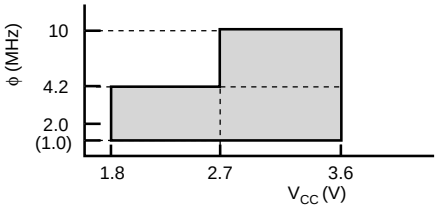


Figure 15.18 Receive Data Sampling Timing in Asynchronous Mode

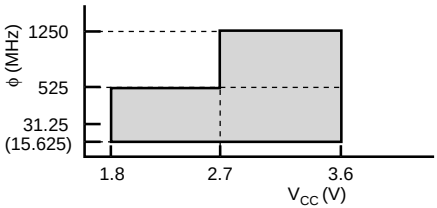
Bit	Bit Name	Initial Value	R/W	Description
2	BC2	0	R/W	Bit Counter 2 to 0
1	BC1	0	R/W	These bits specify the number of bits to be transferred next. When read, the remaining number of transfer bits is indicated. With the I²C bus format, the data is transferred with one addition acknowledge bit. Bit BC2 to BC0 settings should be made during an interval between transfer frames. If bits BC2 to BC0 are set to a value other than 000, the setting should be made while the SCL pin is low. The value returns to 000 at the end of a data transfer, including the acknowledge bit. With the clock synchronous serial format, these bits should not be modified.
0	BC0	0	R/W	

I²C Bus Format	Clock Synchronous Serial Format
000: 9 bits	000: 8 bits
001: 2 bits	001: 1 bits
010: 3 bits	010: 2 bits
011: 4 bits	011: 3 bits
100: 5 bits	100: 4 bits
101: 6 bits	101: 5 bits
110: 7 bits	110: 6 bits
111: 8 bits	111: 7 bits

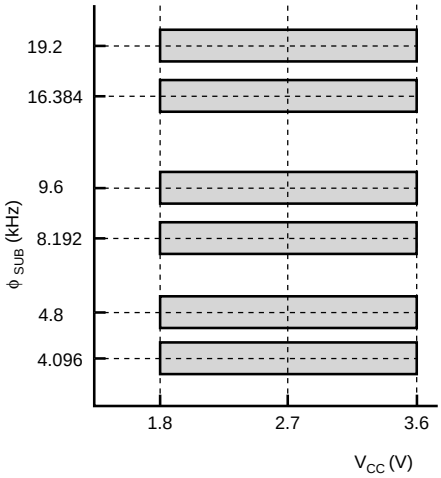
(2) Power Supply Voltage and Operating Frequency Range



- Active (high-speed) mode
- Sleep (high-speed) mode (except CPU)
- Refer to no.1 in the note.



- Active (medium-speed) mode
- Sleep (medium-speed) mode (except A/D converter)
- Refer to no.2 in the note.

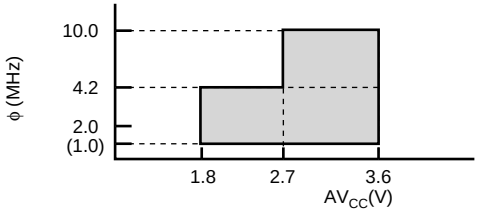


- Subactive mode
- Subsleep mode (except CPU)
- Watch mode (except CPU)

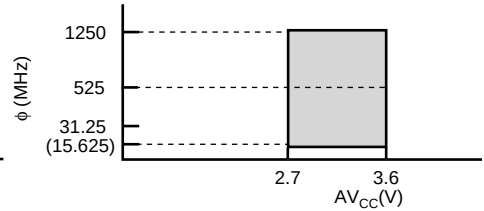
Notes: 1. The value in parentheses is the minimum operating frequency when an external clock is input. When using a resonator, the minimum operating frequency (ϕ) is 2 MHz.

2. The value in parentheses is the minimum operating frequency when an external clock is input. When using a resonator, the minimum operating frequency (ϕ) is 31.25 kHz.

(3) Analog Power Supply Voltage and A/D Converter Operating Frequency Range



- Active (high-speed) mode
- Sleep (high-speed) mode
- Refer to no.1 in the note.



- Active (medium-speed) mode
- Sleep (medium-speed) mode
- Refer to no.2 in the note.

Notes: 1. The minimum operating frequency (ϕ) is 2 MHz when using a resonator; and 1 MHz when using an external clock.

2. The minimum operating frequency (ϕ) is 31.25 kHz when using a resonator; and 15.625 kHz when using an external clock.

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Differential lineality error			PGA bypass (DV_{cc} = 3.0 V, V_{ref} = 2.7 V, conversion speed = 32 µs)*6	—	1.3	—	LSB	*7
				—	-0.8	—		
Offset error			PGA bypass (DV_{cc} = 3.0 V, V_{ref} = 2.7 V, conversion speed = 32 µs)*6	—	10	—	mV	*7
Full scale error			PGA bypass (DV_{cc} = 3.0 V, V_{ref} = 2.7 V, conversion speed = 32 µs)*6	—	28.0	—	mV	*7
PGA gain				—	1/3	—	V/V	
				—	1	—	V/V	
				—	2	—	V/V	
				—	4	—	V/V	
PGA gain error	Tad		PGA = 1/3, DV_{cc} = 3.0 V	—	6	—	mV	*7
			PGA = 1, DV_{cc} = 3.0 V	—	7	—	mV	
			PGA = 2, DV_{cc} = 3.0 V	—	-20	—	mV	
			PGA = 4, DV_{cc} = 3.0 V	—	-44	—	mV	
Internal reference voltage		REF		—	1.17	—	V	*4 *5
External reference voltage		V_{ref}		0.2 DV_{cc}	—	0.9 DV_{cc}	V	

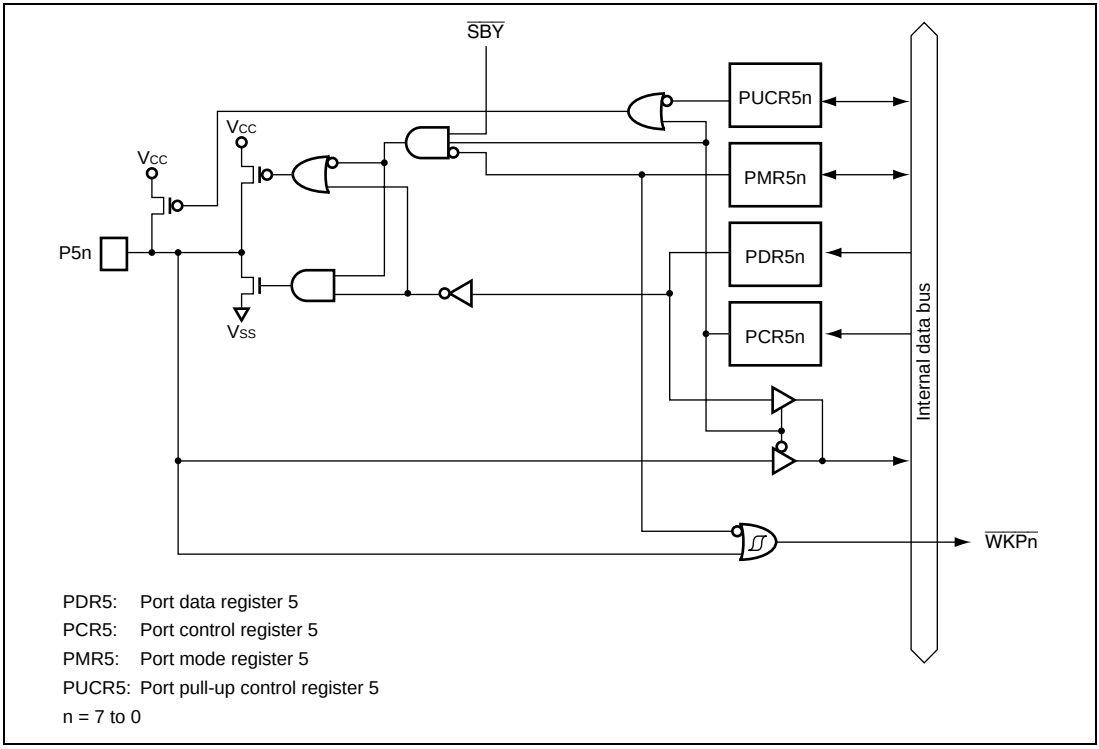
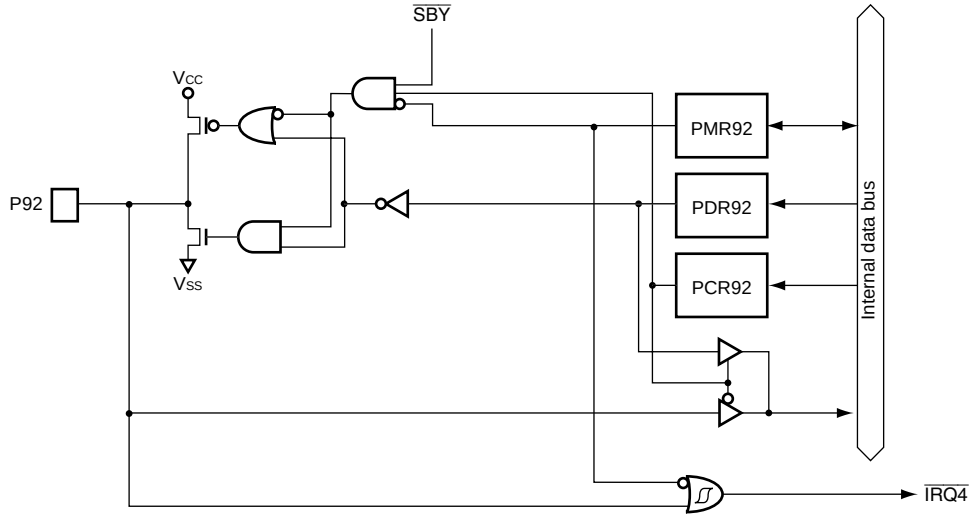


Figure B.4 Port 5 Block Diagram



PDR9: Port data register 9
PCR9: Port control register 9
PMR9: Port mode register 9

Figure B.8 (b) Port 9 Block Diagram (P92)

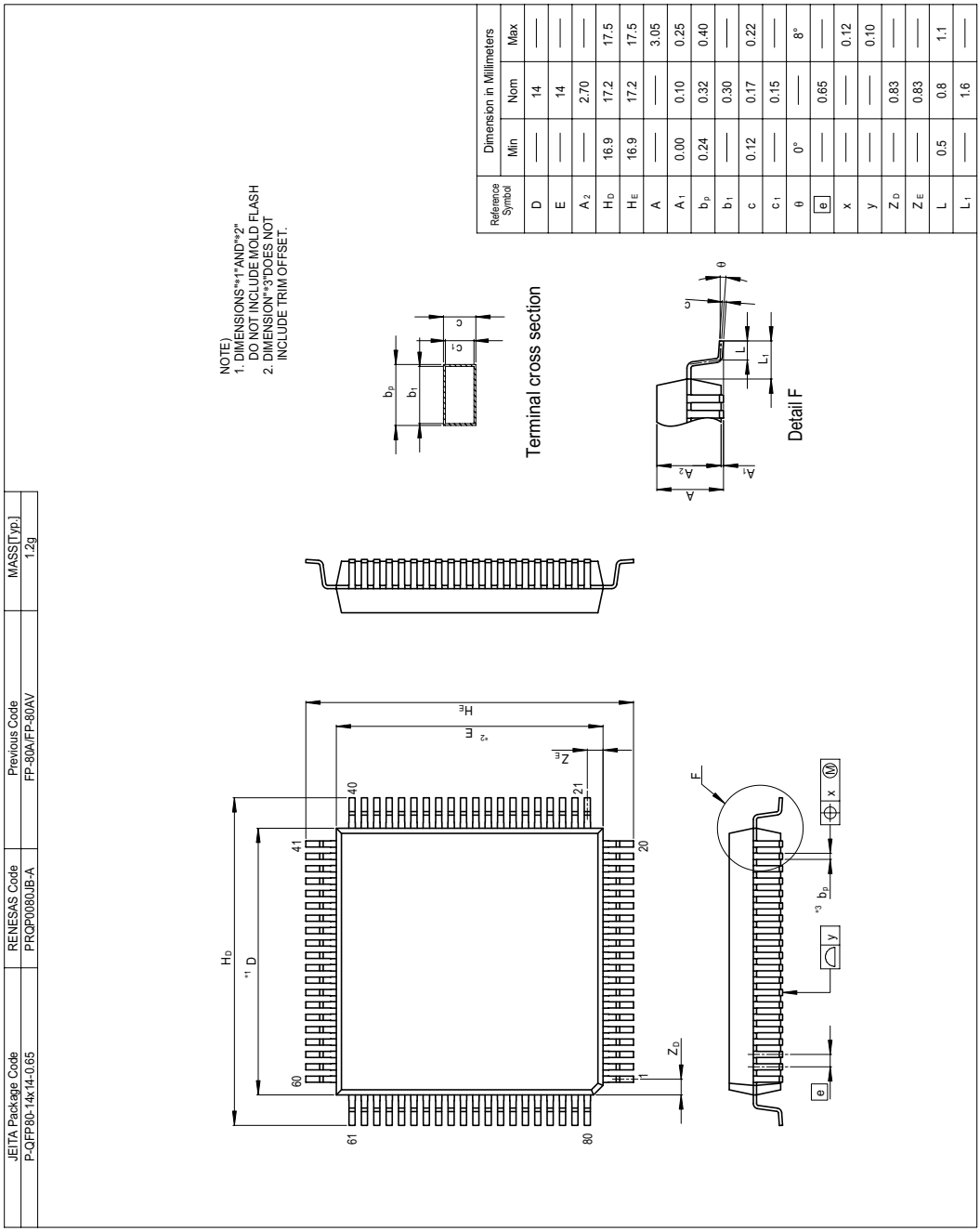


Figure D.1 Package Dimensions (FP-80A)