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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	10MHz
Connectivity	I²C, IrDA, SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	52KB (52K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 3x10b, 2x14b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38086rw10v

Item	Page	Revision (See Manual for Details)
6.1.1 System Control Register 1 (SYSCR1)	112	Table amended

Bit	Bit Name	Initial Value	R/W	Description
6	STS2	0	R/W	When an external clock is to be used, the minimum value (STS2 = 1, STS1 = 0, STS0 = 1) is recommended. If the internal oscillator is used, the settings CTCS2 = 0, STS = 1, and STS0 = 0 are recommended. If the setting other than the recommended value is made, operation may start before the end of the waiting time.
5	STS1	0	R/W	
4	STS0	0	R/W	

6.1.2 System Control Register 2 (SYSCR2)	114	Table amended

Bit	Bit Name	Initial Value	R/W	Description
4	NESEL	1	R/W	Noise Elimination Sampling Frequency Select The subclock pulse generator generates the watch clock signal (ϕ_w) and the system clock pulse generator generates the oscillator clock (ϕ_{osc}). This bit selects the sampling frequency of ϕ_{osc} when ϕ_w is sampled. When ϕ_{osc} = 2 to 10 MHz, clear this bit to 0. Set it to 1 if the internal oscillator is used. 0: Sampling rate is ϕ_{osc}/16. 1: Sampling rate is ϕ_{osc}/4.
1	SA1	0	R/W	Subactive Mode Clock Select 1 and 0
0	SA0	0	R/W	Select the operating clock frequency in subactive and subsleep modes. The values of SA1 and SA0 do not change if they are written to in subactive mode. 00: ϕ_w/8 01: ϕ_w/4 1X: ϕ_w/2

6.1.3 Clock Halt Registers 1 and 2 (CKSTPR1 and CKSTPR2)	115	Table amended

Bit	Bit Name	Initial Value	R/W	Description
7	S4CKSTP*1*4	1	R/W*1	SCI4 Module Standby SCI4 enters standby mode when this bit is cleared to 0.
1	FROMCKSTP*1*4	1	R/W	Flash Memory Module Standby Flash memory enters standby mode when this bit is cleared to 0.

Type	Symbol	Pin No. FP-80A, TFP-80C	Pin No. TLP-85V	Pad No.*[1]	Pad No.*[2]	I/O	Functions
I/O ports	PA0 to PA3	27 to 30	J4, K5, H5, J6	28 to 31	27 to 30	I/O	4-bit I/O pins. Input or output can be designated for each bit by means of the port control register A (PCRA).
	PB0 to PB2, PB5 to PB7	72 to 70, 65 to 63	C5, B6, B5, A7, B8, B9	73 to 71, 66 to 64	72 to 70 65 to 63	Input	6-bit input-only pins

Notes: 1. Pad no. for the flash memory version.
2. Pad no. for the masked ROM version.

2.4 Instruction Set

2.4.1 Table of Instructions Classified by Function

The H8/300H CPU has 62 instructions. Tables 2.2 to 2.9 summarize the instructions in each functional category. The notation used in tables 2.2 to 2.9 is defined in table 2.1.

Table 2.1 Operation Notation

Symbol	Description
Rd	General register (destination)*
Rs	General register (source)*
Rn	General register*
ERn	General register (32-bit register or address register)
(EAd)	Destination operand
(EAs)	Source operand
CCR	Condition-code register
N	N (negative) flag in CCR
Z	Z (zero) flag in CCR
V	V (overflow) flag in CCR
C	C (carry) flag in CCR
PC	Program counter
SP	Stack pointer
#IMM	Immediate data
disp	Displacement
+	Addition
–	Subtraction
×	Multiplication
÷	Division
∧	Logical AND
∨	Logical OR
⊕	Logical XOR
→	Move
¬	NOT (logical complement)

4.2 Input/Output Pins

Table 4.1 shows the pin configuration of the interrupt controller.

Table 4.1 Pin Configuration

Name	I/O	Function
$\overline{\text{NMI}}$	Input	Nonmaskable external interrupt pin Rising or falling edge can be selected
IRQAEC	Input	Maskable external interrupt pin Rising, falling, or both edges can be selected
$\overline{\text{IRQ4}}$	Input	Maskable external interrupt pins Rising or falling edge can be selected
$\overline{\text{IRQ3}}$	Input	
$\overline{\text{IRQ1}}$	Input	
$\overline{\text{IRQ0}}$	Input	
$\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$	Input	Maskable external interrupt pins Accepted at a rising or falling edge

4.3 Register Descriptions

The interrupt controller has the following registers.

- Interrupt edge select register (IEGR)
- Wakeup edge select register (WEGR)
- Interrupt enable register 1 (IENR1)
- Interrupt enable register 2 (IENR2)
- Interrupt request register 1 (IRR1)
- Interrupt request register 2 (IRR2)
- Wakeup interrupt request register (IWPR)
- Interrupt priority register A (IPRA)
- Interrupt priority register B (IPRB)
- Interrupt priority register C (IPRC)
- Interrupt priority register D (IPRD)
- Interrupt priority register E (IPRE)
- Interrupt mask register (INTM)

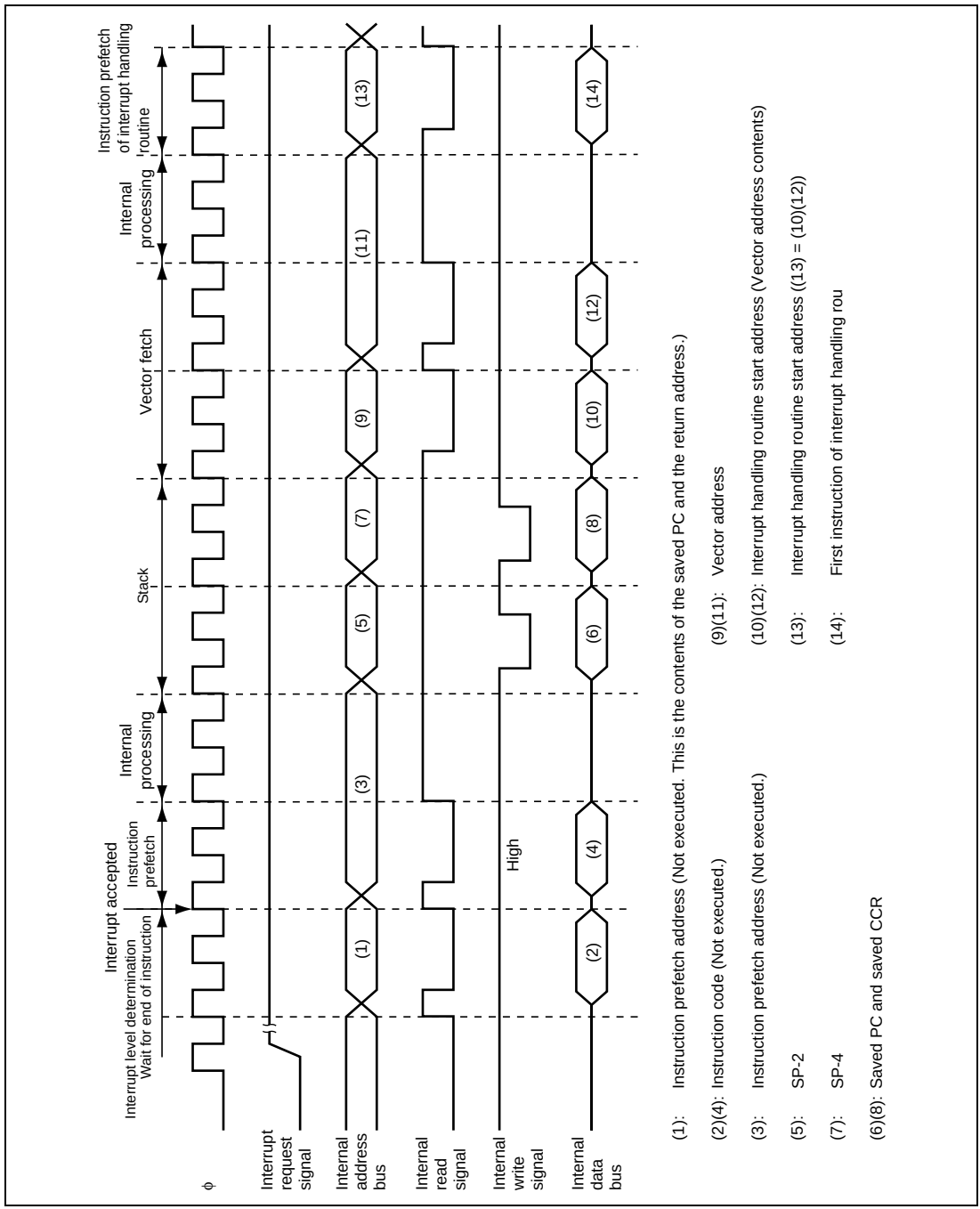


Figure 4.3 Interrupt Exception Handling Sequence

10.3.4 Day-of-Week Data Register (RWKDR)

RWKDR counts the BCD-coded day-of-week value on the carry generated once per day by RHRDR. The setting range is decimal 0 to 6 using bits WK2 to WK0.

Bit	Bit Name	Initial Value	R/W	Description
7	BSY	—	R	RTC Busy This bit is set to 1 when the RTC is updating (operating) the values of second, minute, hour, and day-of-week data registers. When this bit is 0, the values of second, minute, hour, and day-of-week data registers must be adopted.
6 to 3	—	All 0	—	Reserved These bits are always read as 0.
2	WK2	—	R/W	Day-of-Week Counting
1	WK1	—	R/W	Day-of-week is indicated with a binary code
0	WK0	—	R/W	000: Sunday 001: Monday 010: Tuesday 011: Wednesday 100: Thursday 101: Friday 110: Saturday 111: Setting prohibited

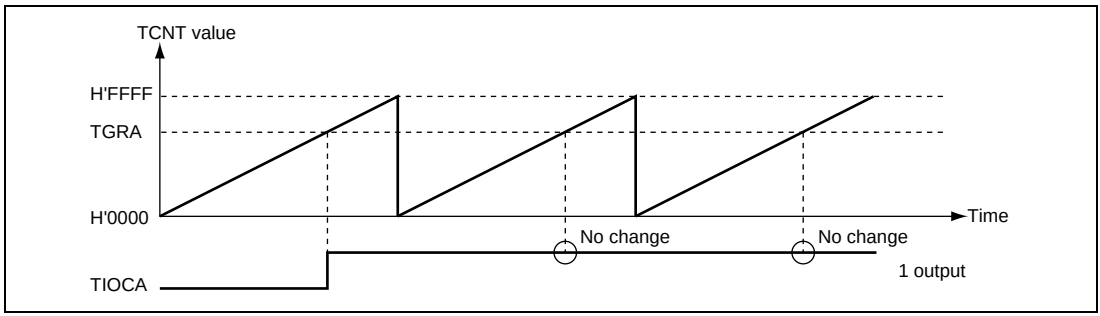


Figure 12.9 Example of 0 Output/1 Output Operation

Figure 12.10 shows an example of toggle output.

In this example, TCNT has been designated as a periodic counter (with counter clearing on compare match A), and settings have been made such that the output is toggled by compare match A.

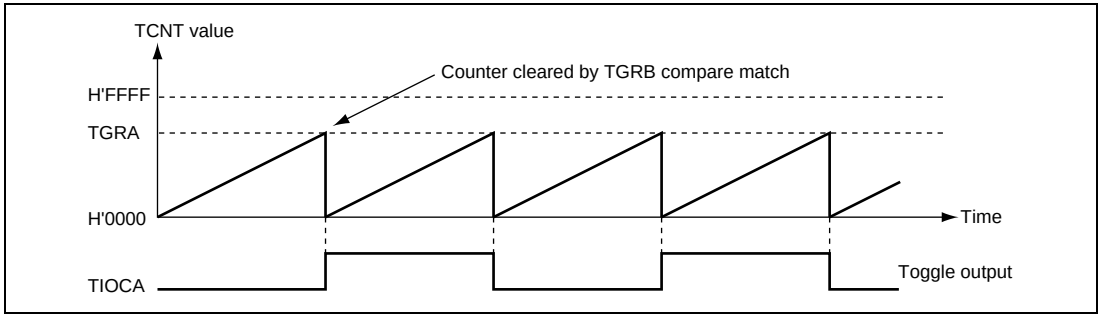


Figure 12.10 Example of Toggle Output Operation

(3) Input Capture Function

The TCNT value can be transferred to TGR on detection of the TIOC pin input edge.

Rising edge, falling edge, or both edges can be selected as the detected edge.

(a) Example of Input Capture Operation Setting Procedure

Figure 12.11 shows an example of the setting procedure for input capture operation.

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	—	All 1	—	Reserved These bits are always read as 1.

Notes: 1. Only 0 can be written to clear the flag.
2. Write operation is necessary because this bit controls data writing to other bit. This bit is always read as 1.
3. Writing is possible only when the write conditions are satisfied.
4. In subactive mode, clear this flag after setting the CKS3 to CKS0 bits in TMWD to B'0XXX (WDT on-chip oscillator).

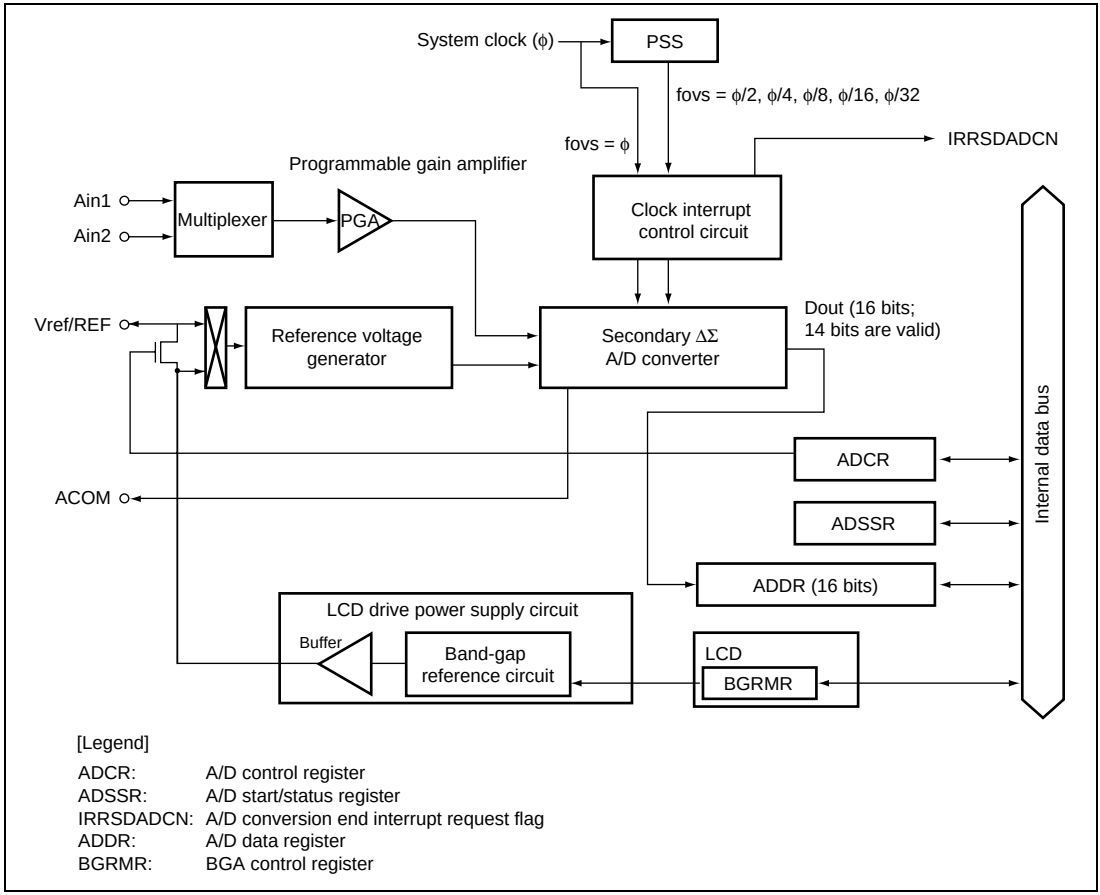


Figure 19.1 Block Diagram of ΔΣ A/D Converter

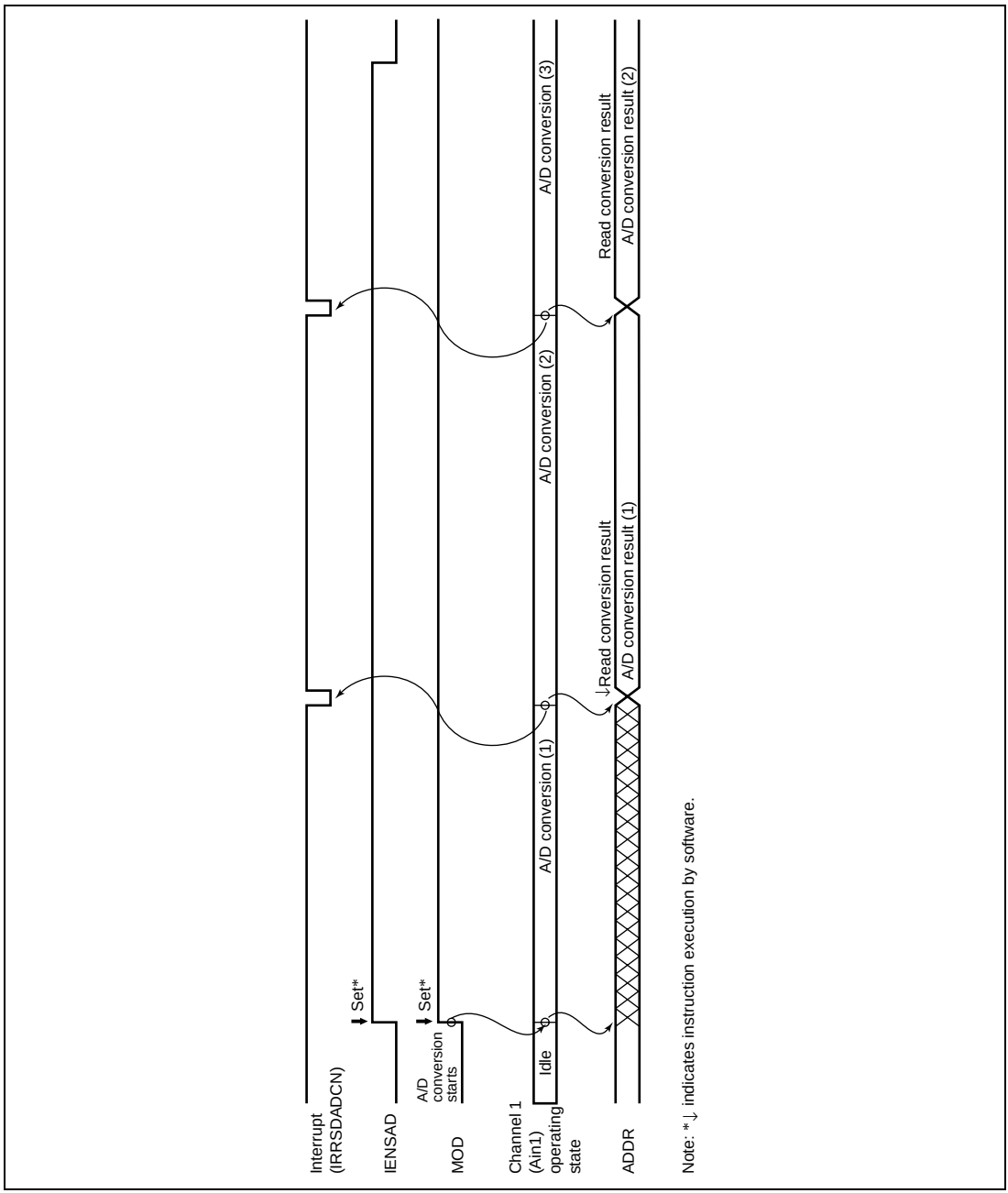


Figure 19.5 Example of ΔΣ A/D Conversion Operation (Continuous Mode)

Figure 20.8 shows a output waveforms for each duty cycle (B waveform).

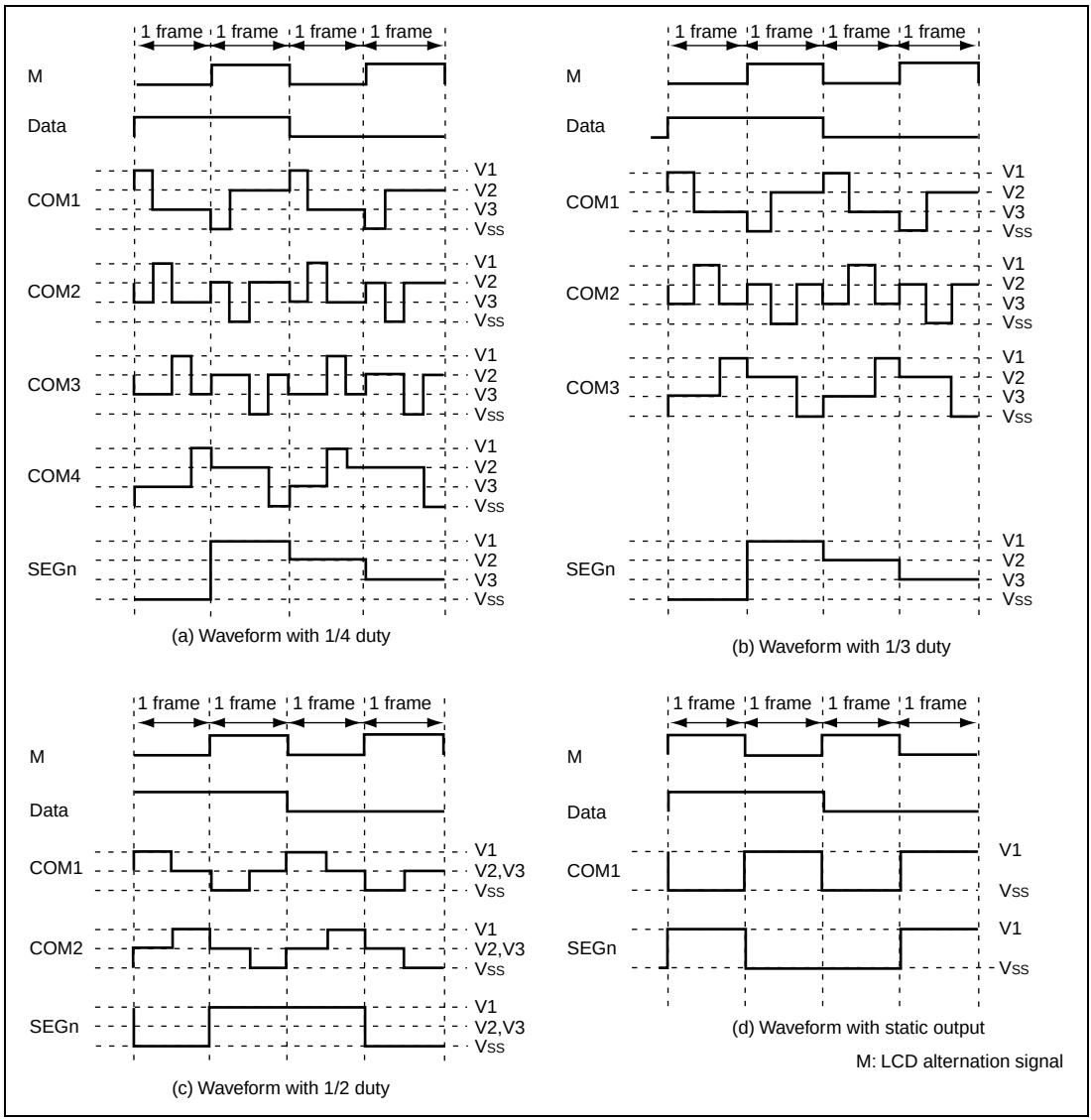


Figure 20.8 Output Waveforms for Each Duty Cycle (B Waveform)

(3) Receive Operation

In receive mode, data is latched at the rise of the transfer clock. The transfer clock is output when MST in ICCR1 is 1, and is input when MST is 0. For receive mode operation timing, refer to figure 21.15. The reception procedure and operations in receive mode are described below.

1. Set the ICE bit in ICCR1 to 1. Set the MST and CKS3 to CKS0 bits in ICCR1 to 1. (Initial setting)
2. When the transfer clock is output, set MST to 1 to start outputting the receive clock.
3. When the receive operation is completed, data is transferred from ICDRS to ICDRR and RDRF in ICSR is set. When MST = 1, the next byte can be received, so the clock is continually output. The continuous reception is performed by reading ICDRR every time RDRF is set. When the 8th clock is risen while RDRF is 1, the overrun is detected and AL/OVE in ICSR is set. At this time, the previous reception data is retained in ICDRR.
4. To stop receiving when MST = 1, set RCVD in ICCR1 to 1, then read ICDRR. Then, SCL is fixed high after receiving the next byte data.

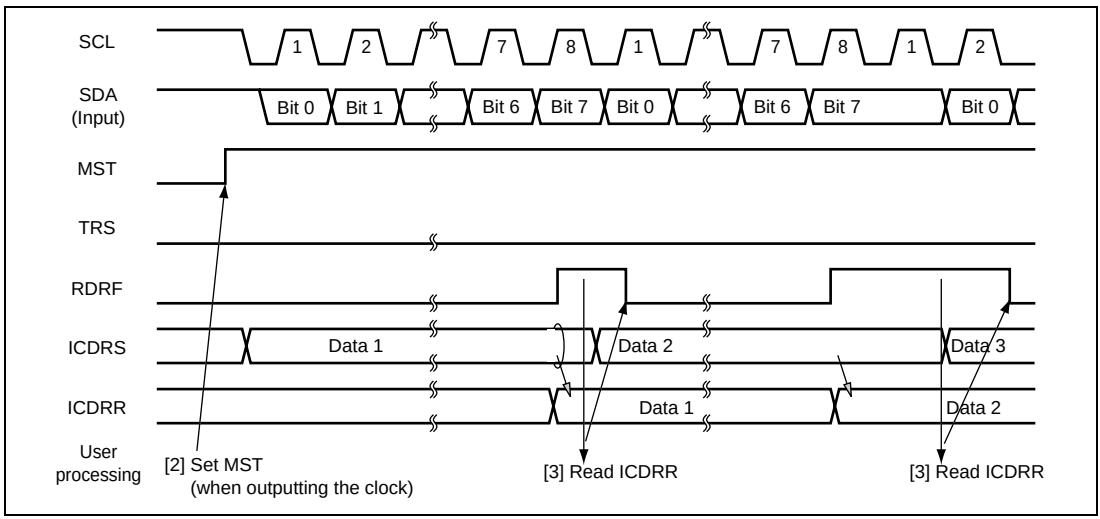


Figure 21.15 Receive Mode Operation Timing

Register Name	Abbre-viation	Bit No.	Address	Module Name	Data Bus Width	Access State
Timer general register A_2	TGRA_2	16	H'F058	TPU_2	16	2
Timer general register B_2	TGRB_2	16	H'F05A	TPU_2	16	2
A/D control register	ADCR	8	H'F060	ΔΣ A/D converter	8	2
A/D start/status register	ADSSR	8	H'F061	ΔΣ A/D converter	8	2
A/D data register	ADDR	16	H'F062	ΔΣ A/D converter	16	2
RTC interrupt flag register	RTCFLG	8	H'F067	RTC	8	2
Second data register/free running counter data register	RSECDR	8	H'F068	RTC	8	2
Minute data register	RMINDR	8	H'F069	RTC	8	2
Hour data register	RHRDR	8	H'F06A	RTC	8	2
Day-of-week data register	RWKDR	8	H'F06B	RTC	8	2
RTC control register 1	RTCCR1	8	H'F06C	RTC	8	2
RTC control register 2	RTCCR2	8	H'F06D	RTC	8	2
SUB32k control register	SUB32CR	8	H'F06E	Clock pulse generator	8	2
Clock source select register	RTCCSR	8	H'F06F	RTC	8	2
I^2C bus control register 1	ICCR1	8	H'F078	IIC2	8	2
I^2C bus control register 2	ICCR2	8	H'F079	IIC2	8	2
I^2C bus mode register	ICMR	8	H'F07A	IIC2	8	2
I^2C bus interrupt enable register	ICIER	8	H'F07B	IIC2	8	2
I^2C bus status register	ICSR	8	H'F07C	IIC2	8	2
Slave address register	SAR	8	H'F07D	IIC2	8	2
I^2C bus transmit data register	ICDRT	8	H'F07E	IIC2	8	2
I^2C bus receive data register	ICDRR	8	H'F07F	IIC2	8	2
Interrupt priority register A	IPRA	8	H'F080	Interrupts	8	2
Interrupt priority register B	IPRB	8	H'F081	Interrupts	8	2
Interrupt priority register C	IPRC	8	H'F082	Interrupts	8	2
Interrupt priority register D	IPRD	8	H'F083	Interrupts	8	2
Interrupt priority register E	IPRE	8	H'F084	Interrupts	8	2

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Allowable output low current (per pin)	I_{OL}	Output pins except port 9		—	—	0.5	mA	
		P90 to P93		—	—	15.0		
Allowable output low current (total)	$\sum I_{OL}$	Output pins except port 9		—	—	20.0	mA	
		Port 9	—	—	—	60.0		
Allowable output high current (per pin)	$-I_{OH}$	All output pins	V_{CC} = 2.7 V to 3.6 V	—	—	2.0	mA	
			V_{CC} = 1.8 V to 3.6 V	—	—	0.2		
Allowable output high current (total)	$\sum -I_{OH}$	All output pins		—	—	10.0	mA	

Notes: 1. Pin states during current measurement.

Mode	$\overline{RES}$ Pin	Internal State	Other Pins	LCD Power Supply	Oscillator Pins
Active (high-speed) mode (I_{OPE1})	V_{CC}	Only CPU operates On-chip WDT oscillator is off	V_{CC}	Halted	System clock oscillator: crystal resonator Subclock oscillator: Pin X1 = GND
Active (medium-speed) mode (I_{OPE2})					
Sleep mode	V_{CC}	Only on-chip timers operate On-chip WDT oscillator is off	V_{CC}	Halted	
Subactive mode	V_{CC}	Only CPU operates On-chip WDT oscillator is off	V_{CC}	Halted	System clock oscillator: crystal resonator Subclock oscillator: crystal resonator
Subsleep mode	V_{CC}	Only on-chip timers operate, CPU stops On-chip WDT oscillator is off	V_{CC}	Halted	
Watch mode	V_{CC}	Only time base operates, CPU stops On-chip WDT oscillator is off TCSRWD1 (WDON) = 0	V_{CC}	Halted	
Standby mode	V_{CC}	CPU and timers both stop On-chip WDT oscillator is off TCSRWD1 (WDON) = 0	V_{CC}	Halted	System clock oscillator: crystal resonator Subclock oscillator: Pin X1 = GND (32KSTOP = 0)

2. Excludes current in pull-up MOS transistors and output buffers.
3. Except for the package for the TLP-85V.
4. Supported only by the 4MHz version.

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Output low voltage	V_{OL}	P10 to P16, P30 to P32, P36, P37, P40 to P42, P50 to P57, P60 to P67, P70 to P77, P80 to P87, PA0 to PA3	I_{OL} = 0.4 mA	—	—	0.5	V	
		P90 to P93	I_{OL} = 15 mA V_{CC} = 2.7 to 3.6 V	—	—	1.0		
			I_{OL} = 10 mA V_{CC} = 2.2 to 3.6 V	—	—	0.5		
			I_{OL} = 8.0 mA V_{CC} = 1.8 to 3.6 V	—	—	0.5		
		SCL, SDA	V_{CC} = 2.0 to 3.6 V I_{OL} = 3.0 mA	—	—	0.4	V	
			V_{CC} = 1.8 to 2.0 V I_{OL} = 3.0 mA	—	—	$0.2V_{CC}$		
Input/output leakage current	$\lvert I_{IL} \rvert$	$\overline{NMI}$, OSC1, X1, P10 to P16, P30 to P32, P36, P37, P40 to P42, P50 to P57, P60 to P67, P70 to P77, P80 to P87, IRQAEC, PA0 to PA3, P90 to P93	V_{IN} = 0.5 V to V_{CC} – 0.5 V	—	—	1.0	µA	
		PB0 to PB2, PB5 to PB7	V_{IN} = 0.5 V to AV_{CC} – 0.5 V	—	—	1.0		
Pull-up MOS current	$-I_p$	P10 to P16, P30, P36, P37, P50 to P57, P60 to P67	V_{CC} = 3.0 V, V_{IN} = 0 V	30	—	180	µA	
Input capacitance*[3]	C_{IN}	All input pins except power supply pin	f = 1 MHz, V_{IN} =0 V, Ta = 25°C	—	—	15.0	pF	

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Active mode current consumption	I_{OPE1}	V_{CC}	Active (high-speed) mode, V_{CC} = 1.8 V, f_{OSC} = 2 MHz	—	0.7	—	mA	*1*2 Max. guideline = 1.1 × typ.
			Active (high-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 4 MHz	—	2.6	—		*1*2 Max. guideline = 1.1 × typ.
			Active (high-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	6.6	10.0		*1*2
	I_{OPE2}	V_{CC}	Active (medium-speed) mode, V_{CC} = 1.8 V, f_{OSC} = 2 MHz, ϕ_{osc}/64	—	0.2	—	mA	*1*2 Max. guideline = 1.1 × typ.
			Active (medium-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 4 MHz, ϕ_{osc}/64	—	0.4	—		*1*2 Max. guideline = 1.1 × typ.
			Active (medium-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 10 MHz, ϕ_{osc}/64	—	0.8	1.8		*1*2
Sleep mode current consumption	I_{SLEEP}	V_{CC}	V_{CC} = 1.8 V, f_{OSC} = 2 MHz	—	0.3	—	mA	*1*2 Max. guideline = 1.1 × typ.
			V_{CC} = 3.0 V, f_{OSC} = 4 MHz	—	1.2	—		*1*2 Max. guideline = 1.1 × typ.
			V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	3.0	5.0		*1*2

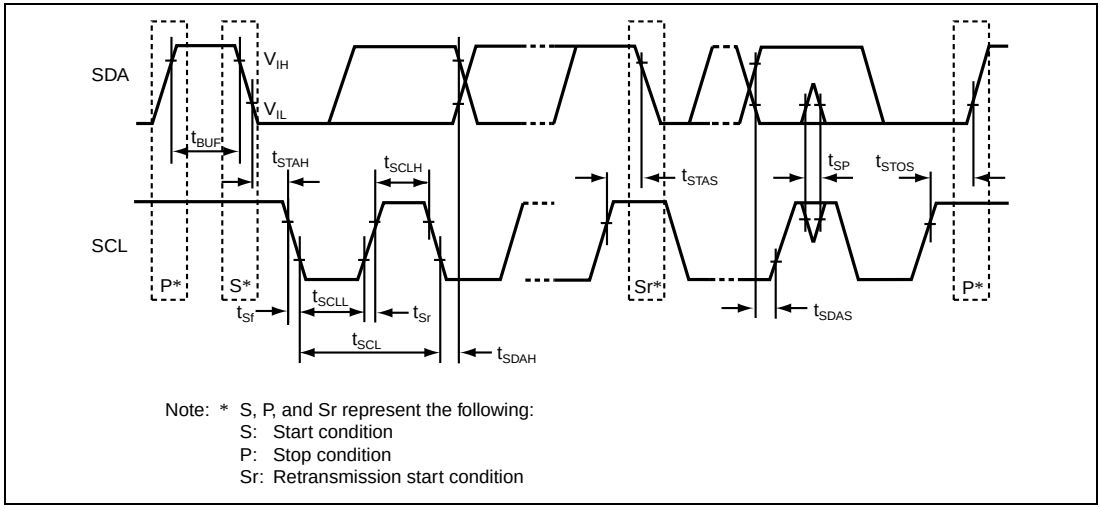


Figure 25.8 I²C Bus Interface Input/Output Timing

25.6 Output Load Circuit

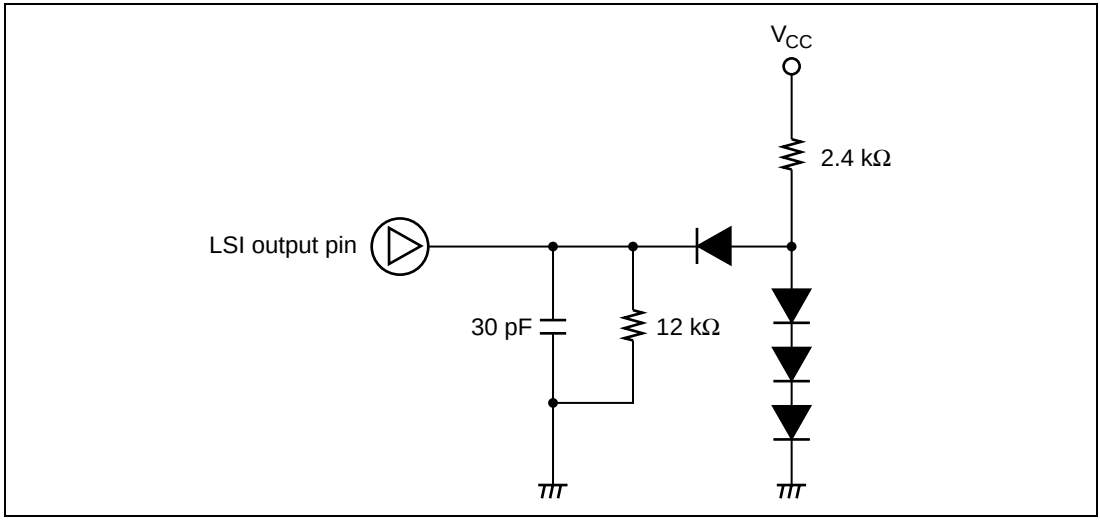
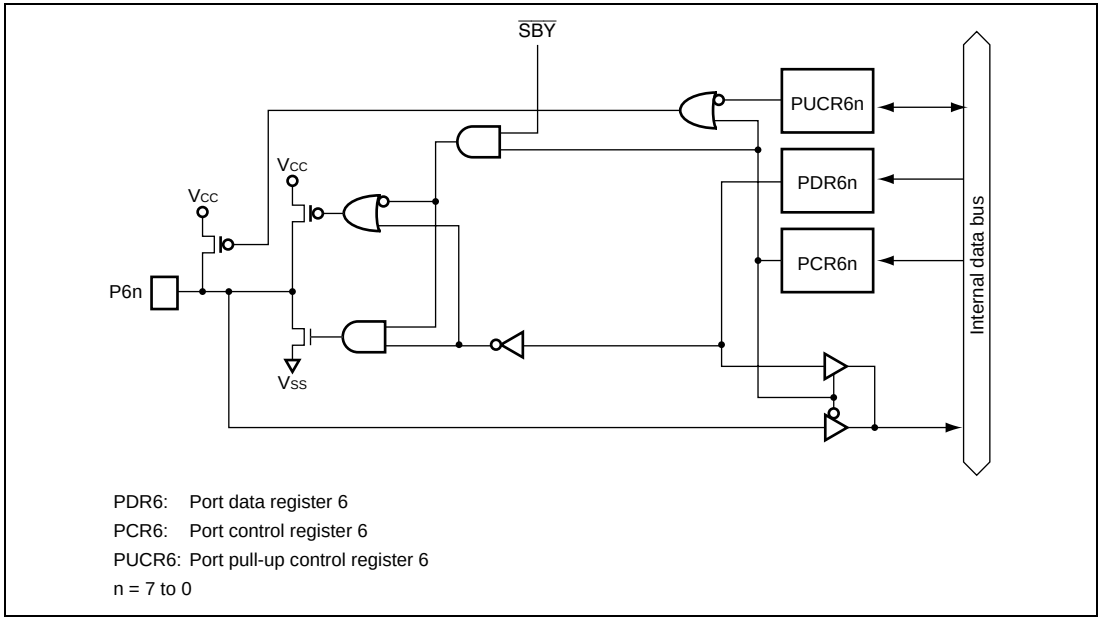


Figure 25.9 Output Load Condition

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
SUBX	SUBX #xx:8, Rd	1					
	SUBX. Rs, Rd	1					
XOR	XOR.B #xx:8, Rd	1					
	XOR.B Rs, Rd	1					
	XOR.W #xx:16, Rd	2					
	XOR.W Rs, Rd	1					
	XOR.L #xx:32, ERd	3					
	XOR.L ERs, ERd	2					
XORC	XORC #xx:8, CCR	1					

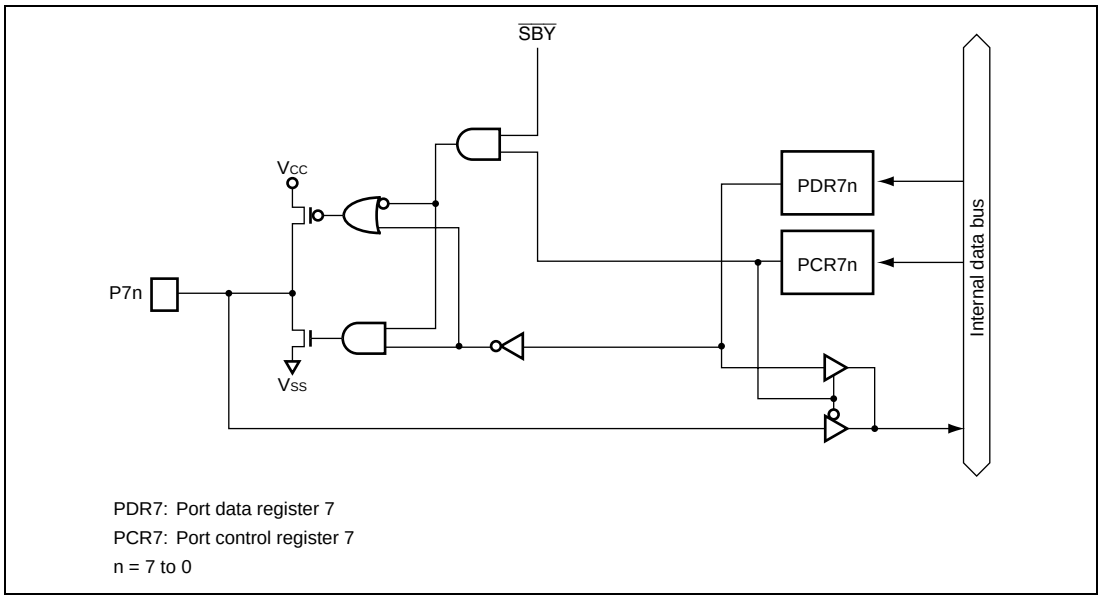
Notes: 1. n: Specified value in R4L. The source and destination operands are accessed n+1 times respectively.

2. It can not be used in this LSI.



PDR6: Port data register 6
PCR6: Port control register 6
PUCR6: Port pull-up control register 6
n = 7 to 0

Figure B.5 Port 6 Block Diagram



PDR7: Port data register 7
PCR7: Port control register 7
n = 7 to 0

Figure B.6 Port 7 Block Diagram