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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	10MHz
Connectivity	I²C, IrDA, SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	52KB (52K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 3x10b, 2x14bSAR
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38086rw10wv

3.1 Exception Sources and Vector Address

Table 3.1 shows the vector addresses and priority of each exception handling. When more than one interrupt is requested, handling is performed from the interrupt with the highest priority.

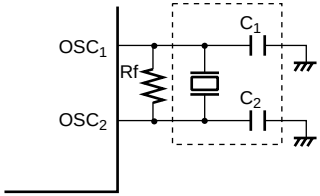
Table 3.1 Exception Sources and Vector Address

Source Origin	Exception Sources	Vector Number	Vector Address	Priority
Reset	$\overline{\text{RES}}$, Watchdog Timer	0	H'0000 to H'0001	High
Reserved for system use	Break instructions	1	H'0002 to H'0003	▲
Reserved for system use	Break interrupts (mode transition)	2	H'0004 to H'0005	
External interrupt	NMI	3	H'0006 to H'0007	
Reserved for system use	Break conditions satisfied	4	H'0008 to H'0009	
Address break	Break conditions satisfied	5	H'000A to H'000B	
External interrupts	IRQ0	6	H'000C to H'000D	
	IRQ1	7	H'000E to H'000F	
	IRQAEC	8	H'0010 to H'0011	
	IRQ3	9	H'0012 to H'0013	
	IRQ4	10	H'0014 to H'0015	
	WKP0	11	H'0016 to H'0017	
	WKP1	12	H'0018 to H'0019	
	WKP2	13	H'001A to H'001B	
	WKP3	14	H'001C to H'001D	
	WKP4	15	H'001E to H'001F	
	WKP5	16	H'0020 to H'0021	
	WKP6	17	H'0022 to H'0023	
	WKP7	18	H'0024 to H'0025	▼
Internal interrupts*	—	19 to 43	H'0026 to H'0057	Low

Note: * For details on the vector table of internal interrupts, refer to section 4.5, Interrupt Exception Handling Vector Table.

5.2.2 Connecting Ceramic Resonator

Figure 5.3 shows a typical method of connecting a ceramic resonator.



Rf = 1 MΩ ±20%

Note: Consult with the crystal resonator manufacturer to determine the circuit constants.

Frequency	Manufacturer	Product Type	C1, C2 Recommendation Value
4.194 MHz	Murata Manufacturing Co., Ltd.	CSTLS4M19G53-B0	15pF (on-chip)
		CSTLS4M19G56-B0	47pF (on-chip)

Figure 5.3 Typical Connection to Ceramic Resonator

5.2.3 External Clock Input Method

Connect an external clock signal to pin OSC1, and leave pin OSC2 open. Figure 5.4 shows a typical connection. The duty cycle of the external clock signal must be 45 to 55%.

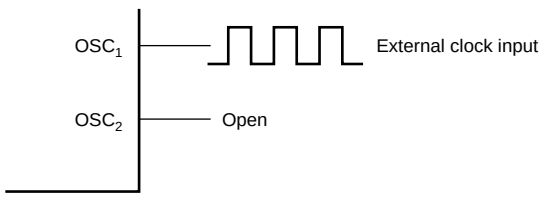


Figure 5.4 Example of External Clock Input

5.2.4 On-Chip Oscillator Selection Method (Supported only by the Masked ROM Version)

The on-chip oscillator is selected by the input level of the IRQAEC pin during a reset. The selection method of the system clock oscillator and the on-chip oscillator is listed in table 5.1. The input level of the IRQAEC pin during a reset* should be fixed either to Vcc or GND, depending on the oscillator type to be selected. The setting takes effect when the rest is cleared. When the on-chip oscillator is selected, to connect a resonator to OSC1 or OSC2 is not necessary. In this case, the OSC1 pin should be fixed to Vcc or GND.

Note: * This reset represents an external reset or power-on reset, but not a reset by the watchdog timer.

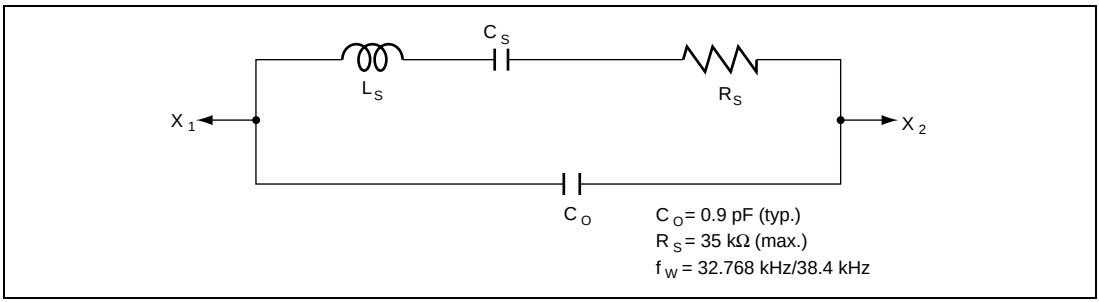


Figure 5.6 Equivalent Circuit of 32.768-kHz/38.4-kHz Crystal Resonator

Notes on Use of Subclock Generator Circuit

The drive capacity of the subclock generator circuit is limited in order to reduce current consumption when operating in the subclock mode. As a result, there may not be sufficient additional margin to accommodate some resonators. Be sure to select a resonator with an equivalent series resistance (R_S) corresponding to that shown in figure 5.6.

5.3.2 Pin Connection when not Using Subclock

When the subclock is not used, connect the X_1 pin to GND and leave the X_2 pin open, as shown in figure 5.7.

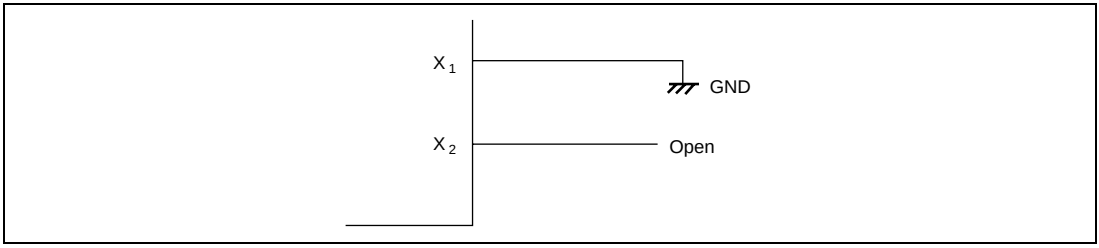


Figure 5.7 Pin Connection when not Using Subclock

6.2 Mode Transitions and States of LSI

Figure 6.1 shows the possible transitions among these operating modes. A transition is made from the program execution state to the program halt state of the program by executing a SLEEP instruction. Interrupts allow for returning from the program halt state to the program execution state of the program. A direct transition between active mode and subactive mode, which are both program execution states, can be made without halting the program. $\overline{\text{RES}}$ input enables transitions from a mode to the reset state. Table 6.2 shows the transition conditions of each mode after the SLEEP instruction is executed and a mode to return by an interrupt. Table 6.3 shows the internal states of the LSI in each mode.

(4) Input Pins to which these Notes Apply

$\overline{\text{IRQ4}}$, $\overline{\text{IRQ3}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ0}}$, $\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$, IRQAEC, TMIF, $\overline{\text{ADTRG}}$, TIOCA1, TIOCB1, TIOCA2 and TIOCB2.

Section 8 RAM

This LSI has an on-chip high-speed static RAM. The RAM is connected to the CPU by a 16-bit data bus, enabling two-state access by the CPU to both byte data and word data.

Product Classification		RAM Size	RAM Address
Flash memory version	H8/38086RF	3 kbytes	H'F380 to H'FF7F
Masked ROM version	H8/38086R	2 kbytes	H'F780 to H'FF7F
	H8/38085R	2 kbytes	H'F780 to H'FF7F
	H8/38084R	1 kbyte	H'FB80 to H'FF7F
	H8/38083R	1 kbyte	H'FB80 to H'FF7F

9.10.3 Pin Functions

The relationship between the register settings and the port functions is shown below.

- PB7/Ain1 pin

  The pin function is switched as shown below according to the AIN1 and AIN2 bits in ADSSR.

AIN1 and AIN2	Other than B'01	B'01
Pin Function	PB7 input pin	Ain1 input pin

- PB6/Ain2 pin

  The pin function is switched as shown below according to the AIN1 and AIN2 bits in ADSSR.

AIN1 and AIN2	Other than B'10	B'10
Pin Function	PB6 input pin	Ain2 input pin

- PB5/Vref/REF pin

  The pin function is switched as shown below according to the VREF1 and VREF2 bits in ADCR.

VREF1 and VREF2	Other than B'00	B'01	B'10, B'11
Pin Function	PB5 input pin	Vref input pin	REF output pin

Note: When these bits are set to B'10 or B'11, the PB5/Vref/REF pin functions as a REF output pin. Thus the power should not be input to the pin. If the power is input, it is short-circuited internally with the REF output and will cause a failure.

- PB2/AN2/$\overline{\text{IRQ3}}$ pin

  The pin function is switched as shown below according to the combination of the CH3 to CH0 bits in AMR and IRQ3 bit in PMRB.

IRQ3	0		1
CH3 to CH0	Other than B'0110	B'0110	x
Pin Function	PB2 input pin	AN2 input pin	$\overline{\text{IRQ3}}$ input pin

[Legend] x: Don't care.

Bit	Bit Name	Initial Value	R/W	Description
1	CKS1	0	R/W	Clock Select 0 and 1
0	CKS0	0	R/W	These bits select the clock source for the on-chip baud rate generator. 00: ϕ clock (n = 0) 01: ϕw/2 or ϕ w clock (n = 1) 10: ϕ/16 clock (n = 2) 11: ϕ/64 clock (n = 3) When the setting value is 01 in active (medium-speed/high-speed) mode and sleep (medium-speed/high-speed) mode ϕw/2 clock is set. In subacive mode and subsleep mode, ϕw clock is set. The SCI3 is enabled only, when ϕw/2 is selected for the CPU operating clock. For the relationship between the bit rate register setting and the baud rate, see section 15.3.8, Bit Rate Register (BRR). n is the decimal representation of the value of n in BRR (see section 15.3.8, Bit Rate Register (BRR)).

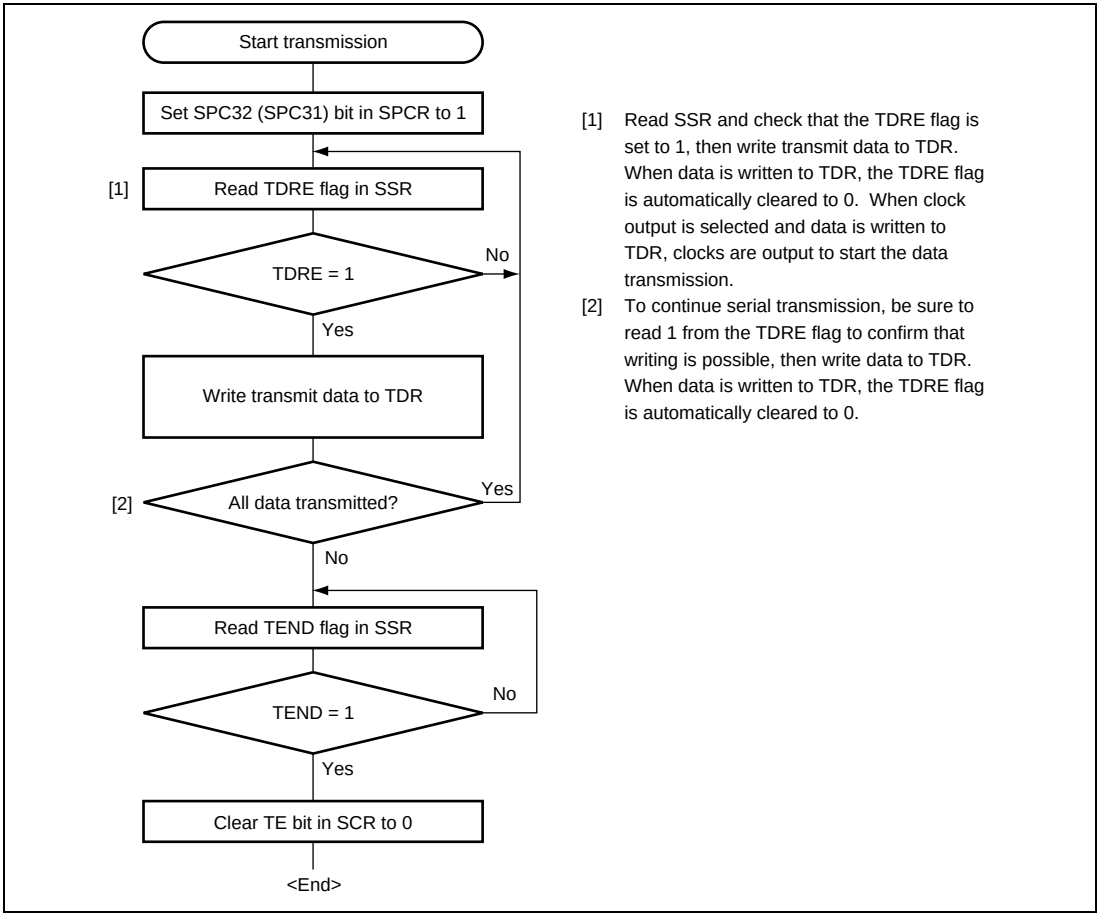


Figure 15.11 Sample Serial Transmission Flowchart (Clocked Synchronous Mode)

During transmission, the SCI4 operates as shown below.

1. The SCI4 sets the TE bit to 1 and clears the TDRE flag to 0 when transmit data is written to in TDR4 to transmit data from TDR4 to SR4. After that, the SCI4 sets the TDRE flag to 1 to start transmission. At this time, when the TIE bit in SCR4 is set to 1, a TXI is generated.
2. In clock output mode, the SCI4 outputs eight pulses of the synchronous clock. When the external clock is selected, the SCI4 outputs data in synchronization with the input clock.
3. Serial data is output from the LSB (bit 0) to MSB (bit 7) on pin SO4. The SCI4 checks the TDRE flag at the timing of outputting the MSB (bit 7).
4. When TDRE = 0, data in TDR4 is transmitted to SR4 and then the data of the next frame starts to be transmitted. When TDRE = 1, the SCI4 sets the TEND bit to 1 and holds the output level after transmitting the MSB (bit 7). At this time, when the TEIE bit in SCR4 is set to 1, a TEI is generated.
5. After the transmission, the output level on pin SCK4 is fixed high.

Note: Transmission cannot be performed when the error flag (ORER) which indicates the data reception status is set to 1. Before transmission, confirm that the ORER flag is cleared to 0.

Figure 16.5 shows the example of transmission operation.

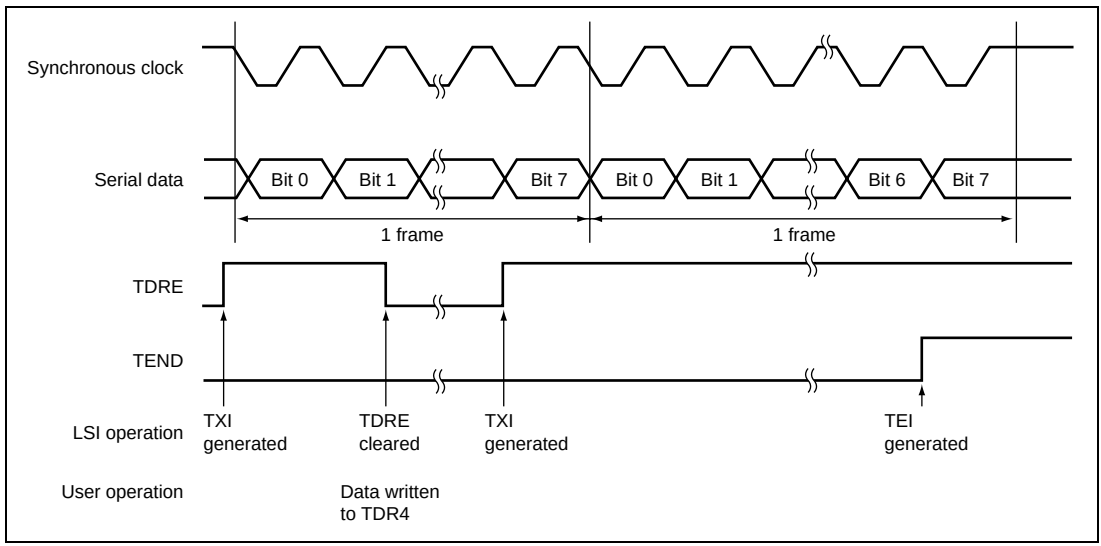


Figure 16.5 Transmit Operation Example

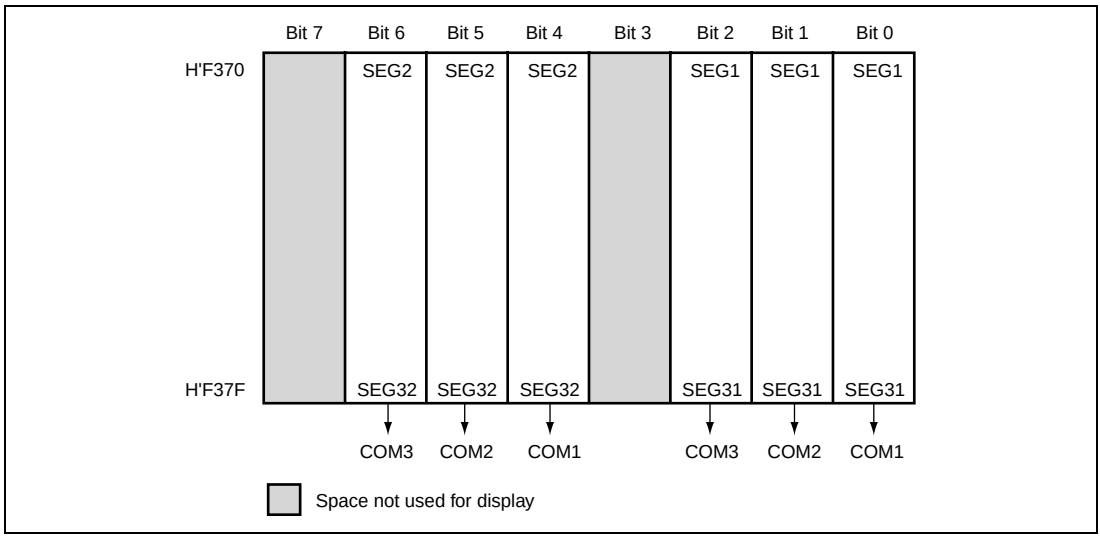


Figure 20.4 LCD RAM Map (1/3 Duty)

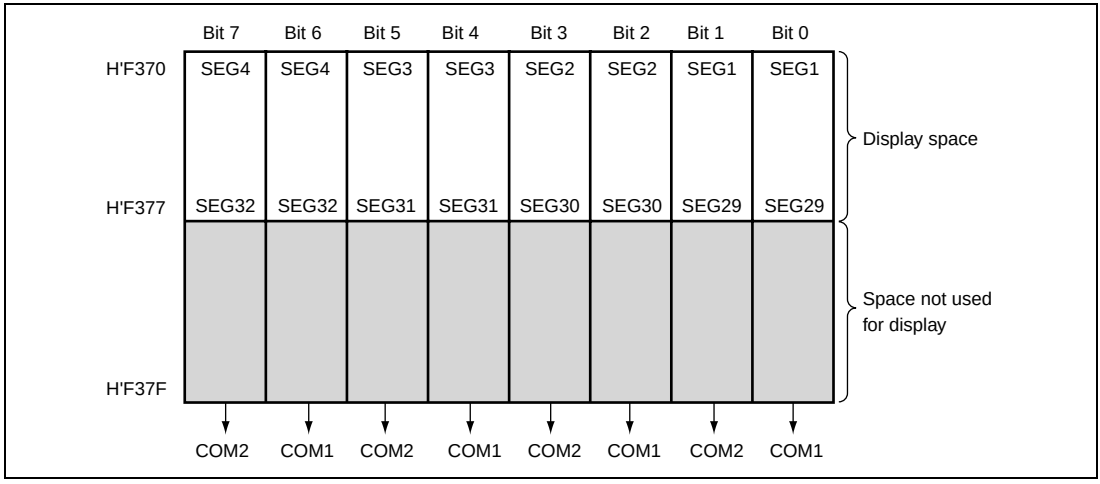


Figure 20.5 LCD RAM Map (1/2 Duty)

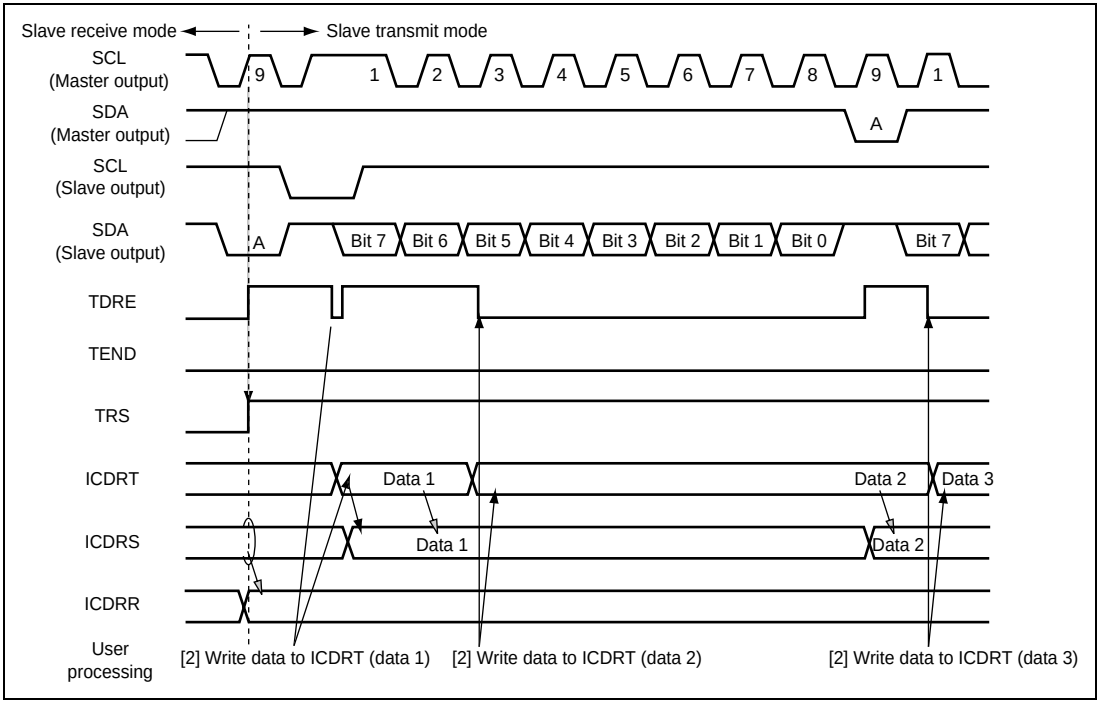


Figure 21.9 Slave Transmit Mode Operation Timing (1)

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
PMR3	—	—	—	—	—	—	—	TMOW	I/O ports
PMR4	—	—	—	—	—	TMOFH	TMOFL	TMIF	
PMR5	WKP7	WKP6	WKP5	WKP4	WKP3	WKP2	WKP1	WKP0	
PMR9	—	—	—	—	—	IRQ4	PWM2	PWM1	
PMRB	—	—	—	ADTSTCHG	—	IRQ3	IRQ1	IRQ0	
PWCR22	—	—	—	—	—	PWCR22	PWCR21	PWCR20	14-bit PWM
PWDR2	—	—	PWDR213	PWDR212	PWDR211	PWDR210	PWDR29	PWDR28	
	PWDR27	PWDR26	PWDR25	PWDR24	PWDR23	PWDR22	PWDR21	PWDR20	
PWCR1	—	—	—	—	—	PWCR12	PWCR11	PWCR10	
PWDR1	—	—	PWDR113	PWDR112	PWDR111	PWDR110	PWDR19	PWDR18	
	PWDR17	PWDR16	PWDR15	PWDR14	PWDR13	PWDR12	PWDR11	PWDR10	
PDR1	—	P16	P15	P14	P13	P12	P11	P10	I/O ports
PDR3	P37	P36	—	—	—	P32	P31	P30	
PDR4	—	—	—	—	—	P42	P41	P40	
PDR5	P57	P56	P55	P54	P53	P52	P51	P50	
PDR6	P67	P66	P65	P64	P63	P62	P61	P60	
PDR7	P77	P76	P75	P74	P73	P72	P71	P70	
PDR8	P87	P86	P85	P84	P83	P82	P81	P80	
PDR9	—	—	—	—	P93	P92	P91	P90	
PDRA	—	—	—	—	PA3	PA2	PA1	PA0	
PDRB	PB7	PB6	PB5	—	—	PB2	PB1	PB0	
PUCR1	—	PUCR16	PUCR15	PUCR14	PUCR13	PUCR12	PUCR11	PUCR10	
PUCR3	PUCR37	PUCR36	—	—	—	—	—	PUCR30	
PUCR5	PUCR57	PUCR56	PUCR55	PUCR54	PUCR53	PUCR52	PUCR51	PUCR50	
PUCR6	PUCR67	PUCR66	PUCR65	PUCR64	PUCR63	PUCR62	PUCR61	PUCR60	
PCR1	—	PCR16	PCR15	PCR14	PCR13	PCR12	PCR11	PCR10	
PCR3	PCR37	PCR36	—	—	—	PCR32	PCR31	PCR30	
PCR4	—	—	—	—	—	PCR42	PCR41	PCR40	
PCR5	PCR57	PCR56	PCR55	PCR54	PCR53	PCR52	PCR51	PCR50	
PCR6	PCR67	PCR66	PCR65	PCR64	PCR63	PCR62	PCR61	PCR60	
PCR7	PCR77	PCR76	PCR75	PCR74	PCR73	PCR72	PCR71	PCR70	

25.2.6 LCD Characteristics

Table 25.8 shows the LCD characteristics.

Table 25.8 LCD Characteristics

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, DV_{CC} = 2.2 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise specified.

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Values Typ.	Values Max.	Unit	Notes
Segment driver drop voltage	V_{DS}	SEG1 to SEG32	I_D = 2 µA V1 = 2.7 V to 3.6 V	—	—	0.6	V	*1
Common driver drop voltage	V_{DC}	COM1 to COM4	I_D = 2 µA V1 = 2.7 V to 3.6 V	—	—	0.3	V	*1
LCD power supply split-resistance	R_{LCD}		Between V1 and V_{SS}	1.5	3.0	7.0	MΩ	
LCD display voltage	V_{LCD}	V1		2.2	—	3.6	V	*2
V3 power supply voltage	V_{LCD3}	V3	Between V3 and V_{SS}	0.9	1.0	1.1	V	*3*4
V2 power supply voltage	V_{LCD2}	V2	Between V2 and V_{SS}	—	2.0 ($V_{LCD3} \times 2$)	—	V	*3*4
V1 power supply voltage	V_{LCD1}	V1	Between V1 and V_{SS}	—	3.0 ($V_{LCD3} \times 3$)	—	V	*3*4
3-V constant voltage LCD power supply circuit current consumption	I_{LCD}	Vcc	Vcc = 3.0 V Booster clock: 125 kHz	—	20	—	µA	Reference value*4*5

Notes: 1. The voltage drop from power supply pins V1, V2, V3, and V_{SS} to each segment pin or common pin.
2. When the LCD display voltage is supplied from an external power source, ensure that the following relationship is maintained: $V1 \geq V2 \geq V3 \geq V_{SS}$.
3. The value when the LCD power supply split-resistor is separated and 3-V constant voltage power supply circuit is driven.
4. For details on the register (BGRMR) setting range when the voltage of the V3 pin is set to 1.0 V, refer to section 20.3.5, BGR Control Register (BGRMR).
5. Includes the current consumption of the band-gap reference circuit (BGR) (operation).

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Input low voltage	V_{IL}	$\overline{RES}$, $\overline{NMI}$, $\overline{WKP0}$ to $\overline{WKP7}$, $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ3}$, $\overline{IRQ4}$, IRQAEC, AEVL, AEVH, TMIF, $\overline{ADTRG}$, SCK32, SCK31, SCK4		–0.3	—	$0.1V_{CC}$	V	
		RXD32, RXD31		–0.3	—	$0.2V_{CC}$		
		OSC1		–0.3	—	$0.1V_{CC}$		
		X1	V_{CC} = 2.7 to 3.6 V	–0.3	—	$0.1V_{CC}$		
		P10 to P16, P30 to P32, P36, P37, P40 to P42, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P93, PA0 to PA3, TCLKA, TCLKB, TCLKC, TIOCA1, TIOCB1, TIOCA2, TIOCB2, SCL, SDA, PB0 to PB2, PB5 to PB7		–0.3	—	$0.2V_{CC}$		
Output high voltage	V_{OH}	P10 to P16, P30 to P32, P36, P37, P40 to P42, P50 to P57, P60 to P67, P70 to P77, P80 to P87, PA0 to PA3	$-I_{OH}$ = 1.0 mA V_{CC} = 2.7 to 3.6 V	V_{CC} – 1.0	—	—	V	
			$-I_{OH}$ = 0.1 mA	V_{CC} – 0.3	—	—		
		P90 to P93	$-I_{OH}$ = 1.0 mA V_{CC} = 2.7 to 3.6 V	V_{CC} – 1.0	—	—		
			$-I_{OH}$ = 0.1 mA	V_{CC} – 0.3	—	—		

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Conversion time			AV_{CC} = 2.7 V to 3.6 V V_{CC} = 2.7 V to 3.6 V	6.2	—	124	µs	
			AV_{CC} = 2.2 V to 3.6 V V_{CC} = 2.2 V to 3.6 V	14.7	—	124		
			Other than above	31	—	124		

Notes: 1. Set $AV_{CC} = V_{CC}$ when the A/D converter is not used.
2. AI_{STOP1} is the current in active and sleep modes while the A/D converter is idle.
3. AI_{STOP2} is the current at a reset and in standby, watch, subactive, and subsleep modes while the A/D converter is idle.
4. Conversion time = 31 µs

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Analog data input voltage	Ain	Ain1, Ain2	PGA = 1/3	0.6	—	2.7 V_{ref} (2.7 V_{ref} < DV_{cc}) 2.7 REF (2.7 REF < DV_{cc})	V	
			PGA = 1, bypass	0.2	—	V_{ref} REF	V	
			PGA = 2	0.1	—	0.5 V_{ref} 0.5 REF	V	
			PGA = 4	0.05	—	0.25 V_{ref} 0.25 REF	V	
Operating temperature	Ta			0	—	50	°C	

Notes:
1. Set DV_{cc} = V_{cc} when the ΔΣ A/D converter is not used.
2. DI_{STOP1} is the current in active and sleep modes while the ΔΣ A/D converter is idle.
3. DI_{STOP2} is the current at a reset and in standby, watch, subactive, and subsleep modes while the ΔΣ A/D converter is idle.
4. BGR stabilization time = 150 μs (Ta = 25°C, V_{cc} = 3.0 V)
   The BGR stabilization time is started after setting bit 7 (BTRSTPN) in BGR control register (BGRMR) to 1. The stabilization time may vary due to factors such as the capacitance connected to the REF pin, so careful evaluation is necessary.
5. Before using the system, the internal reference value must be tested because there is dispersion in sample data.
6. This is the value when the BGR is not used.
7. The error for each item varies depending on factors such as temperature, voltage, conversion time, and sample variation. It is therefore necessary to perform careful evaluation under actual usage conditions.

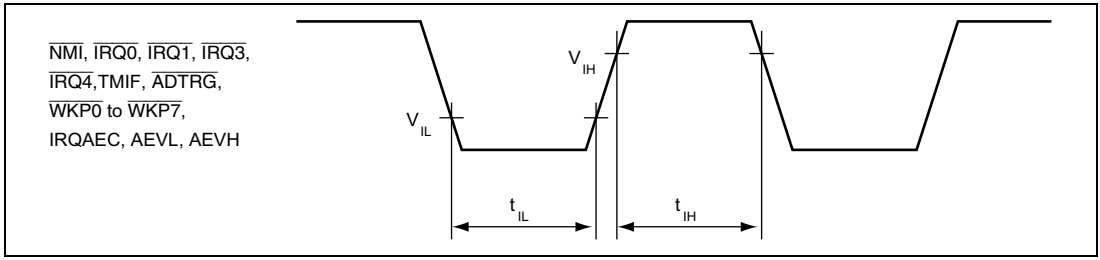


Figure 25.4 Input Timing

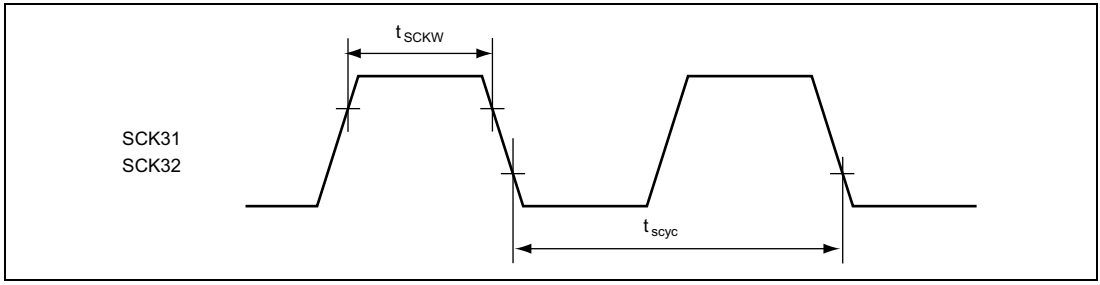


Figure 25.5 SCK3 Input Clock Timing

Mnemonic		Operand Size	Addressing Mode and Instruction Length (bytes)									Operation	Condition Code						No. of States*1	
			#xx	Rn	@ERn	@(d, ERn)	@–ERn/@ERn+	@aa	@(d, PC)	@@aa	—		I	H	N	Z	V	C	Normal	Advanced
NEG	NEG.B Rd	B		2								0–Rd8 → Rd8	—	↕	↕	↕	↕	↕	2	
	NEG.W Rd	W		2								0–Rd16 → Rd16	—	↕	↕	↕	↕	↕	2	
	NEG.L ERd	L		2								0–ERd32 → ERd32	—	↕	↕	↕	↕	↕	2	
EXTU	EXTU.W Rd	W		2								0 → (<bits 15 to 8> of Rd16)	—	—	0	↕	0	—	2	
	EXTU.L ERd	L		2								0 → (<bits 31 to 16> of ERd32)	—	—	0	↕	0	—	2	
EXTS	EXTS.W Rd	W		2								(<bit 7> of Rd16) → (<bits 15 to 8> of Rd16)	—	—	↕	↕	0	—	2	
	EXTS.L ERd	L		2								(<bit 15> of ERd32) → (<bits 31 to 16> of ERd32)	—	—	↕	↕	0	—	2	

L

M

N

O

P

R