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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, Ethernet, IrDA, MMC/SD, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4e8ca-an

5. Power Considerations

5.1 Power Supplies

The SAM4E has several types of power supply pins:

- VDDCORE pins: power the core, the first flash rail, the embedded memories and the peripherals.
  Voltage ranges from 1.08V to 1.32V.
- VDDIO pins: power the peripheral I/O lines (Input/Output Buffers), the second flash rail, the backup part, the USB transceiver, 32 kHz crystal oscillator and oscillator pads.
  Voltage ranges from 1.62V to 3.6V.
- VDDIN pins: voltage regulator input, DAC and Analog Comparator power supply.
  Voltage ranges from 1.62V to 3.6V.
- VDDPLL pin: powers the PLL, the Fast RC and the 3 to 20 MHz oscillator.
  Voltage ranges from 1.08V to 1.32V.

5.2 Voltage Regulator

The SAM4E embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is designed to supply the internal core of SAM4E It features two operating modes:

- In normal mode, the voltage regulator consumes less than 500 µA static current and draws 80 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In wait mode quiescent current is only 5 µA.
- In backup mode, the voltage regulator consumes less than 1.5 µA while its output (VDDOUT) is driven internally to GND. The default output voltage is 1.20V and the start-up time to reach normal mode is less than 300 µs.

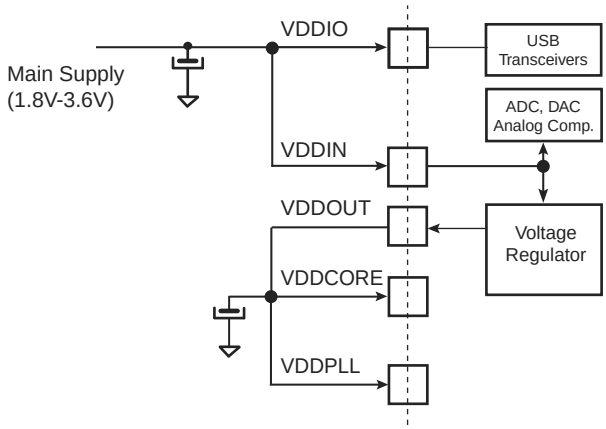
For adequate input and output power supply decoupling/bypassing, refer to the “Voltage Regulator” section in the “Electrical Characteristics” section of the datasheet.

5.3 Typical Powering Schematics

The SAM4E supports a 1.62V-3.6V single supply mode. The internal regulator input is connected to the source and its output feeds VDDCORE. Figure 5-1 below shows the power schematics.

As VDDIN powers the voltage regulator, the DAC and the analog comparator, when the user does not want to use the embedded voltage regulator, it can be disabled by software via the SUPC (note that this is different from backup mode).

Figure 5-1. Single Supply



Note: Restrictions:
- For USB, VDDIO needs to be greater than 3.0V
- For AFE, VDDIN needs to be greater than 2.0V
- For DAC, VDDIN needs to be greater than 2.4V

11.2.3 PIO Controller C Multiplexing

Table 11-4. Multiplexing on PIO Controller C (PIOC)

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PC0	D0	PWML0		AFE0_AD14		144-pin version(1)
PC1	D1	PWML1		AFE1_AD4		144-pin version(1)
PC2	D2	PWML2		AFE1_AD5		144-pin version(1)
PC3	D3	PWML3		AFE1_AD6		144-pin version(1)
PC4	D4	NPCS1		AFE1_AD7		144-pin version(1)
PC5	D5	TIOA6				144-pin version(1)
PC6	D6	TIOB6				144-pin version(1)
PC7	D7	TCLK6				144-pin version(1)
PC8	NWE	TIOA7				144-pin version(1)
PC9	NANDOE	TIOB7				144-pin version(1)
PC10	NANDWE	TCLK7				144-pin version(1)
PC11	NRD	TIOA8				144-pin version(1)
PC12	NCS3	TIOB8	CANRX1	AFE0_AD8		144-pin version(1)
PC13	NWAIT	PWML0		AFE0_AD6		144-pin version(1)
PC14	NCS0	TCLK8				144-pin version(1)
PC15	NCS1	PWML1	CANTX1	AFE0_AD7		144-pin version(1)
PC16	A21/ NANDALE					144-pin version(1)
PC17	A22/ NANDCLE					144-pin version(1)
PC18	A0	PWMH0				144-pin version(1)
PC19	A1	PWMH1				144-pin version(1)
PC20	A2	PWMH2				144-pin version(1)
PC21	A3	PWMH3				144-pin version(1)
PC22	A4	PWML3				144-pin version(1)
PC23	A5	TIOA3				144-pin version(1)
PC24	A6	TIOB3				144-pin version(1)
PC25	A7	TCLK3				144-pin version(1)
PC26	A8	TIOA4		AFE0_AD12		144-pin version(1)
PC27	A9	TIOB4		AFE0_AD13		144-pin version(1)
PC28	A10	TCLK4				144-pin version(1)
PC29	A11	TIOA5		AFE0_AD9		144-pin version(1)
PC30	A12	TIOB5		AFE0_AD10		144-pin version(1)
PC31	A13	TCLK5		AFE0_AD11		144-pin version(1)

Note: 1. Used by peripheral: defined as Bidirectional IO.

25. SAM-BA Boot Program for SAM4E Microcontrollers

25.1 Description

The SAM-BA® Boot Program integrates an array of programs permitting download and/or upload into the different memories of the product.

25.2 Embedded Characteristics

- Default Boot Program Stored in SAM4E Series Products
- Interface with SAM-BA® Graphic User Interface
- SAM-BA Boot
  - Supports Several Communication Media
    - Serial Communication on UART0
    - USB Device Port Communication up to 1M Byte/s
  - USB Requirements
    - External Crystal or Clock with the frequency of:

- 11,289 MHz

- 12,000 MHz

- 16,000 MHz

- 18,432 MHz

25.3 Hardware and Software Constraints

- SAM-BA Boot uses the first 2048 bytes of the SRAM for variables and stacks. The remaining available size can be used for user's code.
- USB Requirements:
  - External Crystal or External Clock(1) with frequency of:
    - 11,289 MHz
    - 12,000 MHz
    - 16,000 MHz
    - 18,432 MHz
- UART0 requirements: None

Note: 1. must be 2500 ppm and 1.8V Square Wave Signal.

Table 25-1. Pins Driven during Boot Program Execution

Peripheral	Pin	PIO Line
UART0	URXD0	PA9
UART0	UTXD0	PA10

27.7.2 DMAC Enable Register

Name: DMAC_EN

Address: 0x400C0004

Access: Read-write

Reset: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	ENABLE

This register can only be written if the WPEN bit is cleared in “DMAC Write Protect Mode Register” .

- **ENABLE: General Enable of DMA**

0: DMA Controller is disabled.

1: DMA Controller is enabled.

The glitch filters are controlled by the register set: PIO_IFER (Input Filter Enable Register), PIO_IFDR (Input Filter Disable Register) and PIO_IFSR (Input Filter Status Register). Writing PIO_IFER and PIO_IFDR respectively sets and clears bits in PIO_IFSR. This last register enables the glitch filter on the I/O lines.

When the glitch and/or debouncing filter is enabled, it does not modify the behavior of the inputs on the peripherals. It acts only on the value read in PIO_PDSR and on the input change interrupt detection. The glitch and debouncing filters require that the PIO Controller clock is enabled.

Figure 33-5. Input Glitch Filter Timing

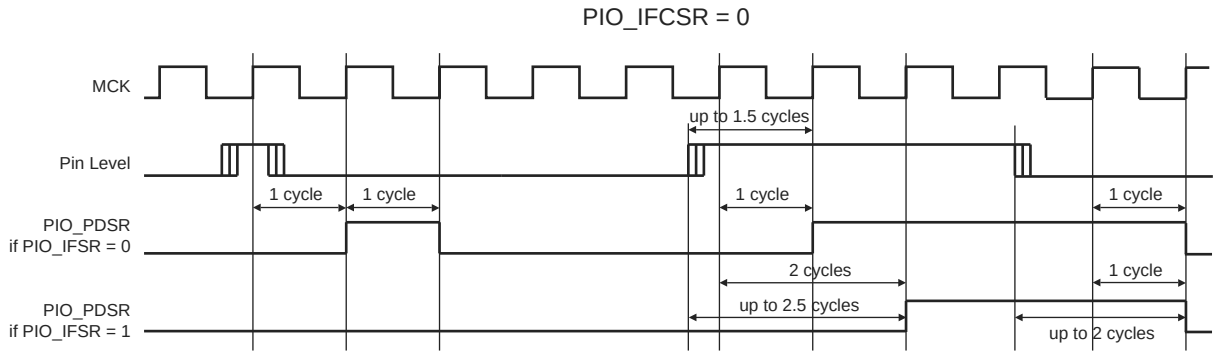
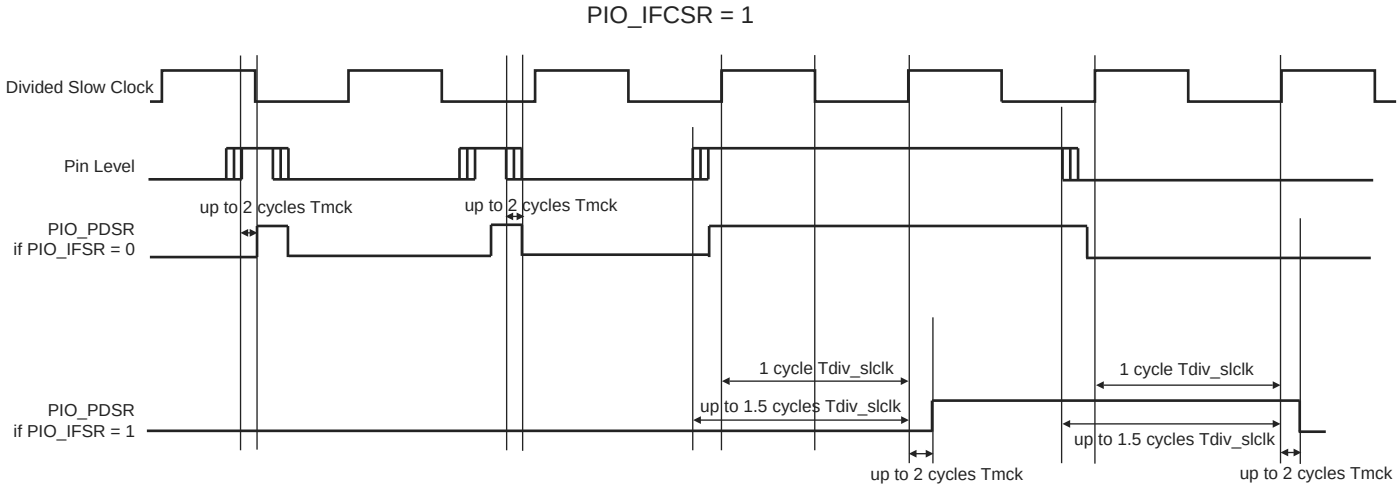


Figure 33-6. Input Debouncing Filter Timing



33.5.10 Input Edge/Level Interrupt

The PIO Controller can be programmed to generate an interrupt when it detects an edge or a level on an I/O line. The Input Edge/Level Interrupt is controlled by writing PIO_IER (Interrupt Enable Register) and PIO_IDR (Interrupt Disable Register), which respectively enable and disable the input change interrupt by setting and clearing the corresponding bit in PIO_IMR (Interrupt Mask Register). As Input change detection is possible only by comparing two successive samplings of the input of the I/O line, the PIO Controller clock must be enabled. The Input Change Interrupt is available, regardless of the configuration of the I/O line, i.e. configured as an input only, controlled by the PIO Controller or assigned to a peripheral function.

By default, the interrupt can be generated at any time an edge is detected on the input.

Some additional Interrupt modes can be enabled/disabled by writing in the PIO_AIMER (Additional Interrupt Modes Enable Register) and PIO_AIMDR (Additional Interrupt Modes Disable Register). The current state of this selection can be read through the PIO_AIMMR (Additional Interrupt Modes Mask Register)

Table 33-3. Register Mapping (Continued)

Offset	Register	Name	Access	Reset
0x0120 to 0x014C	Reserved	–	–	–
0x150	Parallel Capture Mode Register	PIO_PCMR	Read-write	0x00000000
0x154	Parallel Capture Interrupt Enable Register	PIO_PCIER	Write-only	–
0x158	Parallel Capture Interrupt Disable Register	PIO_PCIDR	Write-only	–
0x15C	Parallel Capture Interrupt Mask Register	PIO_PCIMR	Read-only	0x00000000
0x160	Parallel Capture Interrupt Status Register	PIO_PCISR	Read-only	0x00000000
0x164	Parallel Capture Reception Holding Register	PIO_PCRHR	Read-only	0x00000000
0x0168 to 0x018C	Reserved for PDC Registers	–	–	–

Notes: 1. Reset value depends on the product implementation.

2. PIO_ODSR is Read-only or Read/Write depending on PIO_OWSR I/O lines.

3. Reset value of PIO_PDSR depends on the level of the I/O lines. Reading the I/O line levels requires the clock of the PIO Controller to be enabled, otherwise PIO_PDSR reads the levels present on the I/O line at the time the clock was disabled.

4. PIO_ISR is reset at 0x0. However, the first read of the register may read a different value as input changes may have occurred.

Note: If an offset is not listed in the table, it must be considered as reserved.

34.8.6 SPI Interrupt Enable Register

Name: SPI_IER

Address: 0x40088014

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	UNDES	TXEMPTY	NSSR
7	6	5	4	3	2	1	0
TXBUFE	RXBUFF	ENDTX	ENDRX	OVRES	MODF	TDRE	RDRF

0 = No effect.

1 = Enables the corresponding interrupt.

- **RDRF: Receive Data Register Full Interrupt Enable**
- **TDRE: SPI Transmit Data Register Empty Interrupt Enable**
- **MODF: Mode Fault Error Interrupt Enable**
- **OVRES: Overrun Error Interrupt Enable**
- **ENDRX: End of Receive Buffer Interrupt Enable**
- **ENDTX: End of Transmit Buffer Interrupt Enable**
- **RXBUFF: Receive Buffer Full Interrupt Enable**
- **TXBUFE: Transmit Buffer Empty Interrupt Enable**
- **NSSR: NSS Rising Interrupt Enable**
- **TXEMPTY: Transmission Registers Empty Enable**
- **UNDES: Underrun Error Interrupt Enable**

35.12.8 TWI Interrupt Disable Register

Name: TWI_IDR

Address: 0x400A8028 (0), 0x400AC028 (1)

Access: Write-only

Reset: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
TXBUFE	RXBUFF	ENDTX	ENDRX	EOSACC	SCL_WS	ARBLST	NACK
7	6	5	4	3	2	1	0
–	OVRE	GACC	SVACC	–	TXRDY	RXRDY	TXCOMP

- **TXCOMP: Transmission Completed Interrupt Disable**
- **RXRDY: Receive Holding Register Ready Interrupt Disable**
- **TXRDY: Transmit Holding Register Ready Interrupt Disable**
- **SVACC: Slave Access Interrupt Disable**
- **GACC: General Call Access Interrupt Disable**
- **OVRE: Overrun Error Interrupt Disable**
- **NACK: Not Acknowledge Interrupt Disable**
- **ARBLST: Arbitration Lost Interrupt Disable**
- **SCL_WS: Clock Wait State Interrupt Disable**
- **EOSACC: End Of Slave Access Interrupt Disable**
- **ENDRX: End of Receive Buffer Interrupt Disable**
- **ENDTX: End of Transmit Buffer Interrupt Disable**
- **RXBUFF: Receive Buffer Full Interrupt Disable**
- **TXBUFE: Transmit Buffer Empty Interrupt Disable**

0 = No effect.

1 = Disables the corresponding interrupt.

37.7.1 Baud Rate Generator

The Baud Rate Generator provides the bit period clock named the Baud Rate Clock to both the receiver and the transmitter.

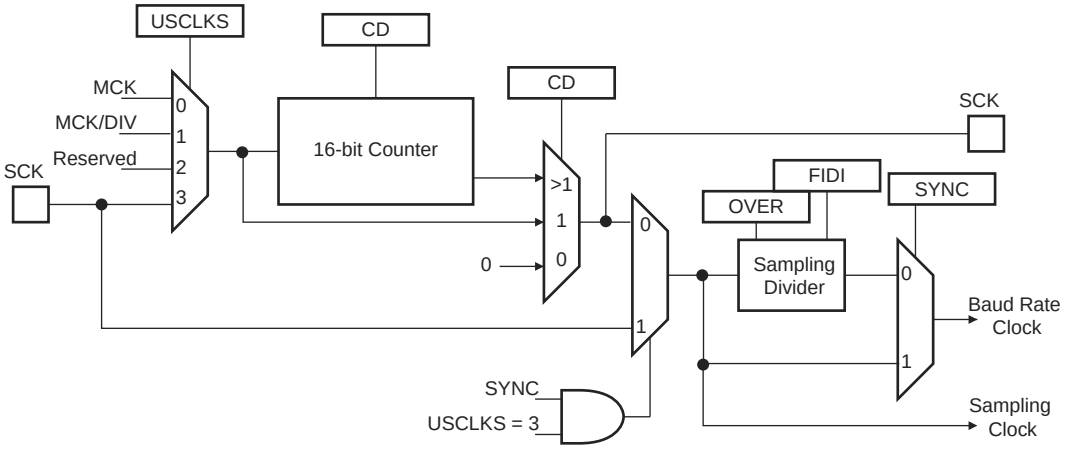
The Baud Rate Generator clock source can be selected by setting the USCLKS field in the Mode Register (US_MR) between:

- The Master Clock MCK
- A division of the Master Clock, the divider being product dependent, but generally set to 8
- The external clock, available on the SCK pin

The Baud Rate Generator is based upon a 16-bit divider, which is programmed with the CD field of the Baud Rate Generator Register (US_BRGR). If CD is programmed to 0, the Baud Rate Generator does not generate any clock. If CD is programmed to 1, the divider is bypassed and becomes inactive.

If the external SCK clock is selected, the duration of the low and high levels of the signal provided on the SCK pin must be longer than a Master Clock (MCK) period. The frequency of the signal provided on SCK must be at least 3 times lower than MCK in USART mode, or 6 times lower in SPI mode.

Figure 37-3. Baud Rate Generator



37.7.1.1 Baud Rate in Asynchronous Mode

If the USART is programmed to operate in asynchronous mode, the selected clock is first divided by CD, which is field programmed in the Baud Rate Generator Register (US_BRGR). The resulting clock is provided to the receiver as a sampling clock and then divided by 16 or 8, depending on the programming of the OVER bit in US_MR.

If OVER is set to 1, the receiver sampling is 8 times higher than the baud rate clock. If OVER is cleared, the sampling is performed at 16 times the baud rate clock.

The following formula performs the calculation of the Baud Rate.

$$Baudrate = \frac{SelectedClock}{(8(2-Over)CD)}$$

This gives a maximum baud rate of MCK divided by 8, assuming that MCK is the highest possible clock and that OVER is programmed to 1.

Baud Rate Calculation Example

38.6.12.3 WAVSEL = 01

When WAVSEL = 01, the value of TC_CV is incremented from 0 to 0xFFFF. Once 0xFFFF is reached, the value of TC_CV is decremented to 0, then re-incremented to 0xFFFF and so on. See Figure 38-12.

A trigger such as an external event or a software trigger can modify TC_CV at any time. If a trigger occurs while TC_CV is incrementing, TC_CV then decrements. If a trigger is received while TC_CV is decrementing, TC_CV then increments. See Figure 38-13.

RC Compare cannot be programmed to generate a trigger in this configuration.

At the same time, RC Compare can stop the counter clock (CPCSTOP = 1) and/or disable the counter clock (CPCDIS = 1).

Figure 38-12. WAVSEL = 01 Without Trigger

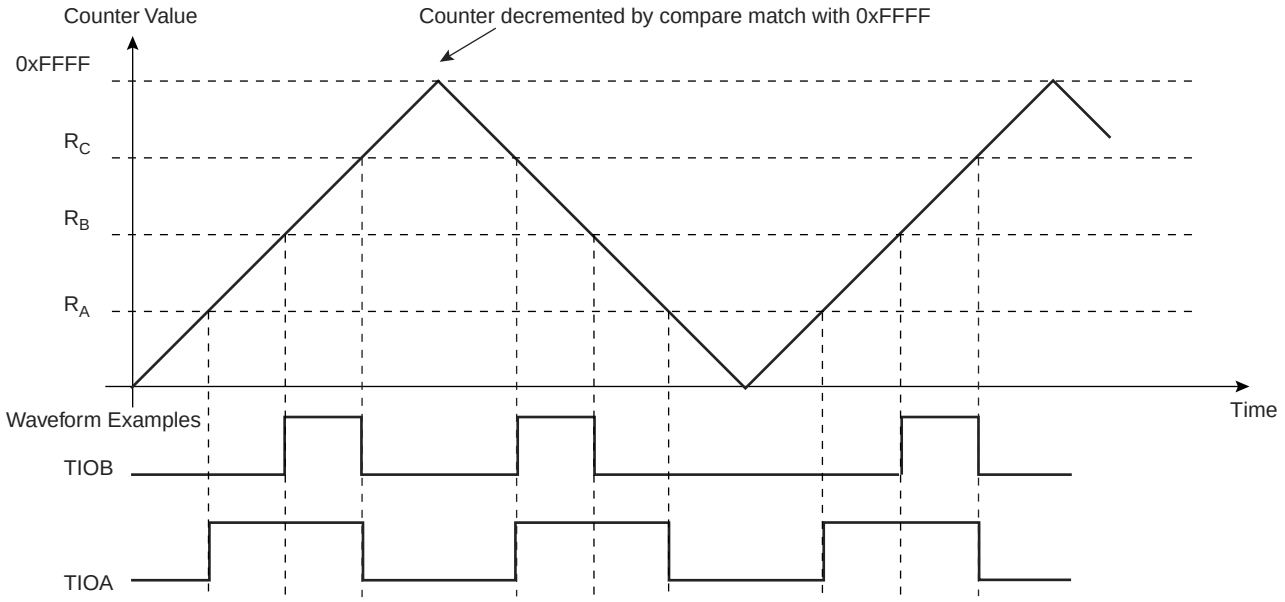


Figure 38-13. WAVSEL = 01 With Trigger

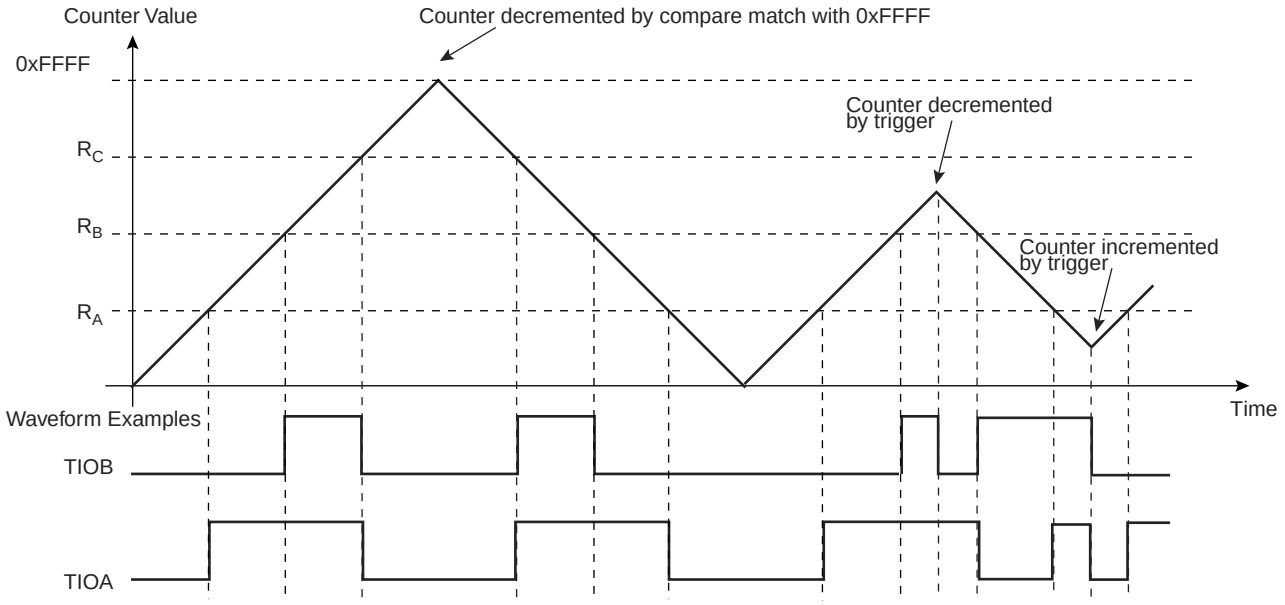
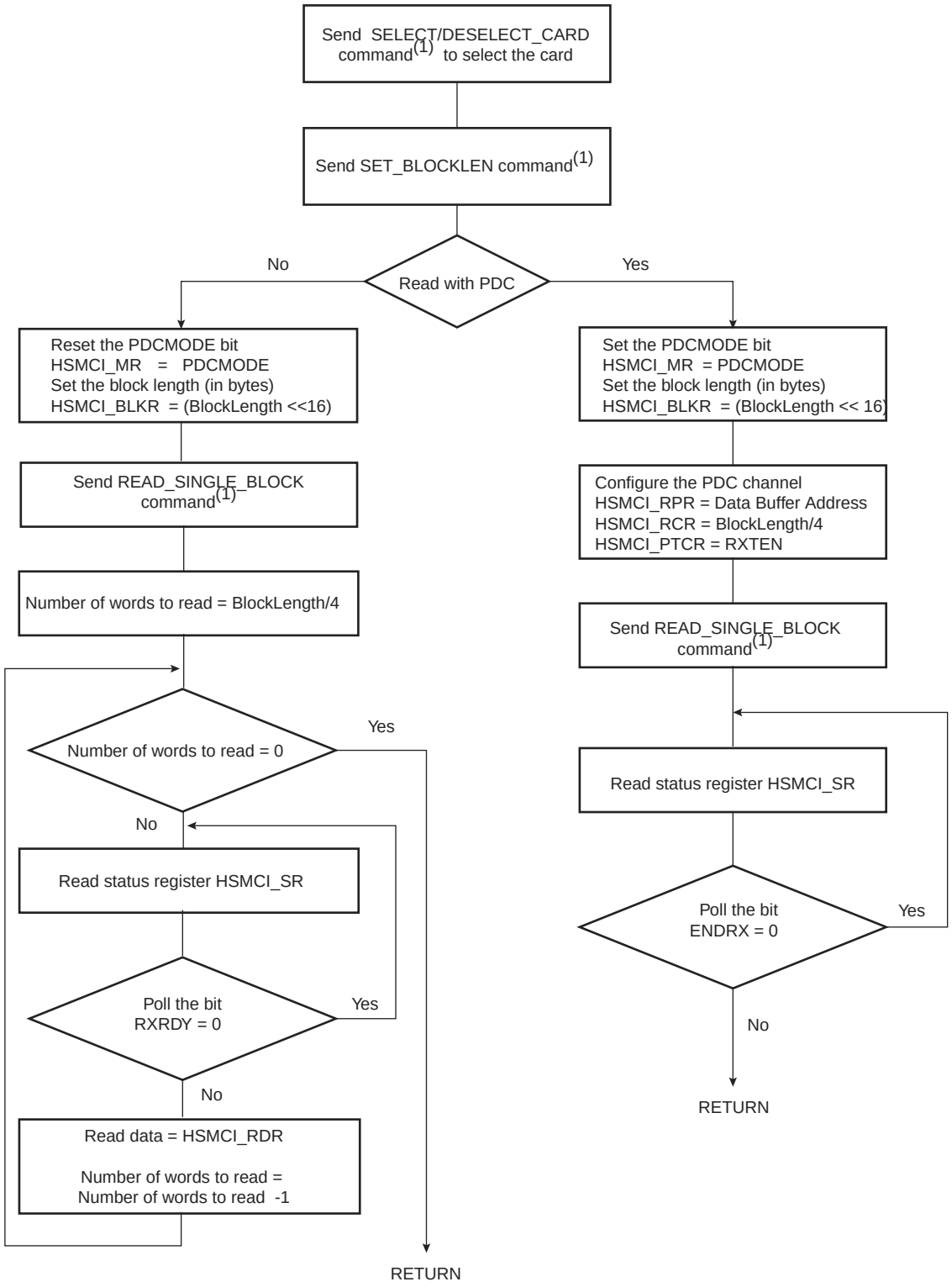


Figure 39-8. Read Functional Flow Diagram



Note: 1. It is assumed that this command has been correctly sent (see Figure 39-7).

For the Single Block Reads, the NOTBUSY flag is set at the end of the data read block.
For the Multiple Block Reads with pre-defined block count, the NOTBUSY flag is set at the end of the last received data block.

The NOTBUSY flag allows to deal with these different states.

0 = The HSMCI is not ready for new data transfer. Cleared at the end of the card response.

1 = The HSMCI is ready for new data transfer. Set when the busy state on the data line has ended. This corresponds to a free internal data receive buffer of the card.

- **ENDRX: End of RX Buffer**

0 = The Receive Counter Register has not reached 0 since the last write in HSMCI_RCR or HSMCI_RNCR.

1 = The Receive Counter Register has reached 0 since the last write in HSMCI_RCR or HSMCI_RNCR.

- **ENDTX: End of TX Buffer**

0 = The Transmit Counter Register has not reached 0 since the last write in HSMCI_TCR or HSMCI_TNCR.

1 = The Transmit Counter Register has reached 0 since the last write in HSMCI_TCR or HSMCI_TNCR.

Note: BLKE and NOTBUSY flags can be used to check that the data has been successfully transmitted on the data lines and not only transferred from the PDC to the HSMCI Controller.

- **SDIOIRQA: SDIO Interrupt for Slot A**

0 = No interrupt detected on SDIO Slot A.

1 = An SDIO Interrupt on Slot A occurred. Cleared when reading the HSMCI_SR.

- **SDIOWAIT: SDIO Read Wait Operation Status**

0 = Normal Bus operation.

1 = The data bus has entered IO wait state.

- **CSRCV: CE-ATA Completion Signal Received**

0 = No completion signal received since last status read operation.

1 = The device has issued a command completion signal on the command line. Cleared by reading in the HSMCI_SR register.

- **RXBUFF: RX Buffer Full**

0 = HSMCI_RCR or HSMCI_RNCR has a value other than 0.

1 = Both HSMCI_RCR and HSMCI_RNCR have a value of 0.

- **TXBUFE: TX Buffer Empty**

0 = HSMCI_TCR or HSMCI_TNCR has a value other than 0.

1 = Both HSMCI_TCR and HSMCI_TNCR have a value of 0.

Note: BLKE and NOTBUSY flags can be used to check that the data has been successfully transmitted on the data lines and not only transferred from the PDC to the HSMCI Controller.

- **RINDE: Response Index Error**

0 = No error.

1 = A mismatch is detected between the command index sent and the response index received. Cleared when writing in the HSMCI_CMDR.

- **RDIRE: Response Direction Error**

0 = No error.

1 = The direction bit from card to host in the response has not been detected.

40.7.45 PWM Channel Dead Time Register

Name: PWM_DTx [x=0..3]

Address: 0x40000218 [0], 0x40000238 [1], 0x40000258 [2], 0x40000278 [3]

Access: Read-write

31	30	29	28	27	26	25	24
DTL							

23	22	21	20	19	18	17	16
DTL							

15	14	13	12	11	10	9	8
DTH							

7	6	5	4	3	2	1	0
DTH							

This register can only be written if the bits WPSWS4 and WPHWS4 are cleared in “PWM Write Protect Status Register” on page 1070.

Only the first 12 bits (dead-time counter size) of fields DTH and DTL are significant.

- **DTH: Dead-Time Value for PWMHx Output**

Defines the dead-time value for PWMHx output. This value must be defined between 0 and CPRD-CDTY (PWM_CPRx and PWM_CDTYx).

- **DTL: Dead-Time Value for PWMLx Output**

Defines the dead-time value for PWMLx output. This value must be defined between 0 and CDTY (PWM_CDTYx).

41.6.1.3 USB Transfer Event Definitions

As indicated below, transfers are sequential events carried out on the USB bus.

Table 41-5. USB Transfer Events

Control Transfers(1) (3)	• Setup transaction > Data IN transactions > Status OUT transaction • Setup transaction > Data OUT transactions > Status IN transaction • Setup transaction > Status IN transaction
Interrupt IN Transfer (device toward host)	• Data IN transaction > Data IN transaction
Interrupt OUT Transfer (host toward device)	• Data OUT transaction > Data OUT transaction
Isochronous IN Transfer(2) (device toward host)	• Data IN transaction > Data IN transaction
Isochronous OUT Transfer(2) (host toward device)	• Data OUT transaction > Data OUT transaction
Bulk IN Transfer (device toward host)	• Data IN transaction > Data IN transaction
Bulk OUT Transfer (host toward device)	• Data OUT transaction > Data OUT transaction

Notes: 1. Control transfer must use endpoints with no ping-pong attributes.
2. Isochronous transfers must use endpoints with ping-pong attributes.
3. Control transfers can be aborted using a stall handshake.

A status transaction is a special type of host-to-device transaction used only in a control transfer. The control transfer must be performed using endpoints with no ping-pong attributes. According to the control sequence (read or write), the USB device sends or receives a status transaction.

42.7.8 ACC Write Protect Mode Register

Name: ACC_WPMR

Address: 0x400BC0E4

Access: Read-write

31	30	29	28	27	26	25	24
WPKEY							
23	22	21	20	19	18	17	16
WPKEY							
15	14	13	12	11	10	9	8
WPKEY							
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	WPEN

- **WPEN: Write Protect Enable**

0 = Disables the Write Protect if WPKEY corresponds to 0x414343 (“ACC” in ASCII).

1 = Enables the Write Protect if WPKEY corresponds to 0x414343 (“ACC” in ASCII).

Protects the registers:

- “ACC Mode Register” on page 1133
- “ACC Analog Control Register” on page 1138

- **WPKEY: Write Protect KEY**

This security code is needed to set/reset the WPROT bit value (see Section 42.6.3 ”Write Protection System” for details).

Must be filled with “ACC” ASCII code.

44.7.11 Interrupt Enable Register

Name: GMAC_IER

Address: 0x40034028

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	WOL	–	SRI	PDRSFT	PDRQFT
23	22	21	20	19	18	17	16
PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR	–	–
15	14	13	12	11	10	9	8
EXINT	PFTR	PTZ	PFNZ	HRESP	ROVR	–	–
7	6	5	4	3	2	1	0
TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS

At reset all interrupts are disabled. Writing a one to the relevant bit location enables the required interrupt. This register is write only and when read will return zero.

- **MFS: Management Frame Sent**

Enable management done interrupt.

- **RCOMP: Receive Complete**

Enable receive complete interrupt.

- **RXUBR: RX Used Bit Read**

Enable receive used bit read interrupt.

- **TXUBR: TX Used Bit Read**

Enable transmit used bit read interrupt.

- **TUR: Transmit Under Run**

Enable transmit buffer under run interrupt.

- **RLEX: Retry Limit Exceeded or Late Collision**

Enable retry limit exceeded or late collision interrupt.

- **TFC: Transmit Frame Corruption due to AHB error**

Enable transmit frame corruption due to AHB error interrupt.

- **TCOMP: Transmit Complete**

Enable transmit complete interrupt.

- **ROVR: Receive Overrun**

Enable receive overrun interrupt.

- **HRESP: HRESP Not OK**

Enable HRESP not OK interrupt.

1 = Interrupt is disabled.

A write to this register directly affects the state of the corresponding bit in the Interrupt Status Register, causing an interrupt to be generated if a 1 is written.

- **TUR: Transmit Under Run**

A read of this register returns the value of the transmit buffer under run interrupt mask.

0 = Interrupt is enabled.

1 = Interrupt is disabled.

A write to this register directly affects the state of the corresponding bit in the Interrupt Status Register, causing an interrupt to be generated if a 1 is written.

- **RLEX: Retry Limit Exceeded**

A read of this register returns the value of the retry limit exceeded interrupt mask.

0 = Interrupt is enabled.

1 = Interrupt is disabled.

A write to this register directly affects the state of the corresponding bit in the Interrupt Status Register, causing an interrupt to be generated if a 1 is written.

- **TFC: Transmit Frame Corruption due to AHB error**

A read of this register returns the value of the transmit frame corruption due to AHB error interrupt mask.

0 = Interrupt is enabled.

1 = Interrupt is disabled.

A write to this register directly affects the state of the corresponding bit in the Interrupt Status Register, causing an interrupt to be generated if a 1 is written.

- **TCOMP: Transmit Complete**

A read of this register returns the value of the transmit complete interrupt mask.

0 = Interrupt is enabled.

1 = Interrupt is disabled.

A write to this register directly affects the state of the corresponding bit in the Interrupt Status Register, causing an interrupt to be generated if a 1 is written.

- **ROVR: Receive Overrun**

A read of this register returns the value of the receive overrun interrupt mask.

0 = Interrupt is enabled.

1 = Interrupt is disabled.

A write to this register directly affects the state of the corresponding bit in the Interrupt Status Register, causing an interrupt to be generated if a 1 is written.

- **HRESP: HRESP Not OK**

A read of this register returns the value of the HRESP not OK interrupt mask.

0 = Interrupt is enabled.

1 = Interrupt is disabled.

A write to this register directly affects the state of the corresponding bit in the Interrupt Status Register, causing an interrupt to be generated if a 1 is written.

44.7.25 Specific Address 4 Bottom Register[31:0]

Name: GMAC_SAB4

Address: 0x400340A0

Access: Read-write

31	30	29	28	27	26	25	24
ADDR							

23	22	21	20	19	18	17	16
ADDR							

15	14	13	12	11	10	9	8
ADDR							

7	6	5	4	3	2	1	0
ADDR							

The addresses stored in the Specific Address Registers are deactivated at reset or when their corresponding Specific Address Register Bottom is written. They are activated when Specific Address Register Top is written.

- **ADDR: Specific Address 4**

Least significant 32 bits of the destination address, that is bits 31:0. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received.

44.7.26 Specific Address 4 Top Register[47:32]

Name: GMAC_SAT4

Address: 0x400340A4

Access: Read-write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
ADDR							

7	6	5	4	3	2	1	0
ADDR							

The addresses stored in the Specific Address Registers are deactivated at reset or when their corresponding Specific Address Register Bottom is written. They are activated when Specific Address Register Top is written.

- **ADDR: Specific Address 4**

The most significant bits of the destination address, that is bits 47:32.

44.7.36 Octets Transmitted [31:0] Register

Name: GMAC_OTLO

Address: 0x40034100

Access: Read-only

31	30	29	28	27	26	25	24
TXO							

23	22	21	20	19	18	17	16
TXO							

15	14	13	12	11	10	9	8
TXO							

7	6	5	4	3	2	1	0
TXO							

When reading the Octets Transmitted and Octets Received Registers, bits 31:0 should be read prior to bits 47:32 to ensure reliable operation.

- **TXO: Transmitted Octets**

Transmitted octets in frame without errors [31:0]. The number of octets transmitted in valid frames of any type. This counter is 48-bits, and is read through two registers. This count does not include octets from automatically generated pause frames.

44.7.37 Octets Transmitted [47:32] Register

Name: GMAC_OTHI

Address: 0x40034104

Access: Read-only

31	30	29	28	27	26	25	24
–							

23	22	21	20	19	18	17	16
–							

15	14	13	12	11	10	9	8
TXO							

7	6	5	4	3	2	1	0
TXO							

When reading the Octets Transmitted and Octets Received Registers, bits 31:0 should be read prior to bits 47:32 to ensure reliable operation.

- **TXO: Transmitted Octets**

Transmitted octets in frame without errors [47:32]. The number of octets transmitted in valid frames of any type. This counter is 48-bits, and is read through two registers. This count does not include octets from automatically generated pause frames.

44.7.71 Jabbers Received Register

Name: GMAC_JR

Address: 0x4003418C

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	JRX	
7	6	5	4	3	2	1	0
JRX							

- **JRX: Jabbers Received**

The register counts the number of frames received exceeding 1518 bytes in length (1536 if bit 8 is set in Network Configuration Register) and have either a CRC error, an alignment error or a receive symbol error. See: Section 44.7.2 ”Network Configuration Register”.

44.7.72 Frame Check Sequence Errors Register

Name: GMAC_FCSE

Address: 0x40034190

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	FCKR	
7	6	5	4	3	2	1	0
FCKR							

- **FCKR: Frame Check Sequence Errors**

The register counts frames that are an integral number of bytes, have bad CRC and are between 64 and 1518 bytes in length (1536 if bit 8 is set in Network Configuration Register). This register is also incremented if a symbol error is detected and the frame is of valid length and has an integral number of bytes.

This register is incremented for a frame with bad FCS, regardless of whether it is copied to memory due to ignore FCS mode being enabled in bit 26 of the Network Configuration Register. See: Section 44.7.2 ”Network Configuration Register”.