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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

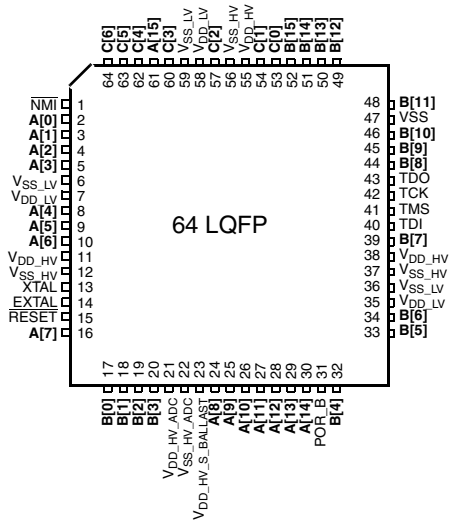
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, WDT
Number of I/O	39
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5604eef1mlh

2 Package pinouts and signal descriptions

2.1 Package pinouts

The LQFP pinouts are shown in the following figures.



Note:
1. All VDD_HV and VSS_HV pins must be shorted on the board. The ADC supply (VDD_HV_ADC) and ground (VSS_HV_ADC) should be managed independently from other high-voltage supplies, (it may still be supplied from the same high-voltage source, but caution must be taken while routing it on the board.)
2. All VDD_LV and VSS_LV pins must be shorted on the board.

Figure 2. 64-pin LQFP pinout(top view)

Table 4. Pin muxing

Port pin	PCR register	Alternate function[1,2,8]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin[6]	
						SRC = 0	SRC = 1	64-pin	100-pin[7]
Port A (16-bit)									
A[0]	PCR[0]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[0] D[0] — — D[11] SIN EIRQ[0]	SIUL SAI0 — — VID DSPI 1 SIUL	I/O I/O — — I I I	Slow	Medium	2	2
A[1]	PCR[1]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[1] D[1] SOUT — D[10] EIRQ[1]	SIUL SAI0 DSPI1 — VID SIUL	I/O I/O O — I I	Slow	Medium	3	4
A[2]	PCR[2]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[2] D[2] SCK D[0] D[9] ETC[5] EIRQ[2]	SIUL SAI0 DSPI1 SAI1 VID ETIMER0 SIUL	I/O I/O I/O I/O I I I	Slow	Medium	4	6
A[3]	PCR[3]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[3] D[3] — D[0] D[8] SIN EIRQ[3]	SIUL SAI0 — SAI2 VID DSPI2 SIUL	I/O I/O — I/O I I I	Slow	Medium	5	8
A[4]	PCR[4]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[4] SYNC SOUT — D[7] ETC[3] EIRQ[4]	SIUL SAI0 DSPI2 — VID ETIMER0 SIUL	I/O I/O O — I I I	Slow	Medium	8	15
A[5]	PCR[5]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[5] SYNC SCK D[0] CLK ETC[4] EIRQ[5]	SIUL SAI1 DSPI2 SAI1 VID ETIMER0 SIUL	I/O I/O I/O I/O I I I	Medium	Fast	9	16

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2,8]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin[6]	
						SRC = 0	SRC = 1	64-pin	100-pin[7]
A[6]	PCR[6]	ALT0 ALT1 ALT2 ALT3 — — — —	GPIO[6] SYNC CS0 — VSYNC D[0] ETC[1] EIRQ[6]	SIUL SAI2 DSPI2 — VID VID ETIMER0 SIUL	I/O I/O I/O — I I I I	Slow	Medium	10	17
A[7]	PCR[7]	ALT0 ALT1 ALT2 ALT3 — — — —	GPIO[7] BCLK CS1 — HREF D[1] ETC[2] EIRQ[7]	SIUL SAI0 DSPI2 — VID VID ETIMER0 SIUL	I/O I/O I/O — I I I I	Slow	Medium	16	23
A[8]	PCR[8]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[8] BCLK CS0 D[0] D[6] RX EIRQ[8]	SIUL SAI1 DSPI1 SAI2 VID LIN1 SIUL	I/O I/O I/O I/O I I I	Slow	Medium	24	37
A[9]	PCR[9]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[9] BCLK CS1 TX D[5] EIRQ[9]	SIUL SAI2 DSPI1 LIN1 VID SIUL	I/O I/O I/O O I I	Slow	Medium	25	38
A[10]	PCR[10]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[10] MCLK ETC[5] — D[4] SIN EIRQ[10]	SIUL SAI2 ETIMER0 — VID DSPI0 SIUL	I/O I/O I/O — I I I	Slow	Medium	26	39
A[11]	PCR[11]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[11] TX CS1 CS0 D[3] RX RX	SIUL CAN0 DSPI0 DSPI1 VID LIN0 LIN1	I/O O O I/O I I I	Slow	Medium	27	40

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2,8]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin[6]	
						SRC = 0	SRC = 1	64-pin	100-pin[7]
B[3]	PCR[19]	ALT0 ALT1 ALT2 ALT3 — — — —	GPIO[19] ETC[2] SOUT PPS1 AN[3] RX EIRQ[14] —	SIUL ETIMER0 DSPI0 CE_RTC ADC0[8] LIN0 SIUL —	I/O I/O O I I I I —	Slow	Medium	20	29
B[4]	PCR[20]	ALT0 ALT1 ALT2 ALT3 —	GPIO[20] — — — RX_DV	SIUL — — — FEC	I/O — — — I	Slow	Medium	32	50
B[5]	PCR[21]	ALT0 ALT1 ALT2 ALT3	GPIO[21] TX_D0 DEBUG[0] —	SIUL FEC SSCM —	I/O O I/O —	Slow	Medium	33	55
B[6]	PCR[22]	ALT0 ALT1 ALT2 ALT3	GPIO[22] TX_D1 DEBUG[1] —	SIUL FEC SSCM —	I/O O I/O —	Slow	Medium	34	56
B[7]	PCR[23]	ALT0 ALT1 ALT2 ALT3	GPIO[23] TX_D2 DEBUG[2] —	SIUL FEC SSCM —	I/O O I/O —	Slow	Medium	39	62
B[8]	PCR[24]	ALT0 ALT1 ALT2 ALT3	GPIO[24] TX_D3 DEBUG[3] —	SIUL FEC SSCM —	I/O O I/O —	Slow	Medium	44	67
B[9]	PCR[25]	ALT0 ALT1 ALT2 ALT3	GPIO[25] TX_EN DEBUG[4] —	SIUL FEC SSCM —	I/O O I/O —	Slow	Medium	45	70
B[10]	PCR[26]	ALT0 ALT1 ALT2 ALT3	GPIO[26] MDC DEBUG[5] —	SIUL FEC SSCM —	I/O O I/O —	Slow	Medium	46	73
B[11]	PCR[27]	ALT0 ALT1 ALT2 ALT3	GPIO[27] MDIO DEBUG[6] —	SIUL FEC SSCM —	I/O I/O I/O —	Slow	Medium	48	75
B[12]	PCR[28]	ALT0 ALT1 ALT2 ALT3 —	GPIO[28] — DEBUG[7] — TX_CLK	SIUL — SSCM — FEC	I/O — I/O — I	Slow	Medium	49	76

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2,8]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin[6]	
						SRC = 0	SRC = 1	64-pin	100-pin[7]
C[4]	PCR[36]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[36] CLK_OUT ETC[4] MCLK TRIGGER1 ABS[0] EIRQ[19]	SIUL MC_CGL ETIMER0 SAI0 CE_RTC MC_RGM SIUL	I/O O I/O I/O I I I	Medium	Fast	62	96
C[5]	PCR[37]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[37] CLK ETC[3] CS2 ABS[2] EIRQ[20]	SIUL IIC0 ETIMER0 DSPI2 MC_RGM SIUL	I/O — I/O O I I	Slow	Medium	63	99
C[6]	PCR[38]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[38] DATA CS0 CS3 FAB EIRQ[21]	SIUL IIC0 DSPI1 DSPI2 MC_RGM SIUL	I/O — I/O O I I	Slow	Medium	64	100
C[7]	PCR[39]	ALT0 ALT1 ALT2 ALT3 —	GPIO[39] TXD — — RXD	SIUL LIN0 — — LIN1	I/O O — — I	Slow	Medium	—	3
C[8]	PCR[40]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[40] TXD — — RXD EIRQ[22]	SIUL LIN1 — — LIN0 SIUL	I/O O — — I I	Slow	Medium	—	5
C[9]	PCR[41]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[41] — — — SIN EIRQ[23]	SIUL — — — DSPI0 SIUL	I/O — — — I I	Slow	Medium	—	7
C[10]	PCR[42]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[42] ETC[5] ETC[4] — SIN EIRQ[24]	SIUL ETIMER0 ETIMER0 — DSPI1 SIUL	I/O I/O I/O — I I	Slow	Medium	—	24
C[11]	PCR[43]	ALT0 ALT1 ALT2 ALT3	GPIO[43] ETC[2] ETC[1] ETC[3]	SIUL ETIMER0 ETIMER0 ETIMER0	I/O I/O I/O I/O	Slow	Medium	—	25

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2,8]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin[6]	
						SRC = 0	SRC = 1	64-pin	100-pin[7]
C[12]	PCR[44]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[44] PPS1 PPS2 ALARM1 TRIGGER1 TRIGGER2 EIRQ[25]	SIUL CE_RTC CE_RTC CE_RTC CE_RTC CE_RTC SIUL	I/O O O O I I I	Slow	Medium	—	44
C[13]	PCR[45]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[45] — — — D[1] EIRQ[26]	SIUL — — — VID SIUL	I/O — — — I I	Slow	Medium	—	46
C[14]	PCR[46]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[46] — — — D[0] EIRQ[27]	SIUL — — — VID SIUL	I/O — — — I I	Slow	Medium	—	47
C[15]	PCR[47]	ALT0 ALT1 ALT2 ALT3 —	GPIO[47] — — — COL	SIUL — — — FEC	I/O — — — I	Slow	Medium	—	48
Port D (100-pin package: 16-bit)									
D[0]	PCR[48]	ALT0 ALT1 ALT2 ALT3	GPIO[48] MDO0 — —	SIUL NEXUS — —	I/O O — —	Slow	Medium	—	9
D[1]	PCR[49]	ALT0 ALT1 ALT2 ALT3	GPIO[49] MCK0 — —	SIUL NEXUS — —	I/O O — —	Slow	Medium	—	14
D[2]	PCR[50]	ALT0 ALT1 ALT2 ALT3	GPIO[50] EVTO — —	SIUL NEXUS — —	I/O O — —	Slow	Medium	—	13
D[3]	PCR[51]	ALT0 ALT1 ALT2 ALT3	GPIO[51] MSEO1 — —	SIUL NEXUS — —	I/O O — —	Slow	Medium	—	72
D[4]	PCR[52]	ALT0 ALT1 ALT2 ALT3	GPIO[52] MSEO0 — —	SIUL NEXUS — —	I/O O — —	Slow	Medium	—	78

Table 4. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2,8]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin[6]	
						SRC = 0	SRC = 1	64-pin	100-pin[7]
D[5]	PCR[53]	ALT0 ALT1 ALT2 ALT3	GPIO[53] MDO3 — —	SIUL NEXUS — —	I/O O — —	Slow	Medium	—	80
D[6]	PCR[54]	ALT0 ALT1 ALT2 ALT3	GPIO[54] MDO2 — —	SIUL NEXUS — —	I/O O — —	Slow	Medium	—	84
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3	GPIO[55] MDO1 — —	SIUL NEXUS — —	I/O — — —	Slow	Medium	—	98
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3 —	GPIO[56] — — — EVTI	SIUL — — — NEXUS	I/O — — — I	Slow	Medium	—	10
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[57] ETC[3] ETC[2] — RXD EIRQ[28]	SIUL ETIMER0 ETIMER0 — CAN0 SIUL	I/O I/O I/O — I I	Slow	Medium	—	49
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	GPIO[58] TXD — —	SIUL CAN0 — —	I/O O — —	Slow	Medium	—	51
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] ETC[0] ETC[5] ETC[4]	SIUL ETIMER0 ETIMER0 ETIMER0	I/O I/O I/O I/O	Slow	Medium	—	52
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3 —	GPIO[60] ETC[1] ETC[0] — SIN	SIUL ETIMER0 ETIMER0 — DSPI0	I/O I/O I/O — I	Slow	Medium	—	53
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[61] — — — CRS EIRQ[29]	SIUL — — — FEC SIUL	I/O — — — I I	Slow	Medium	—	54

[2] Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIU module. PCR.PA = 00 → ALT0; PCR.PA = 01 → ALT1; PCR.PA = 10 → ALT2; PCR.PA = 11 → ALT3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

[3] Module included on the MCU.

[4] Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.

[5] Programmable via the SRC (Slew Rate Control) bits in the respective Pad Configuration Register.

[6] Additional board pull resistors are recommended when JTAG pins are not being used on the board or application.

[7] The 100-pin package is not a production package. It is used for software development only.

[8] Do not use ALT multiplexing when ADC channels are used.

3.3 Absolute maximum ratings

Table 6. Absolute Maximum Ratings[1]

Symbol		Parameter	Conditions	Min	Max[2]	Unit
V_{SS}	SR	Device ground	—	V_{SS}	V_{SS}	V
$V_{DD\_HV\_IO}$	SR	3.3 V Input/Output Supply Voltage (supply). Code Flash supply with $V_{DD\_HV\_IO3}$ and Data Flash with $V_{DD\_HV\_IO2}$	—	V_{SS} _ 0.3	V_{SS} + 6.0	V
$V_{SS\_HV\_IO}$	SR	3.3 VInput/Output Supply Voltage (ground). Code Flash ground with $V_{SS\_HV\_IO3}$ and Data Flash with $V_{SS\_HV\_IO2}$	—	V_{SS} _ 0.1	V_{SS} + 0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V Crystal Oscillator Amplifier Supply voltage (supply)	The oscillator and flash supply segments are double-bounded with the $V_{DD\_HV\_IO}$ segments. See $V_{DD\_HV\_IO}$ and $V_{SS\_HV\_IO}$ specifications.			—
$V_{SS\_HV\_OSC}$	SR	3.3 V Crystal Oscillator Amplifier Supply voltage (ground)				
$V_{DD\_HV\_ADC0}$[3]	SR	3.3 V ADC_0 Supply and High Reference voltage	—	V_{SS} _ 0.3	V_{SS} + 6.0	V
$V_{SS\_HV\_ADC0}$	SR	3.3 V ADC_0 Ground and Low Reference voltage	—	V_{SS} _ 0.1	V_{SS} + 0.1	V
$V_{DD\_HV\_REG}$	SR	3.3 V Voltage Regulator Supply voltage	—	V_{SS} _ 0.3	V_{SS} + 6.0	V
TV_{DD}	SR	Slope characteristics on all VDD during power up[4]	—	—	0.1	V/us
$V_{DD\_LV\_COR}$	SR	1.2 V supply pins for core logic (supply)	—	V_{SS} _ 0.3	V_{SS} + 1.4	V
$V_{SS\_LV\_COR}$	SR	1.2 V supply pins for core logic (ground)	—	V_{SS} _ 0.1	V_{SS} + 0.1	V
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS\_HV\_IO}$)	—	$V_{SS\_HV\_IO}$ _ 0.3	$V_{DD\_HV\_IO}$ +0.5	V
I_{INJPAD}	SR	Input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all input currents during overload condition	—	–50	50	mA
$T_{STORAGE}$	SR	Storage temperature	—	–55	150	°C
T_J	SR	Junction temperature under bias	—	–40	150	°C
T_A	SR	Ambient temperature under bias	f_{CPU}<64 MHz	–40	125	°C
			f_{CPU}<64 MHz Video use case with internal supply	–40	105	°C

1 Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134 U.S.A.
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, *An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module*, Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
2. G. Kromann, S. Shidore, and S. Addison, *Thermal Modeling of a PBGA for Air-Cooled Applications*, Electronic Packaging and Production, pp. 53-58, March 1998.
3. B. Joiner and V. Adams, *Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling*, Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

3.6 Electromagnetic Interference (EMI) characteristics

Table 10. EMI Testing Specifications[1]

Symbol	Parameter	Conditions	Clocks	Frequency Range	Level (Typ)	Unit
Radiated emissions	V_{EME}	V_{DD} = 3.3 V T_A = +25 °C Device Configuration, test conditions and EM testing per standard IEC61967-2.	Oscillator Frequency = 8 MHz; System Bus Frequency = 64 MHz; CPU Freq = 64MHZ No PLL Frequency Modulation	150 kHz–50 MHz	2	dBμV
				50–150 MHz	14	
				150–500 MHz	11	
				500–1000 MHz	7	
				IEC Level	M	
			External Oscillator Freq = 8 MHz System Bus Freq = 64 MHz CPU Freq = 64MHZ 2% PLL Freq Modulation	150 kHz–50 MHz	1	dBμV
				50–150 MHz	11	
				150–500 MHz	7	
				500–1000 MHz	1	
				IEC Level	N	

[1] EMI testing and I/O port waveforms per standard IEC61967-2.

be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (fc \times C_S)$, where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the Equation 4:

Eqn. 4

$$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

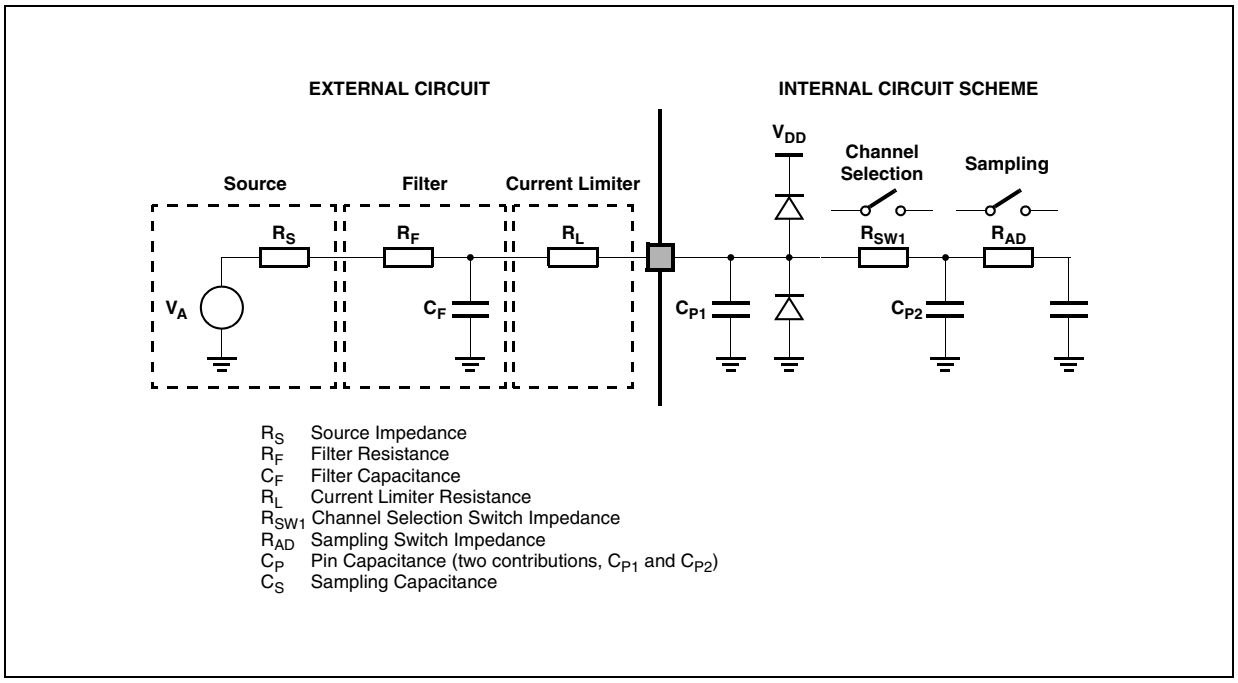


Figure 10. Input equivalent circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 10): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

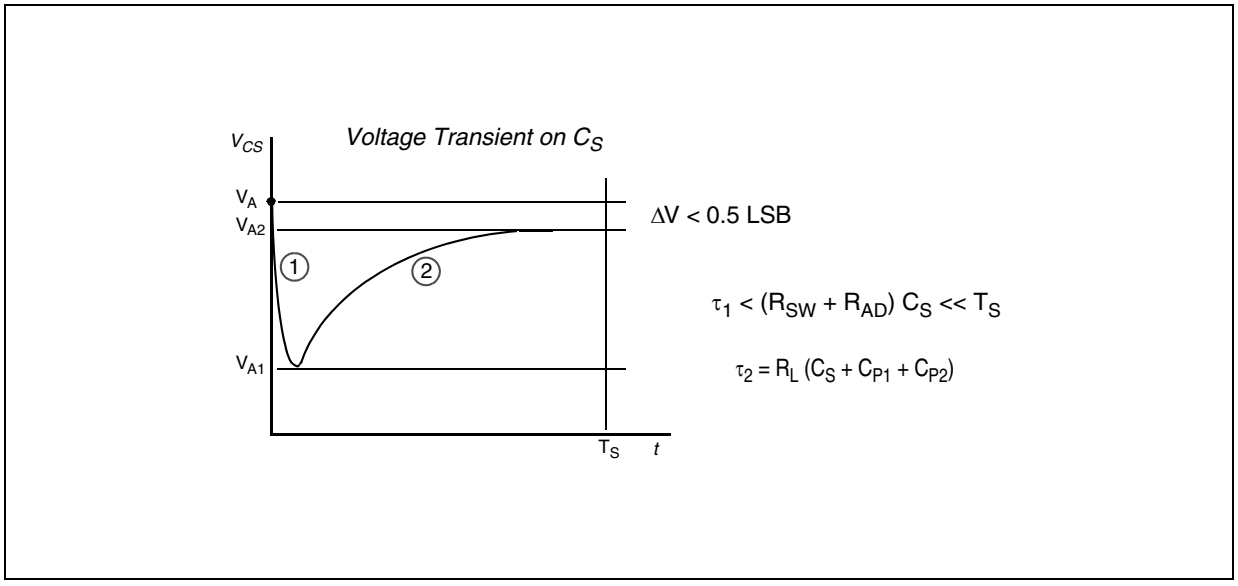


Figure 11. Transient behavior during sampling phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Eqn. 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

Eqn. 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

1 V_{DD} = 3.3 V to 3.6 V, T_A = –40 to +125 °C, unless otherwise specified and analog input voltage from V_{AGND} to V_{AREF}

2 ADCClk clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.

3 During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.

4 This parameter does not include the sample time t_{ADC_S}, but only the time for determining the digital result and the time to load the result register with the conversion result.

5 20 MHz ADC clock. Specific prescaler is programmed on MC_PLL_CLK to provide 20 MHz clock to the ADC.

6 See Figure 10.

7 Does not include packaging and bonding capacitances

3.15 Temperature sensor electrical characteristics

Table 22. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					min	typical	max	
—	CC	C	Temperature monitoring range	—	–40	—	150	°C
—	CC	C	Sensitivity	—	—	5.14	—	mV/°C
—	CC	C	Accuracy	T_J = –40 to 25 °C	–10	—	10	°C
—	CC	C		T_J = –25 to 125 °C	–10	—	10	°C

3.16 Flash memory electrical characteristics

Table 23. Code flash program and erase specifications[1]

Symbol	Parameter	Min Value	Typical Value[2] (0 Cycles)	Initial Max[3] (100 Cycles)	Max[4] (100000 Cycles)	Unit
T_{DWPRG}	Double Word Program[5]	—	22	50	500	µs
T_{BKPRG}	Bank Program (512 KB)[5, 6]	—	1.45	1.65	33	s
T_{ER8K}	Sector Erase (8KB)	—	0.2	0.4	5.0	s
T_{ER16K}	Sector Erase (16KB)	—	0.3	0.5	5.0	s
T_{ER32K}	Sector Erase (32KB)	—	0.3	0.6	5.0	s
T_{ER64K}	Sector Erase (64KB)	—	0.6	0.9	5.0	s
T_{ER128K}	Sector Erase (128KB)	—	0.8	1.3	7.5	s
T_{ER512K}	Bank Erase (512KB)	—	4.8	7.6	55	s
T_{PABT}	Program Abort Latency	—	—	10	10	µs
T_{EABT}	Erase Abort Latency	—	—	30	30	µs

3.18 AC timing characteristics

3.18.1 Generic timing diagrams

The generic timing diagrams in Figure 14 and Figure 15 apply to all I/O pins with pad types fast, slow and medium. See Section 2.2, "Signal descriptions for the pad type for each pin.

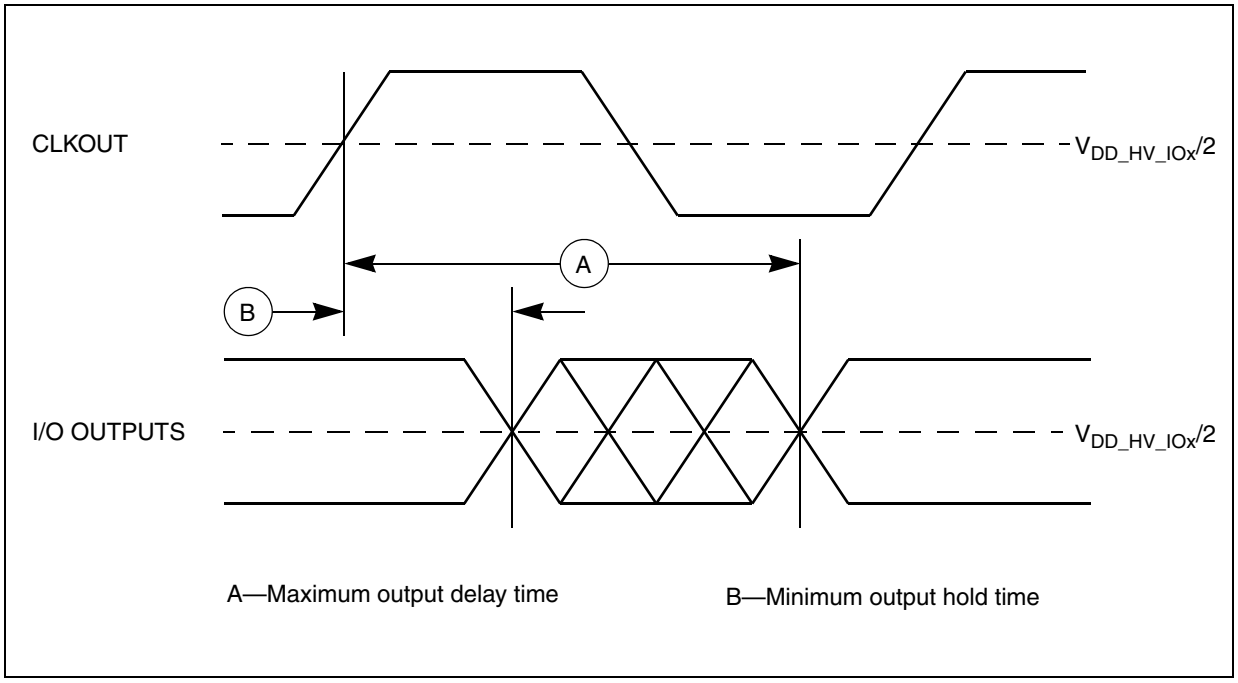


Figure 14. Generic output delay/hold timing

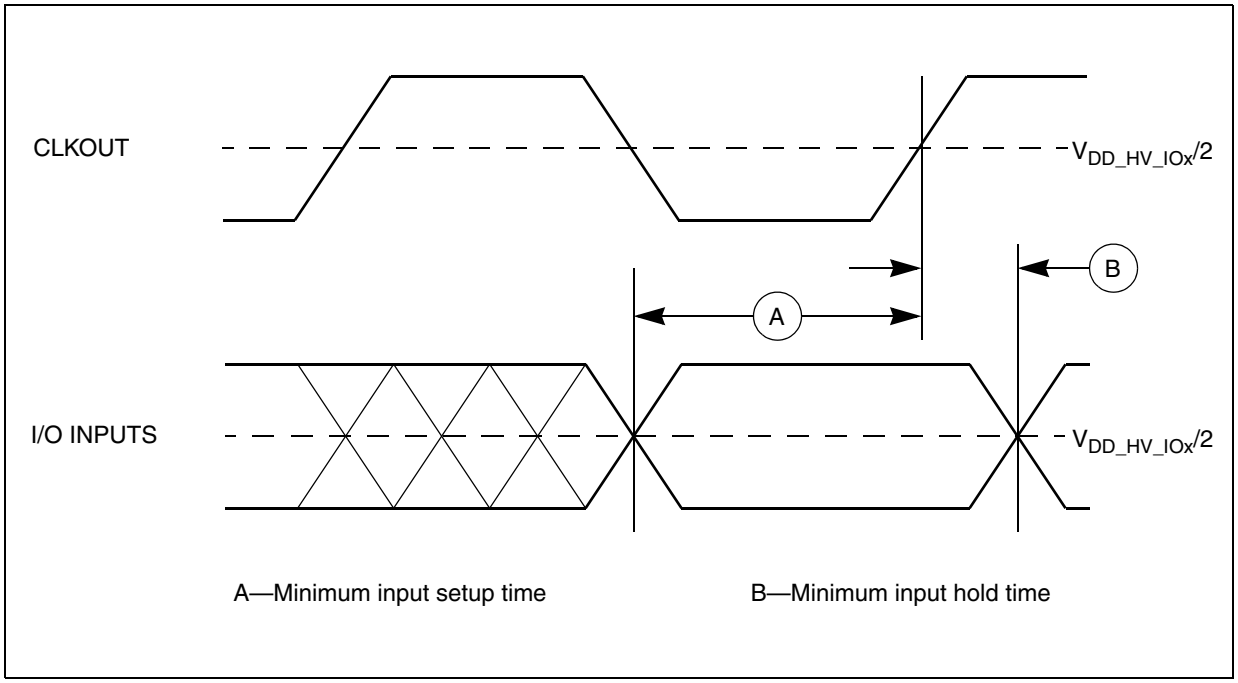


Figure 15. Generic Input setup/hold timing

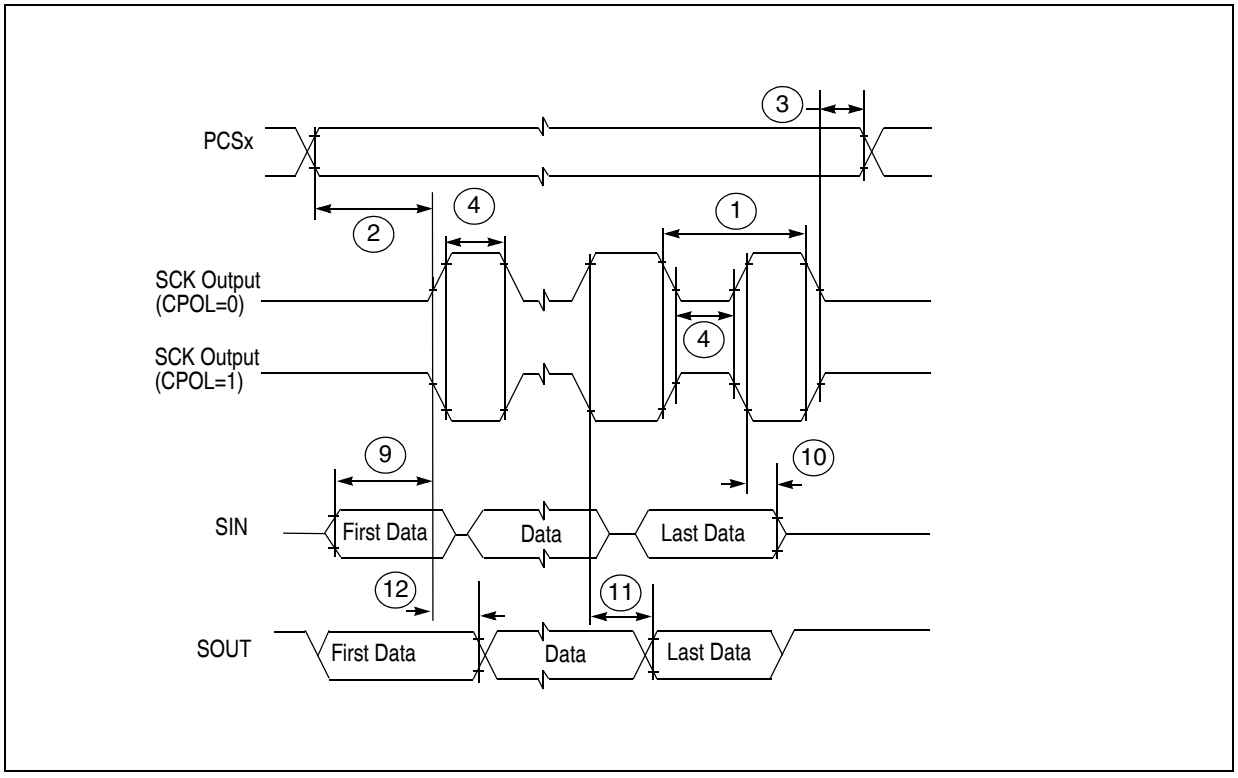


Figure 26. DSPI modified transfer format timing — Master, CPHA = 0

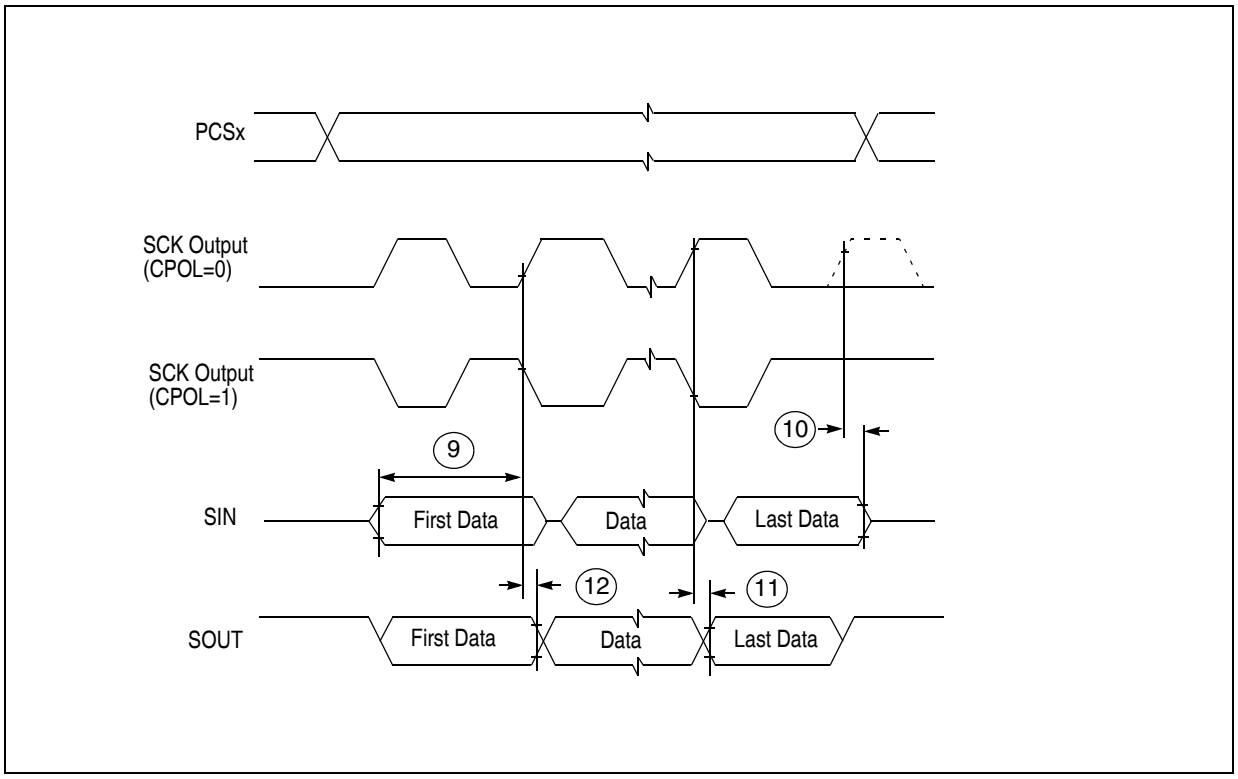


Figure 27. DSPI modified transfer format timing — Master, CPHA = 1

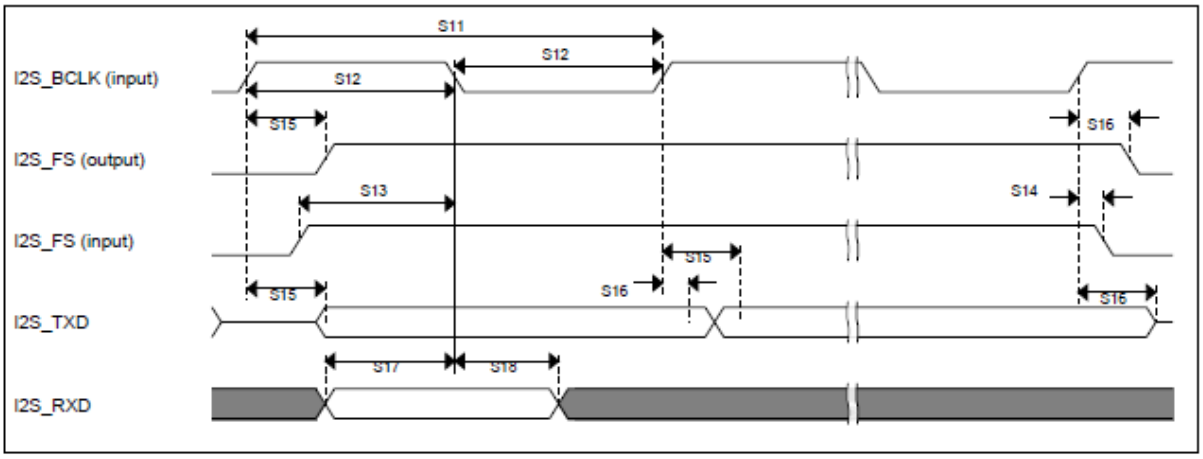


Figure 38. SAI timing slave modes

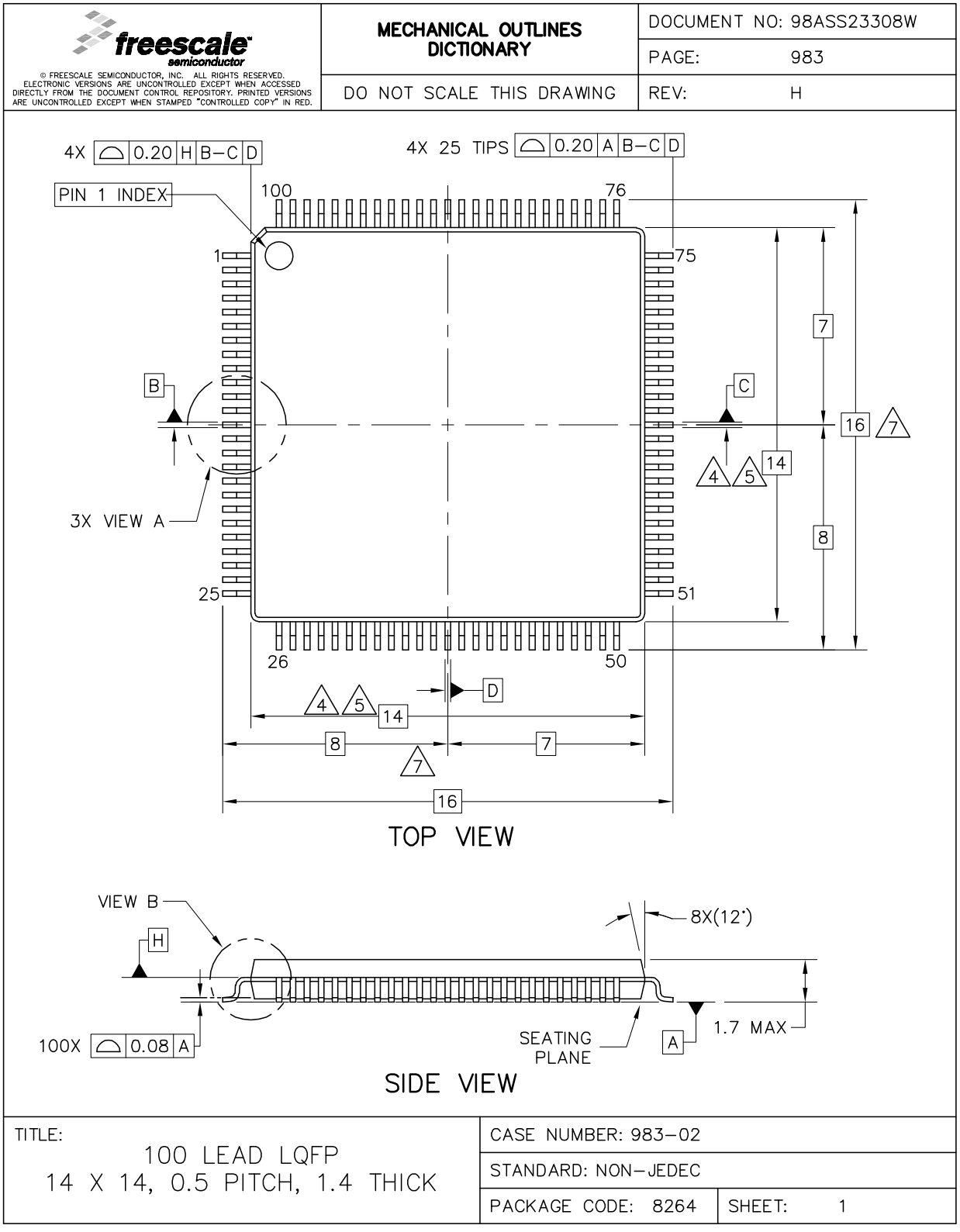


Figure 39. 100 LQFP package mechanical drawing (part 1)

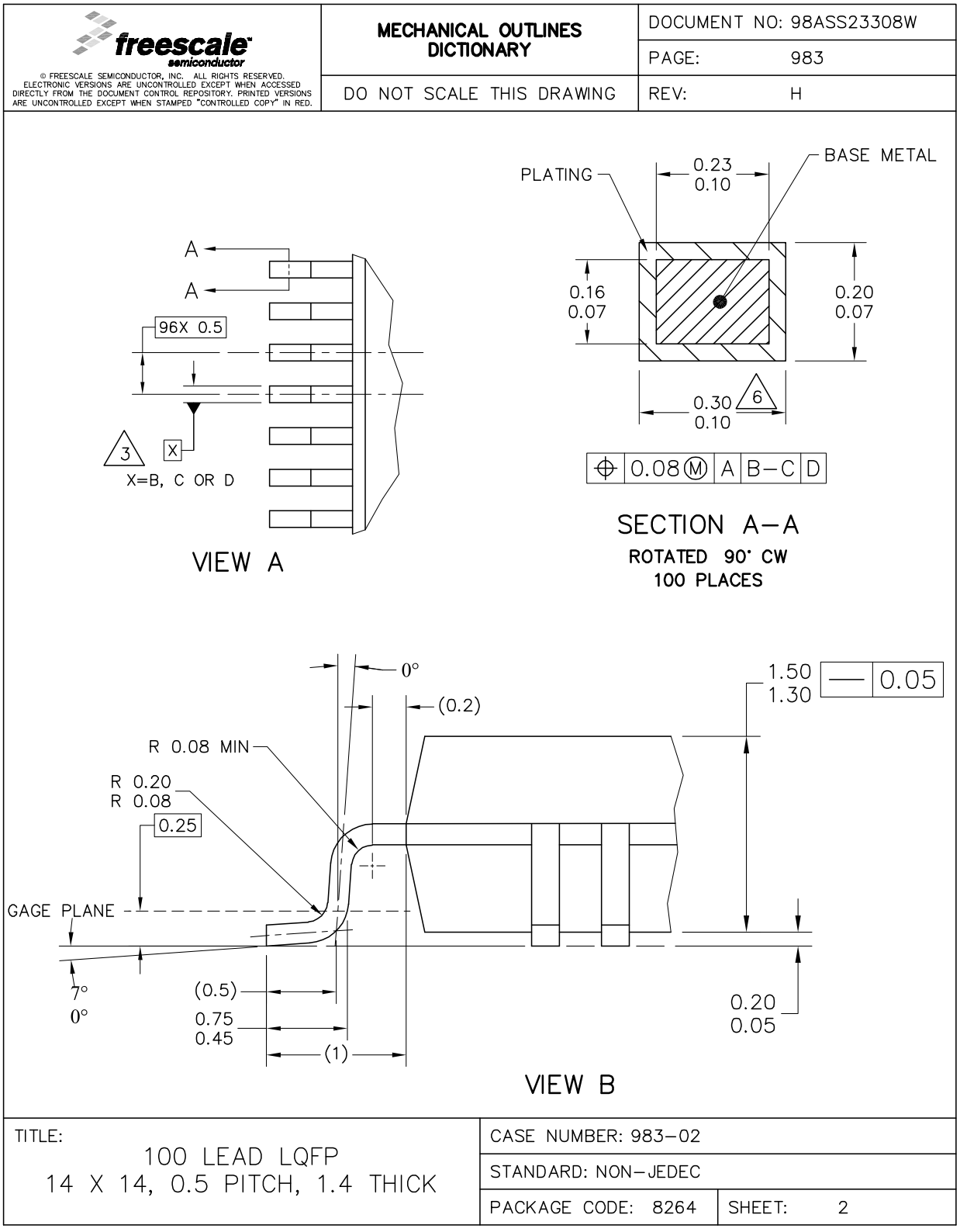
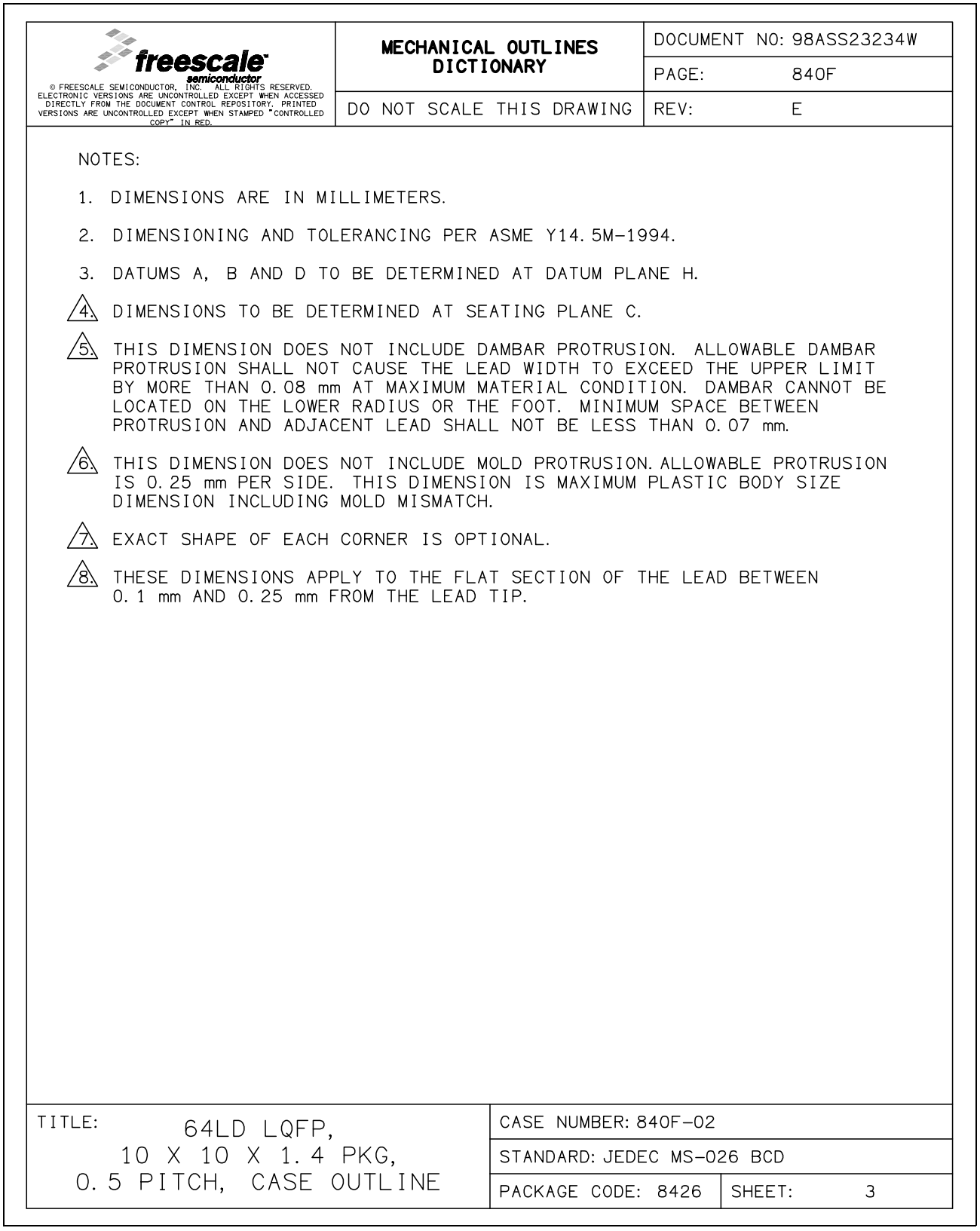


Figure 40. 100 LQFP package mechanical drawing (part 2)



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MECHANICAL OUTLINES
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DO NOT SCALE THIS DRAWING

REV: E

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE

CASE NUMBER: 840F–02

STANDARD: JEDEC MS–026 BCD

PACKAGE CODE: 8426

SHEET: 3

Figure 44. 64LQFP package mechanical drawing (part 3)

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