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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, WDT
Number of I/O	39
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5604eef2mlh

Table 2. Supply pins (continued)

Supply			Pin	
Port Pin	**Multi-bonded Power Supplies/Ground**	**Description**	**64-pin**	**100-pin[1]**
Power supply pins (1.2 V). Pins available on 64-pin and 100-pin package.				
V_{DD_LV}	$V_{DD\_LV\_COR0\_3}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR0\_3}$ pin.	7	12
	$V_{DD\_LV\_PLL0}$	1.2 V PLL supply voltage	7	12
V_{DD_LV}	$V_{DD\_LV\_COR0\_2}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR0\_2}$ pin.	58	92
	$V_{DD\_LV\_FLA0}$	Code and data flash supply voltage	58	92
	$V_{DD\_LV\_COR0\_1}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR0\_1}$ pin.	35	58
	$V_{DD\_LV\_FLA1}$	Code and data flash supply voltage	35	58
V_{SS_LV}	$V_{SS\_LV\_COR0\_3}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected betwee.n these pins and the nearest $V_{DD\_LV\_COR0\_3}$ pin.	6	11
	$V_{SS\_LV\_PLL0}$	PLL supply ground	6	11
	$V_{SS\_LV\_COR0\_2}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected betwee.n these pins and the nearest $V_{DD\_LV\_COR0\_2}$ pin.	59	93
	$V_{SS\_LV\_FLA0}$	Code and data flash supply ground	59	93
	$V_{SS\_LV\_COR0\_1}$	1.2 V supply pins for core logic and data Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR0\_2}$ pin.	36	59
	$V_{SS\_LV\_FLA1}$	Code and data flash supply ground	36	59

[1] The 100-pin package is not a production package. It is used for software development only.

2.2.2 System pins

Table 3 and Table 4 contain information on pin functions for the MPC5604E devices. The pins listed in Table 3 are single-function pins. The pins shown in Table 4 are multi-function pins, programmable via their respective Pad Configuration Register (PCR) values.

2 Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.

3 MPC5604E's I/O, flash, and oscillator circuit supplies are interconnected. The ADC supply managed independently from other supplies.

4 Guaranteed by device validation.

3.4 Recommended operating conditions

Table 7. Recommended operating conditions

Symbol		Parameter	Conditions	Min	Max[1]	Unit
V_{SS}	SR	Device ground	—	V_{SS}	V_{SS}	V
$V_{DD\_HV\_IO}$	SR	3.3 V input/output supply voltage	—	3.0	3.6	V
$V_{SS\_HV\_IO}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	3.3 V Crystal Oscillator Amplifier Supply voltage (supply)	The oscillator and flash supply segments are double-bounded with the $V_{DD\_HV\_IOx}$ segments. See $V_{DD\_HV\_IOx}$ and $V_{SS\_HV\_IOx}$ specifications.			—
$V_{SS\_HV\_OSC}$	SR	3.3 V Crystal Oscillator Amplifier Supply voltage (ground)				
$V_{DD\_HV\_ADC0}$[2]	SR	3.3 V ADC_0 Supply and High Reference voltage	—	3.0	3.6	V
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.6	V
$V_{DD\_LV\_EXTCOR}$	SR	Externally supplied core voltage	—	1.15	1.32	V
$V_{DD\_LV\_REGCOR}$	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_COR}$	SR	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_COR}$	SR	Internal reference voltage	—	0	0	V
$V_{SS\_HV\_ADC0}$	SR	Ground and Low Reference voltage	—	0	0	V
T_J	SR	Junction temperature under bias		–40	150	°C
T_A	SR	Ambient temperature under bias	f_{CPU}<64 MHz	–40	125	°C
			f_{CPU}<64 MHz Video use case with internal supply	–40	105	°C

1 Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.

2 MPC5604E's I/O, flash, and oscillator circuit supplies are interconnected. The ADC supply managed independently from other supplies.

3.5 Thermal characteristics

Table 8. Thermal characteristics for 100-pin LQFP[1]

Symbol	Parameter	Conditions	Typical value	Unit
$R_{\theta JA}$	Thermal resistance junction-to-ambient, natural convection[2]	Single layer board—1s	51	°C/W
		Four layer board—2s2p	38	°C/W
$R_{\theta JMA}$	Thermal resistance junction-to-ambient[2]	@ 200 ft./min.[3], single layer board—1s	41	°C/W
		@ 200 ft./min.[3], four layer board—2s2p	32	°C/W
$R_{\theta JB}$	Thermal resistance junction to board[4]	—	23	°C/W
$R_{\theta JCtop}$	Thermal resistance junction to case (top)[5]	—	11	°C/W
Ψ_{JT}	Junction to package top natural convection[6]	—	2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Flow rate of forced air flow.

4 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

5 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

6 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 9. Thermal characteristics for 64-pin LQFP[1]

Symbol	Parameter	Conditions	Typical value	Unit
$R_{\theta JA}$	Thermal resistance junction-to-ambient, natural convection[2]	Single layer board—1s	64	°C/W
		Four layer board—2s2p	45	°C/W
$R_{\theta JMA}$	Thermal resistance junction-to-ambient[2]	@ 200 ft./min.[3], single layer board—1s	52	°C/W
		@ 200 ft./min.[3], four layer board—2s2p	39	°C/W
$R_{\theta JB}$	Thermal resistance junction to board[4]	—	28	°C/W
$R_{\theta JCtop}$	Thermal resistance junction to case (top)[5]	—	14	°C/W
Ψ_{JT}	Junction to package top natural convection[6]	—	3	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

[3] Flow rate of forced air flow.

[4] Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

[5] Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

[6] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.5.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from Equation 1:

$$T_J = T_A + (R_{\theta JA} * P_D) \qquad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in Equation 2 as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using Equation 3:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

3.7 Electrostatic Discharge (ESD) characteristics

Table 11. ESD ratings[1,2]

Symbol		Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	—	2000	V
$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	—	750 (corners)	V
				500 (other)	

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification

3.8 Power management electrical characteristics

3.8.1 Power Management Overview

The device supports the following power modes:

- Internal voltage regulation mode
- External voltage regulation mode

3.8.1.1 Internal voltage regulation mode

In this mode, the following supplies are involved:

- $V_{DD\_HV\_IO}$ (3.3V) — This is the main supply provided externally.

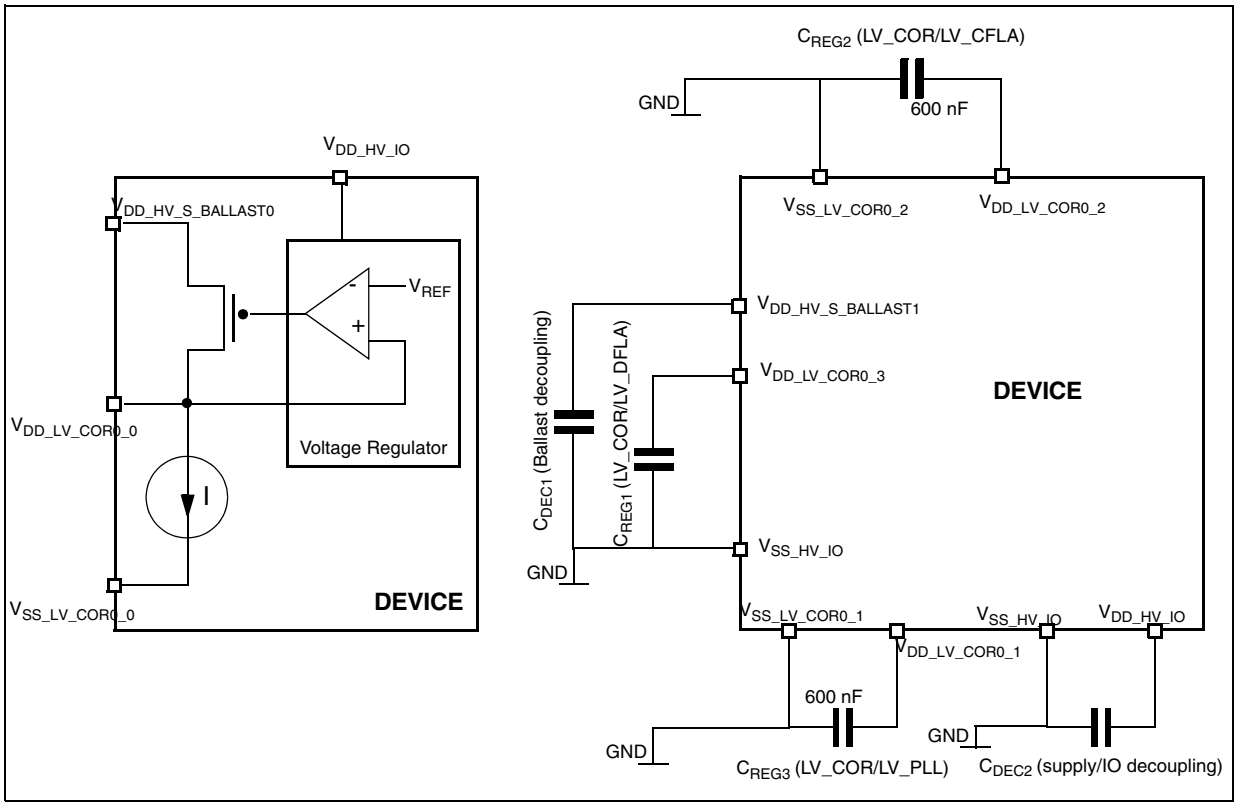

Figure 6. Voltage regulator capacitance connection

Table 13. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{REGn}[2]	SR	—	Internal voltage regulator external capacitance	—	200	—	600	nF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	—	0.05	—	0.2	Ω
C_{DEC1}	SR	—	Decoupling capacitance[3] ballast	—	100[4]	470[5]	—	nF
				—	400		—	
C_{DEC2}	SR	—	Decoupling capacitance regulator supply	—	100 nF	1 μF	—	—
V_{MREG}	CC	T	Main regulator output voltage	Before exiting from reset	—	1.32	—	V
		P		After trimming	1.15	1.28	1.32	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	150	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	

- Several Low Voltage Detectors, working on voltage regulator supply are monitoring the voltage of the critical modules (Voltage regulator, I/Os, Flash and Low voltage domain). LVDs are gated low when POWER_ON is active.
- A POWER_OK signal is generated when all critical supplies monitored by the LVD are available. This signal is active high and released to all modules including I/Os, Flash and RC16 oscillator needed during power-up phase and reset phase. When POWER_OK is low the associated module are set into a safe state.

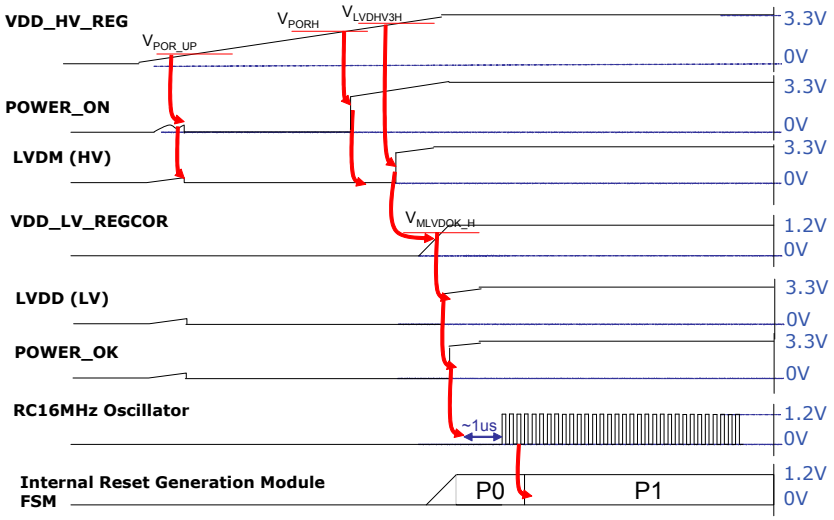

Figure 7. Power-up typical sequence

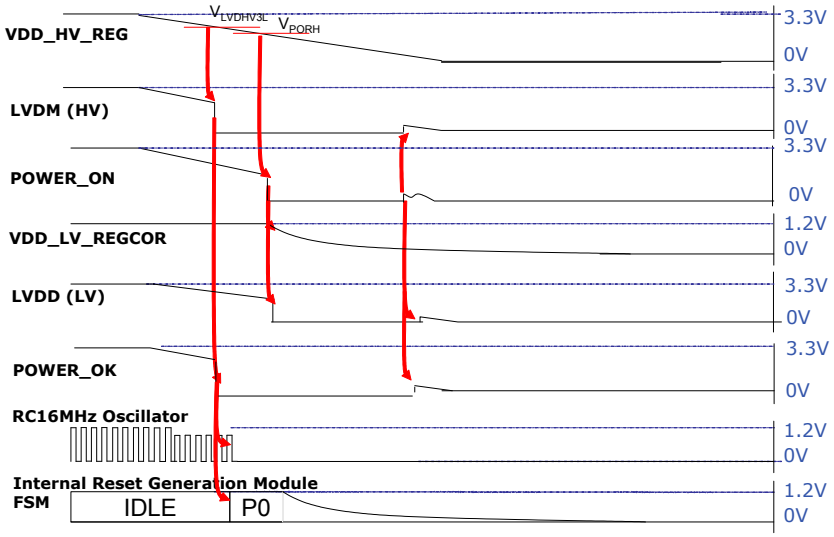

Figure 8. Power-down typical sequence

3.10 DC electrical characteristics

Table 15 gives the DC electrical characteristics at 3.3 V (3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V).

Table 15. DC electrical characteristics (3.3 V)[1]

Symbol		Parameter	Conditions	Min	Max	Unit
V_{IL}	D	Minimum low level input voltage	—	–0.4[2]	—	V
V_{IL}	P	Maximum low level input voltage	—	—	0.35 $V_{DD\_HV\_IO}$	V
V_{IH}	P	Minimum high level input voltage	—	0.65 $V_{DD\_HV\_IO}$	—	V
V_{IH}	D	Maximum high level input voltage	—	—	$V_{DD\_HV\_IO}$ + 0.4[2]	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IO}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 2 mA	—	0.1$V_{DD_HV_IO}$	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –2 mA	0.8$V_{DD_HV_IO}$	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 2 mA	—	0.1$V_{DD_HV_IO}$	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –3 mA	0.8$V_{DD_HV_IO}$	—	V
V_{OL_F}	P	Fast, high level output voltage	I_{OL} = 11 mA	—	0.1$V_{DD_HV_IO}$	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –11 mA	0.8$V_{DD_HV_IO}$	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–95	—	µA
I_{PD}	P	Equivalent pull-down current	V_{IN} = V_{IH}	—	95	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	—	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	—	0.5	µA
V_{ILR}	D	Minimum $\overline{\text{RESET}}$, low level input voltage	—	–0.4[2]	—	V
V_{ILR}	P	Maximum $\overline{\text{RESET}}$, low level input voltage	—	—	0.35 $V_{DD\_HV\_IO}$	V
V_{IHR}	P	Minimum $\overline{\text{RESET}}$, high level input voltage	—	0.65 $V_{DD\_HV\_IO}$	—	V
V_{IHR}	D	Maximum $\overline{\text{RESET}}$, high level input voltage	—	—	$V_{DD\_HV\_IO}$ + 0.4[2]	V
V_{HYSR}	D	$\overline{\text{RESET}}$, Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IO}$	—	V
V_{OLR}	D	$\overline{\text{RESET}}$, low level output voltage	I_{OL} = 0.5 mA	—	0.1$V_{DD_HV_IO}$	V
I_{PU}	D	$\overline{\text{RESET}}$, equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	
C_{IN}	D	Input capacitance	—	—	10	pF

1 These specifications are design targets and subject to change per device characterization.

2 “SR” parameter values must not exceed the absolute maximum ratings shown in Table 6.

Table 19. PLLMRFM electrical specifications[1] (V_{DDPLL} = 3.0 V to 3.6 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
f_{UL}	D	Frequency un-LOCK range	—	–18	18	% f_{sys}
f_{CS} f_{DS}	D	Modulation Depth	Center spread	±0.25	±4.0[11]	%f_{sys}
			Down Spread	–0.5	–8.0	
f_{MOD}	D	Modulation frequency[12]	—	—	100	kHz

1 All values given are initial design targets and subject to change.

2 Considering operation with PLL not bypassed.

3 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.

4 f_{VCO} self clock range is 20-150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.

5 This value is determined by the crystal manufacturer and board design.

6 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.

7 Proper PC board layout procedures must be followed to achieve specifications.

8 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).

9 This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.

10 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

11 This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).

12 Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.13 16 MHz RC oscillator electrical characteristics

Table 20. 16 MHz RC oscillator electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
f_{RC}	C	RC oscillator frequency	T_A = 25 °C	8.5	16	24	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation in temperature and supply with respect to f_{RC} at T_A = 55 °C in high-frequency configuration	—	–5	—	5	%
$\Delta_{RCMTRIM}$	T	Post Trim Accuracy: The variation of the PTF[1] from the 16 MHz oscillator	T_A = 25 °C	–2	—	2	%

1 PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature

be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (fc \times C_S)$, where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the Equation 4:

Eqn. 4

$$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

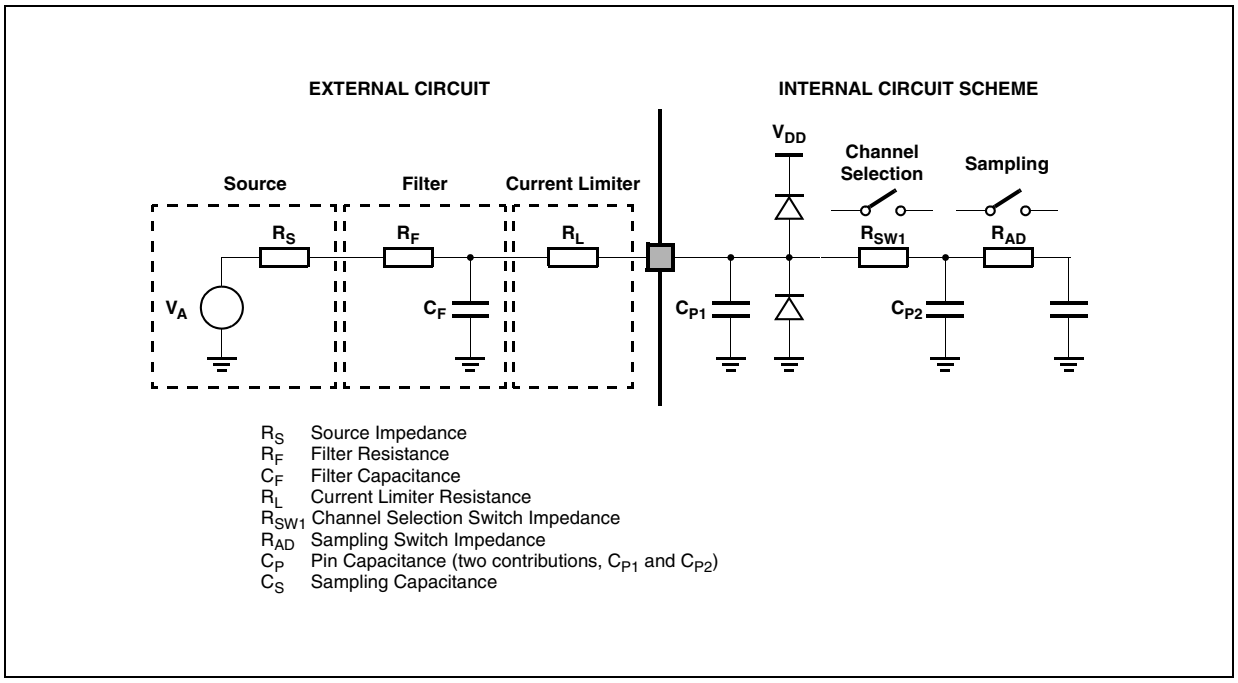

Figure 10. Input equivalent circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 10): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

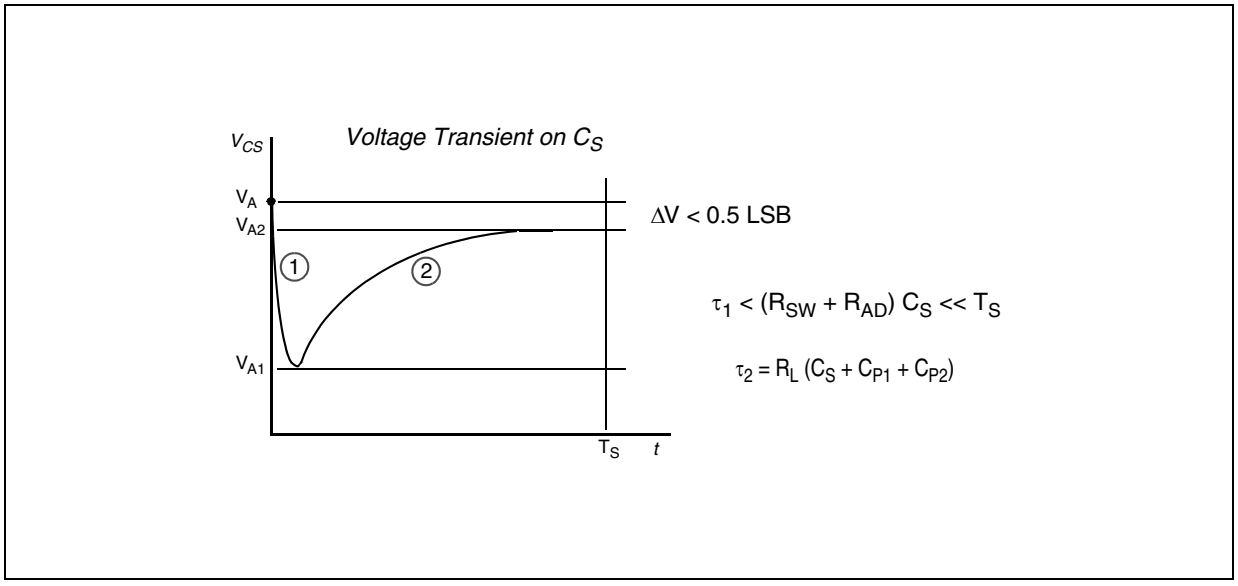

Figure 11. Transient behavior during sampling phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Eqn. 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

Eqn. 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

Eqn. 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Eqn. 12

$$C_F > 2048 \bullet C_S$$

1 V_{DD} = 3.3 V to 3.6 V, T_A = –40 to +125 °C, unless otherwise specified and analog input voltage from V_{AGND} to V_{AREF}

2 ADCClk clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.

3 During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.

4 This parameter does not include the sample time t_{ADC_S}, but only the time for determining the digital result and the time to load the result register with the conversion result.

5 20 MHz ADC clock. Specific prescaler is programmed on MC_PLL_CLK to provide 20 MHz clock to the ADC.

6 See Figure 10.

7 Does not include packaging and bonding capacitances

3.15 Temperature sensor electrical characteristics

Table 22. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					min	typical	max	
—	CC	C	Temperature monitoring range	—	–40	—	150	°C
—	CC	C	Sensitivity	—	—	5.14	—	mV/°C
—	CC	C	Accuracy	T_J = –40 to 25 °C	–10	—	10	°C
—	CC	C		T_J = –25 to 125 °C	–10	—	10	°C

3.16 Flash memory electrical characteristics

Table 23. Code flash program and erase specifications[1]

Symbol	Parameter	Min Value	Typical Value[2] (0 Cycles)	Initial Max[3] (100 Cycles)	Max[4] (100000 Cycles)	Unit
T_{DWPRG}	Double Word Program[5]	—	22	50	500	µs
T_{BKPRG}	Bank Program (512 KB)[5, 6]	—	1.45	1.65	33	s
T_{ER8K}	Sector Erase (8KB)	—	0.2	0.4	5.0	s
T_{ER16K}	Sector Erase (16KB)	—	0.3	0.5	5.0	s
T_{ER32K}	Sector Erase (32KB)	—	0.3	0.6	5.0	s
T_{ER64K}	Sector Erase (64KB)	—	0.6	0.9	5.0	s
T_{ER128K}	Sector Erase (128KB)	—	0.8	1.3	7.5	s
T_{ER512K}	Bank Erase (512KB)	—	4.8	7.6	55	s
T_{PABT}	Program Abort Latency	—	—	10	10	µs
T_{EABT}	Erase Abort Latency	—	—	30	30	µs

Table 23. Code flash program and erase specifications[1]

Symbol	Parameter	Min Value	Typical Value[2] (0 Cycles)	Initial Max[3] (100 Cycles)	Max[4] (100000 Cycles)	Unit
T_{EABT}	Erase Suspend Latency	—	—	30	30	µs
T_{EABT}	Erase Suspend Request Rate	10	—	—	—	ms
NER	Endurance (8KB, 16KB sectors) Endurance (32KB, 64KB sectors) Endurance (128KB sectors)	100 10 1	—	—	—	Kcycles
T_{DR}	Data Retention at 1K cycles Data Retention at 10K cycles Data Retention at 100K cycles	20 10 5	—	—	—	Years

1 TBC = To be confirmed

2 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

3 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

4 The maximum program & erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

5 Actual hardware programming times. This does not include software overhead.

6 Typical Bank programming time assumes that all cells are programmed in a single pulse. In reality some cells will require more than one pulse, adding a small overhead to total bank programming time (see Initial Max column).

Table 24. Data flash program and erase specifications[1]

Symbol	Parameter	Min Value	Typical Value[2] (0 Cycles)	Initial Max[3] (100 Cycles)	Max[4] (100000 Cycles)	Unit
T_{DWPRG}	Word Program[5]	—	30	TBC	TBC	µs
T_{BKPRG}	Bank Program (64 KB)[5, 6]	—	0.49	TBC	TBC	s
T_{ER16K}	Sector Erase (16KB)	—	0.7	TBC	TBC	s
T_{ER512K}	Bank Erase (64KB)	—	1.9	TBC	TBC	s
T_{PABT}	Program Abort Latency	—	—	12	12	µs
T_{EABT}	Erase Abort Latency	—	—	30	30	µs
T_{EABT}	Erase Suspend Latency	—	—	30	30	µs
T_{EABT}	Erase Suspend Request Rate	10	—	—	—	ms
NER	Endurance (16KB sectors)	100	—	—	—	K cycles
T_{DR}	Data Retention at 1K cycles Data Retention at 10K cycles Data Retention at 100K cycles	20 10 1	—	—	—	Years @85C

1 TBC = To be confirmed

2 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

Table 27. $\overline{\text{RESET}}$ electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	$V_{DD}+0.4$	V
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 3 mA,	—	—	$0.1V_{DD}$	V
T_{tr}	CC	D	Output transition time output pin[3] MEDIUM configuration	C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	12	ns
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	25	
				C_L = 100 pF, V_{DD} = 3.3 V ± 10%	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	500	—	—	ns
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%	10	—	150	µA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 C_L includes device and package capacitance (C_{PKG} < 5 pF).

3.18.3 Nexus and JTAG timing

Table 28. Nexus debug port timing[1]

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{MCYC}	CC	D	MCKO Cycle Time	2	—	8	t_{CYC}
2A	t_{MCYCP}	CC	D	MCKO cycle period	15	—	—	ns
2B	t_{MDC}	CC	D	MCKO duty cycle	48	—	52	%
3	t_{MDOV}	CC	D	MCKO low to MDO data valid[2]	–0.1	—	0.22	t_{MCYC}
4	t_{MSEOV}	CC	D	MCKO low to $\overline{\text{MSEO}}$ data valid[2]	–0.1	—	0.22	t_{MCYC}
5	t_{EVTOV}	CC	D	MCKO low to $\overline{\text{EVTO}}$ data valid[2]	–0.1	—	0.22	t_{MCYC}
6	t_{TCYC}	CC	D	TCK cycle time	50	—	—	ns
7	t_{TDC}	CC	D	TCK Duty Cycle	40	—	60	%

3.18.8 DSPI timing

Table 32. DSPI timing

No.	Symbol		C	Parameter	Conditions	Min	Max	Unit
1	t_{SCK}	CC	D	DSPI cycle time	Master (MTFE = 0)	62.5	—	ns
					Slave (MTFE = 0)	128	—	
					Master (MTFE = 1,CPHA=1)	31.25	—	
2	t_{CSC}	CC	D	CS to SCK delay	—	16	—	ns
3	t_{ASC}	CC	D	After SCK delay	—	16	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	—	0.4 * t_{SCK}	0.6 * t_{SCK}	ns
5	t_A	CC	D	Slave access time	$\overline{SS}$ active to SOUT valid	—	40	ns
6	t_{DIS}	CC	D	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT High-Z or invalid	—	10	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time	—	13	—	ns
9	t_{SUI}	CC	D	Data setup time for inputs	Master (MTFE = 0)	12	—	ns
					Slave	2	—	
					Master (MTFE = 1, CPHA = 0)	NA[1]		
					Master (MTFE = 1, CPHA = 1)	12	—	
10	t_{HI}	CC	D	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	NA[1]		
					Master (MTFE = 1, CPHA = 1)	–5	—	
11	t_{SUO}	CC	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	4	ns
					Slave	—	33	
					Master (MTFE = 1, CPHA = 0)	NA[1]		
					Master (MTFE = 1, CPHA = 1)	—	11	
12	t_{HO}	CC	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
					Slave	6	—	
					Master (MTFE = 1, CPHA = 0)	NA[1]		
					Master (MTFE = 1, CPHA = 1)	–2	—	

[1] This mode is not feasible at 32 MHz.

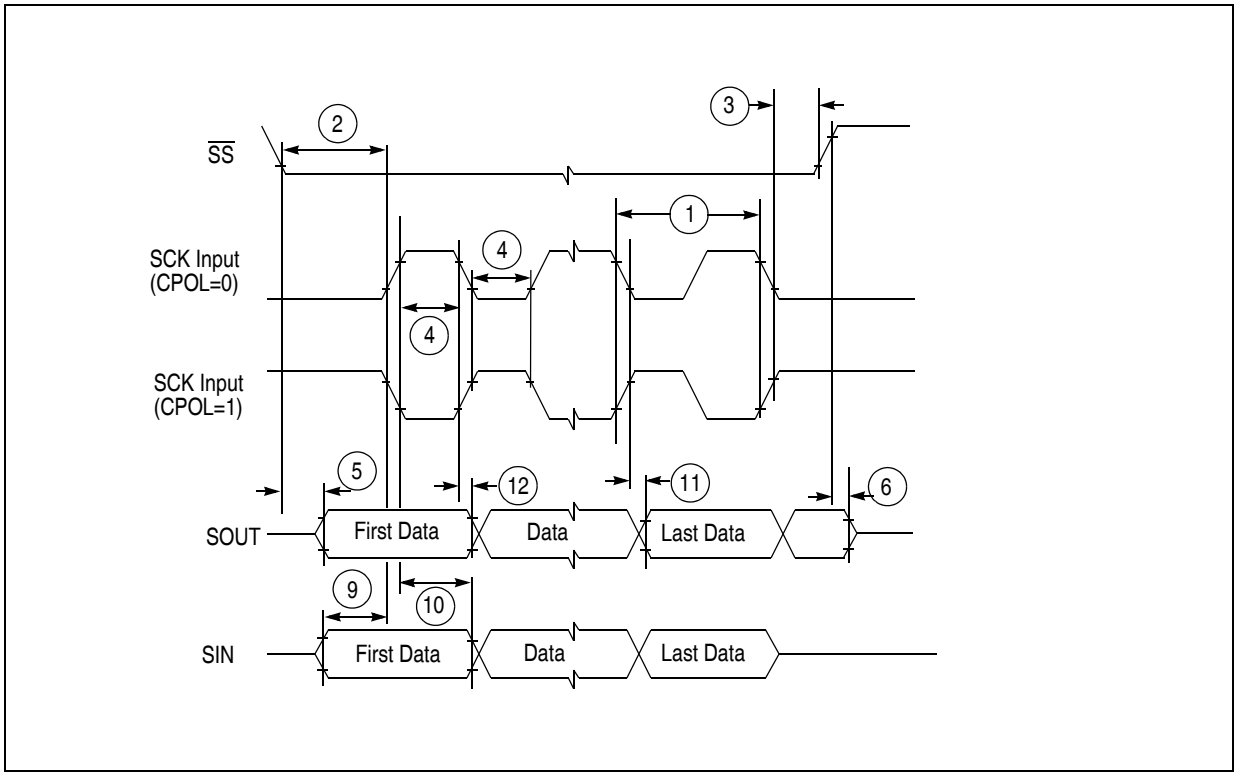

Figure 24. DSPI classic SPI timing — Slave, CPHA = 0

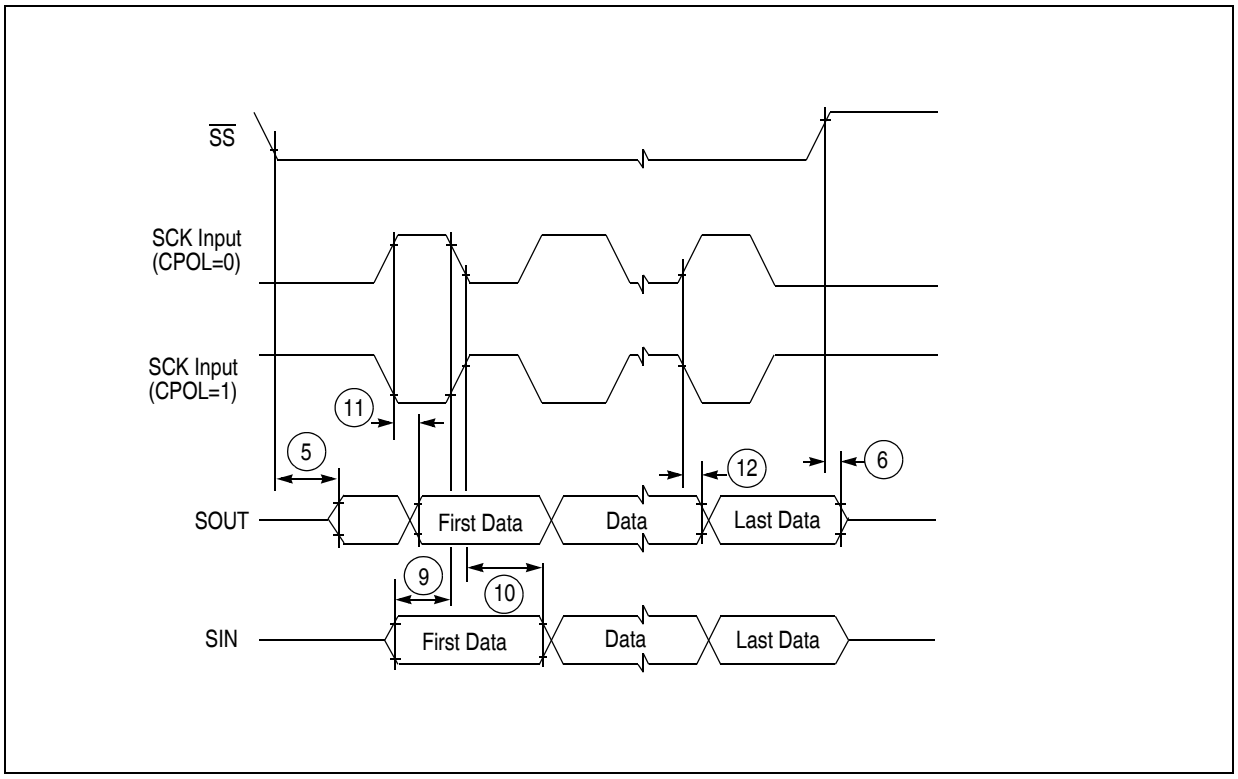

Figure 25. DSPI classic SPI timing — Slave, CPHA = 1

3.18.10 Fast ethernet interface

MII signals use CMOS signal levels compatible with devices operating at either 5.0 V or 3.3 V. Signals are not TTL compatible. They follow the CMOS electrical characteristics.

3.18.10.1 MII receive signal timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the RX_CLK frequency.

Table 34. MII receive signal timing

No.	Parameter	Min	Max	Unit
1	Rx Clock Period	40	—	ns
2	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
3	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
4	Rx Clock Duty Cycle	40	60	%

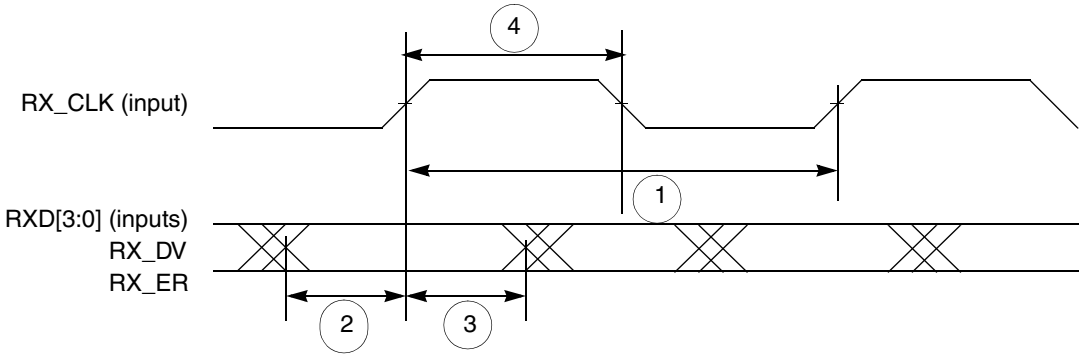

Figure 32. MII receive signal timing diagram

3.18.10.2 MII transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the Ethernet chapter for details of this option and how to enable it.

Table 35. MII transmit signal timing[1]

No.	Parameter	Min	Max	Unit
5	TX Clock Period	40	—	ns
6	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
7	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
8	TX Clock Duty Cycle	40	60	%

[1] Output pads configured with SRC = 0b11.

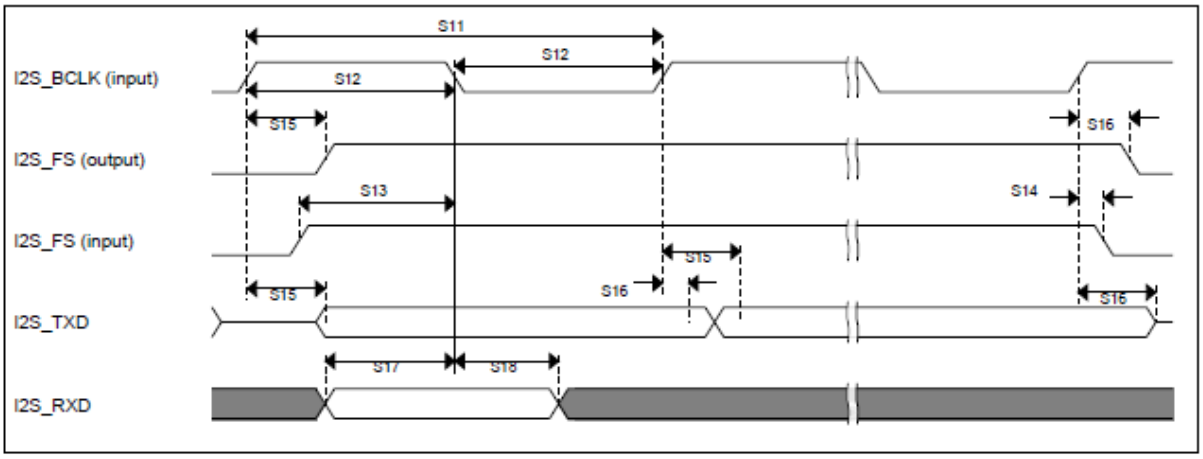

Figure 38. SAI timing slave modes

4.2 64 LQFP mechanical outline drawing

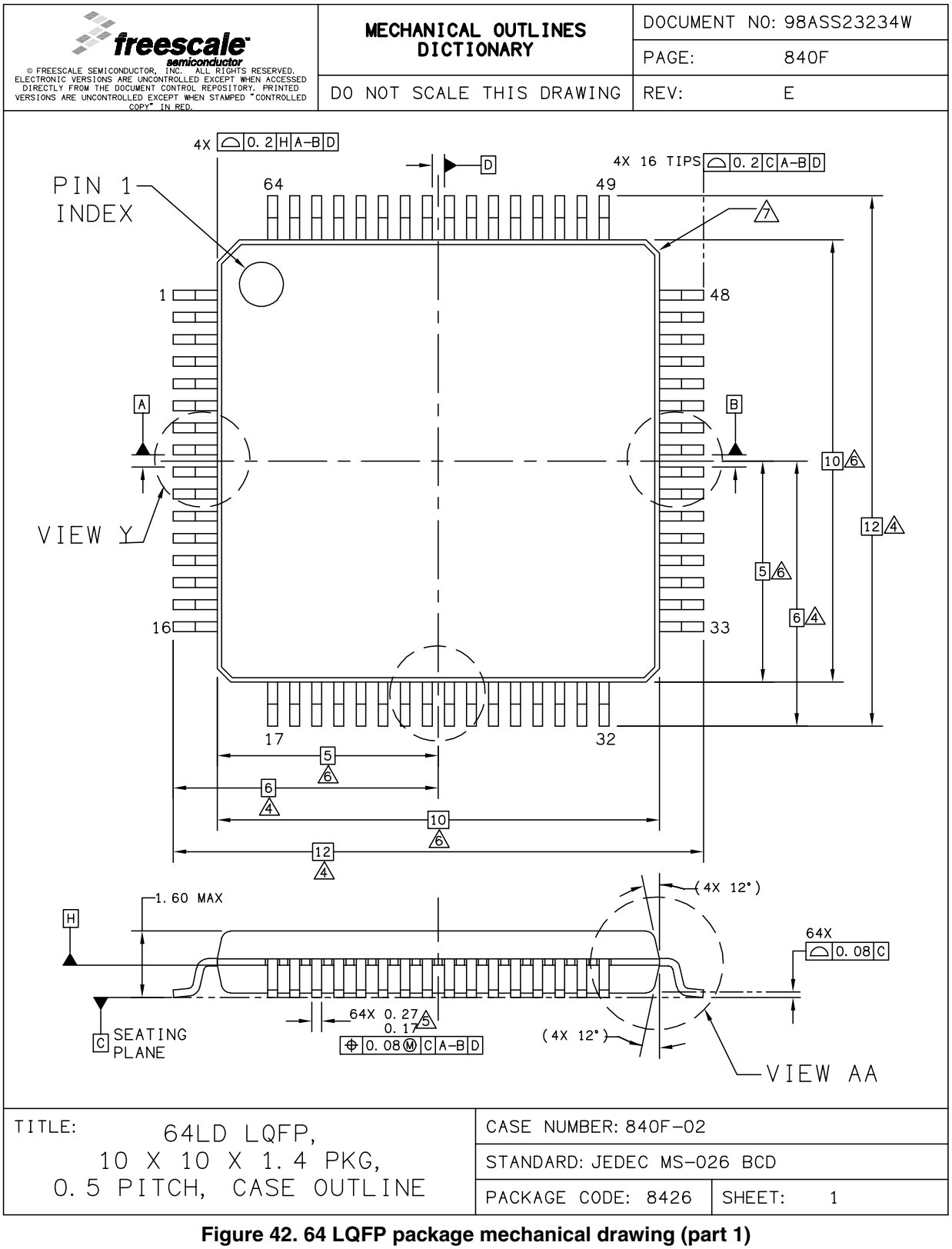

Figure 42. 64 LQFP package mechanical drawing (part 1)