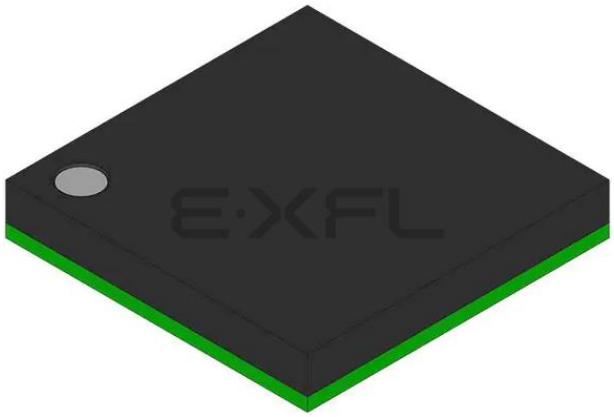


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | CANbus, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG |
| Peripherals | DMA, I²S, LCD, LVD, POR, PWM, WDT |
| Number of I/O | 52 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 17x16b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 81-LBGA |
| Supplier Device Package | 81-MAPBGA (10x10) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mk40dx256zvmb10 |

# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK40 and MK40 .

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

## 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|---|---|---|
| Q | Qualification status | • M = Fully qualified, general market flow<br>• P = Prequalification |
| K## | Kinetis family | • K40 |
| A | Key attribute | • D = Cortex-M4 w/ DSP<br>• F = Cortex-M4 w/ DSP and FPU |
| M | Flash memory type | • N = Program flash only<br>• X = Program flash and FlexMemory |

*Table continues on the next page...*

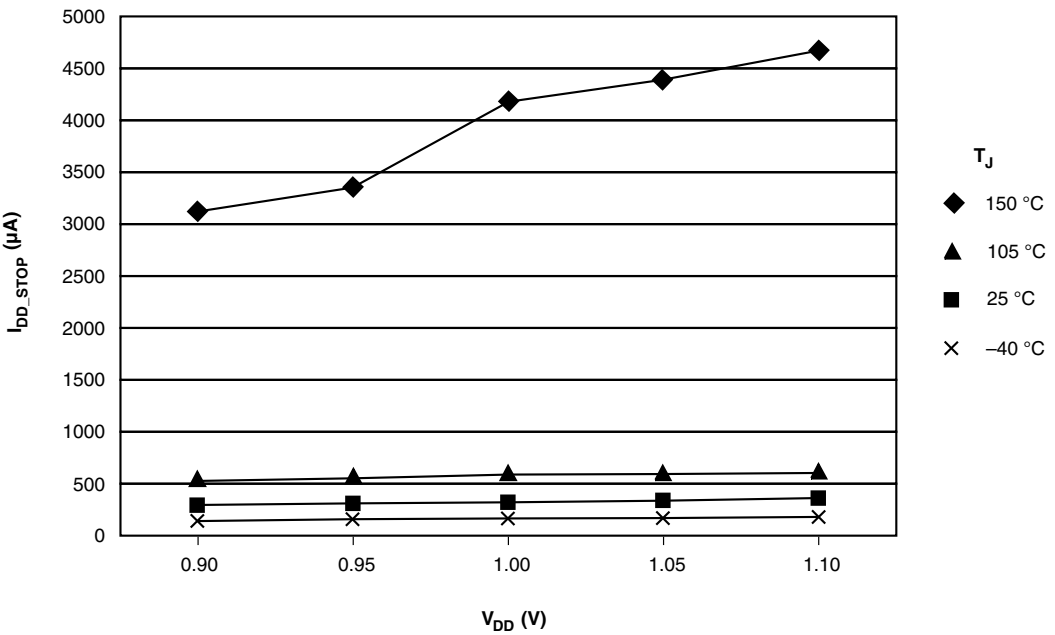
### 3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{WP}$ | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | µA |

### 3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:




## 3.9 Typical value conditions

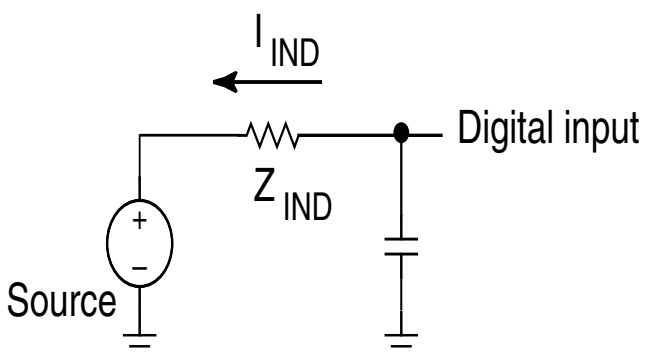
Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient temperature | 25 | °C |
| $V_{DD}$ | 3.3 V supply voltage | 3.3 | V |

**Table 4. Voltage and current operating behaviors (continued)**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{IND}$ | Input leakage current, digital pins<br>• $V_{DD} < V_{IN} < 5.5$ V | —<br>— | <br>1 | <br>50 | <br>μA | 4, 5 |
| $Z_{IND}$ | Input impedance examples, digital pins<br>• $V_{DD} = 3.6$ V<br>• $V_{DD} = 3.0$ V<br>• $V_{DD} = 2.5$ V<br>• $V_{DD} = 1.7$ V | <br>—<br>—<br>—<br>— | <br>—<br>—<br>—<br>— | <br>48<br>55<br>57<br>85 | <br>kΩ<br>kΩ<br>kΩ<br>kΩ | 4, 7 |
| $R_{PU}$ | Internal pullup resistors | 20 | 35 | 50 | kΩ | 8 |
| $R_{PD}$ | Internal pulldown resistors | 20 | 35 | 50 | kΩ | 9 |

1. Typical values characterized at 25°C and VDD = 3.6 V unless otherwise noted.
2. Open drain outputs must be pulled to $V_{DD}$.
3. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
4. Digital pins have an associated GPIO port function and have 5V tolerant inputs, except EXTAL and XTAL.
5. Internal pull-up/pull-down resistors disabled.
6. Characterized, not tested in production.
7. Examples calculated using $V_{IL}$ relation, $V_{DD}$, and max $I_{IND}$: $Z_{IND}=V_{IL}/I_{IND}$. This is the impedance needed to pull a high signal to a level below $V_{IL}$ due to leakage when $V_{IL} < V_{IN} < V_{DD}$. These examples assume signal source low = 0 V.
8. Measured at $V_{DD}$ supply voltage = $V_{DD}$ min and Vinput = $V_{SS}$
9. Measured at $V_{DD}$ supply voltage = $V_{DD}$ min and Vinput = $V_{DD}$




## 5.2.4 Power mode transition operating behaviors

All specifications except $t_{POR}$, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

## Table 6. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DD\_VLPR}$ | Very-low-power run mode current at 3.0 V — all peripheral clocks enabled | — | N/A | — | mA | 7 |
| $I_{DD\_VLPW}$ | Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled | — | N/A | — | mA | 8 |
| $I_{DD\_STOP}$ | Stop mode current at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 0.59 | 1.4 | mA | |
| | • @ 70°C | — | 2.26 | 7.9 | mA | |
| | • @ 105°C | — | 5.94 | 19.2 | mA | |
| $I_{DD\_VLPS}$ | Very-low-power stop mode current at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 93 | 435 | µA | |
| | • @ 70°C | — | 520 | 2000 | µA | |
| | • @ 105°C | — | 1350 | 4000 | µA | |
| $I_{DD\_LLS}$ | Low leakage stop mode current at 3.0 V | | | | | 9 |
| | • @ –40 to 25°C | — | 4.8 | 20 | µA | |
| | • @ 70°C | — | 28 | 68 | µA | |
| | • @ 105°C | — | 126 | 270 | µA | |
| $I_{DD\_VLLS3}$ | Very low-leakage stop mode 3 current at 3.0 V | | | | | 9 |
| | • @ –40 to 25°C | — | 3.1 | 8.9 | µA | |
| | • @ 70°C | — | 17 | 35 | µA | |
| | • @ 105°C | — | 82 | 148 | µA | |
| $I_{DD\_VLLS2}$ | Very low-leakage stop mode 2 current at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 2.2 | 5.4 | µA | |
| | • @ 70°C | — | 7.1 | 12.5 | µA | |
| | • @ 105°C | — | 41 | 125 | µA | |
| $I_{DD\_VLLS1}$ | Very low-leakage stop mode 1 current at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 2.1 | 7.6 | µA | |
| | • @ 70°C | — | 6.2 | 13.5 | µA | |
| | • @ 105°C | — | 30 | 46 | µA | |
| $I_{DD\_VBAT}$ | Average current with RTC and 32kHz disabled at 3.0 V | | | | | |
| | • @ –40 to 25°C | — | 0.33 | 0.39 | µA | |
| | • @ 70°C | — | 0.60 | 0.78 | µA | |
| | • @ 105°C | — | 1.97 | 2.9 | µA | |

*Table continues on the next page...*

## 5.4.1 Thermal operating requirements

**Table 11. Thermal operating requirements**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_J$ | Die junction temperature | –40 | 125 | °C |
| $T_A$ | Ambient temperature | –40 | 105 | °C |

## 5.4.2 Thermal attributes

| Board type | Symbol | Description | 81 MAPBGA | 80 LQFP | Unit | Notes |
|---|---|---|---|---|---|---|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 65 | 50 | °C/W | 1 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 36 | 35 | °C/W | 1 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 52 | 39 | °C/W | 1 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 31 | 29 | °C/W | 1 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 17 | 19 | °C/W | 2 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 13 | 8 | °C/W | 3 |
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top outside center (natural convection) | 3 | 2 | °C/W | 4 |

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.

**Table 14. JTAG full voltage range electricals (continued)**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| J3 | TCLK clock pulse width | | | |
| | • Boundary Scan | 50 | — | ns |
| | • JTAG and CJTAG | 25 | — | ns |
| | • Serial Wire Debug | 12.5 | — | ns |
| J4 | TCLK rise and fall times | — | 3 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | 20 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 0 | — | ns |
| J7 | TCLK low to boundary scan output data valid | — | 25 | ns |
| J8 | TCLK low to boundary scan output high-Z | — | 25 | ns |
| J9 | TMS, TDI input data setup time to TCLK rise | 8 | — | ns |
| J10 | TMS, TDI input data hold time after TCLK rise | 1.4 | — | ns |
| J11 | TCLK low to TDO data valid | — | 22.1 | ns |
| J12 | TCLK low to TDO high-Z | — | 22.1 | ns |
| J13 | $\overline{\text{TRST}}$ assert time | 100 | — | ns |
| J14 | $\overline{\text{TRST}}$ setup time (negation) to TCLK high | 8 | — | ns |

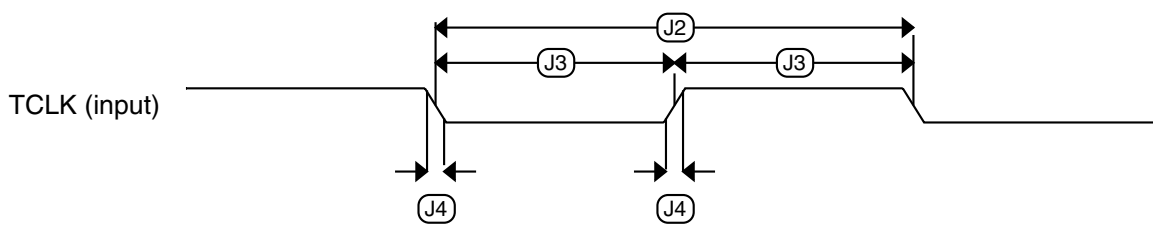



**Figure 5. Test clock input timing**

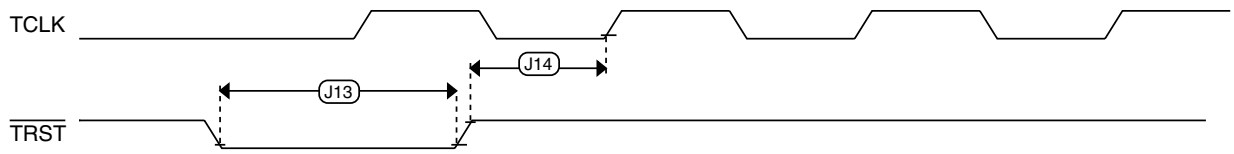



**Figure 8. $\overline{\text{TRST}}$ timing**

## 6.2 System modules

There are no specifications necessary for the device's system modules.

## 6.3 Clock modules

### 6.3.1 MCG specifications

**Table 15. MCG specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{ints\_ft}$ | Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C | — | 32.768 | — | kHz | |
| $f_{ints\_t}$ | Internal reference frequency (slow clock) — user trimmed — over fixed voltage and temperature range of 0–70°C | 31.25 | — | 38.2 | kHz | |
| $\Delta_{fdco\_res\_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM | — | ± 0.3 | ± 0.6 | $\%f_{dco}$ | 1 |
| $\Delta f_{dco\_t}$ | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C | — | ± 1.5 | ± 4.5 | $\%f_{dco}$ | 1 |
| $f_{intf\_ft}$ | Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C | — | 4 | — | MHz | |
| $f_{intf\_t}$ | Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C | 3 | — | 5 | MHz | |
| $f_{loc\_low}$ | Loss of external clock minimum frequency — RANGE = 00 | (3/5) x $f_{ints\_t}$ | — | — | kHz | |
| $f_{loc\_high}$ | Loss of external clock minimum frequency — RANGE = 01, 10, or 11 | (16/5) x $f_{ints\_t}$ | — | — | kHz | |
| FLL | | | | | | |
| $f_{fll\_ref}$ | FLL reference frequency range | 31.25 | — | 39.0625 | kHz | |

*Table continues on the next page...*

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ($\Delta f_{dco\_t}$) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## 6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

### 6.3.2.1 Oscillator DC electrical specifications

**Table 16. Oscillator DC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V | |
| $I_{DDOSC}$ | Supply current — low-power mode (HGO=0) | | | | | 1 |
| | • 32 kHz | — | 500 | — | nA | |
| | • 4 MHz | — | 200 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 300 | — | µA | |
| | • 16 MHz | — | 950 | — | µA | |
| | • 24 MHz | — | 1.2 | — | mA | |
| | • 32 MHz | — | 1.5 | — | mA | |
| $I_{DDOSC}$ | Supply current — high gain mode (HGO=1) | | | | | 1 |
| | • 32 kHz | — | 25 | — | µA | |
| | • 4 MHz | — | 400 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 500 | — | µA | |
| | • 16 MHz | — | 2.5 | — | mA | |
| | • 24 MHz | — | 3 | — | mA | |
| | • 32 MHz | — | 4 | — | mA | |
| $C_x$ | EXTAL load capacitance | — | — | — | | 2, 3 |
| $C_y$ | XTAL load capacitance | — | — | — | | 2, 3 |

*Table continues on the next page...*

### 6.6.1.1 16-bit ADC operating conditions

**Table 25. 16-bit ADC operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $\Delta V_{DDA}$ | Supply voltage | Delta to $V_{DD}$ ($V_{DD}$ - $V_{DDA}$) | -100 | 0 | +100 | mV | 2 |
| $\Delta V_{SSA}$ | Ground voltage | Delta to $V_{SS}$ ($V_{SS}$ - $V_{SSA}$) | -100 | 0 | +100 | mV | 2 |
| $V_{REFH}$ | ADC reference voltage high | | 1.13 | $V_{DDA}$ | $V_{DDA}$ | V | |
| $V_{REFL}$ | ADC reference voltage low | | $V_{SSA}$ | $V_{SSA}$ | $V_{SSA}$ | V | |
| $V_{ADIN}$ | Input voltage | • 16-bit differential mode<br>• All other modes | VREFL<br>VREFL | —<br>— | 31/32 * VREFH<br>VREFH | V | |
| $C_{ADIN}$ | Input capacitance | • 16-bit mode<br>• 8-bit / 10-bit / 12-bit modes | —<br>— | 8<br>4 | 10<br>5 | pF | |
| $R_{ADIN}$ | Input resistance | | — | 2 | 5 | kΩ | |
| $R_{AS}$ | Analog source resistance | 13-bit / 12-bit modes<br>$f_{ADCK}$ < 4 MHz | — | — | 5 | kΩ | 3 |
| $f_{ADCK}$ | ADC conversion clock frequency | ≤ 13-bit mode | 1.0 | — | 18.0 | MHz | 4 |
| $f_{ADCK}$ | ADC conversion clock frequency | 16-bit mode | 2.0 | — | 12.0 | MHz | 4 |
| $C_{rate}$ | ADC conversion rate | ≤ 13-bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 20.000 | — | 818.330 | Ksps | 5 |
| $C_{rate}$ | ADC conversion rate | 16-bit mode<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 37.037 | — | 461.467 | Ksps | 5 |

1. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25 °C, $f_{ADCK}$ = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The $R_{AS}/C_{AS}$ time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, the ADHSC bit must be set and the ADLPC bit must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

### 6.6.1.3 16-bit ADC with PGA operating conditions

**Table 27. 16-bit ADC with PGA operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $V_{REFPGA}$ | PGA ref voltage | | VREF_OUT | VREF_OUT | VREF_OUT | V | 2, 3 |
| $V_{ADIN}$ | Input voltage | | $V_{SSA}$ | — | $V_{DDA}$ | V | |
| $V_{CM}$ | Input Common Mode range | | $V_{SSA}$ | — | $V_{DDA}$ | V | |
| $R_{PGAD}$ | Differential input impedance | Gain = 1, 2, 4, 8 | — | 128 | — | kΩ | IN+ to IN-[4] |
| | | Gain = 16, 32 | — | 64 | — | | |
| | | Gain = 64 | — | 32 | — | | |
| $R_{AS}$ | Analog source resistance | | — | 100 | — | Ω | 5 |
| $T_S$ | ADC sampling time | | 1.25 | — | — | µs | 6 |
| $C_{rate}$ | ADC conversion rate | ≤ 13 bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled<br>Peripheral clock = 50 MHz | 18.484 | — | 450 | Ksps | 7 |
| | | 16 bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled<br>Peripheral clock = 50 MHz | 37.037 | — | 250 | Ksps | 8 |

1. Typical values assume $V_{DDA}$ = 3.0 V, Temp = 25°C, $f_{ADCK}$ = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. ADC must be configured to use the internal voltage reference (VREF_OUT)
3. PGA reference is internally connected to the VREF_OUT pin. If the user wishes to drive VREF_OUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
4. For single ended configurations the input impedance of the driven input is $R_{PGAD}/2$
5. The analog source resistance ($R_{AS}$), external to MCU, should be kept as minimum as possible. Increased $R_{AS}$ causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
6. The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25µs time should be allowed for $F_{in}$=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.
7. ADC clock = 18 MHz, ADLSMP = 1, ADLST = 00, ADHSC = 1
8. ADC clock = 12 MHz, ADLSMP = 1, ADLST = 01, ADHSC = 1

### 6.6.1.4 16-bit ADC with PGA characteristics

**Table 28. 16-bit ADC with PGA characteristics**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $I_{DDA\_PGA}$ | Supply current | Low power (ADC_PGA[PGALPb]=0) | — | 420 | 644 | µA | 2 |
| $I_{DC\_PGA}$ | Input DC current | | $\frac{2}{R_{PGAD}}\left(\frac{(V_{REFPGA}\times 0.583)-V_{CM}}{(Gain+1)}\right)$ | | | A | 3 |
| | | Gain =1, $V_{REFPGA}$=1.2V, $V_{CM}$=0.5V | — | 1.54 | — | µA | |
| | | Gain =64, $V_{REFPGA}$=1.2V, $V_{CM}$=0.1V | — | 0.57 | — | µA | |
| G | Gain[4] | • PGAG=0 | 0.95 | 1 | 1.05 | | $R_{AS} < 100\Omega$ |
| | | • PGAG=1 | 1.9 | 2 | 2.1 | | |
| | | • PGAG=2 | 3.8 | 4 | 4.2 | | |
| | | • PGAG=3 | 7.6 | 8 | 8.4 | | |
| | | • PGAG=4 | 15.2 | 16 | 16.6 | | |
| | | • PGAG=5 | 30.0 | 31.6 | 33.2 | | |
| | | • PGAG=6 | 58.8 | 63.3 | 67.8 | | |
| BW | Input signal bandwidth | • 16-bit modes | — | — | 4 | kHz | |
| | | • < 16-bit modes | — | — | 40 | kHz | |
| PSRR | Power supply rejection ratio | Gain=1 | — | -84 | — | dB | $V_{DDA}$= 3V ±100mV, $f_{VDDA}$= 50Hz, 60Hz |
| CMRR | Common mode rejection ratio | • Gain=1 | — | -84 | — | dB | $V_{CM}$= 500mVpp, $f_{VCM}$= 50Hz, 100Hz |
| | | • Gain=64 | — | -85 | — | dB | |
| $V_{OFS}$ | Input offset voltage | | — | 0.2 | — | mV | Output offset = $V_{OFS}$*(Gain+1) |
| $T_{GSW}$ | Gain switching settling time | | — | — | 10 | µs | 5 |
| $E_{IL}$ | Input leakage error | All modes | $I_{In} \times R_{AS}$ | | | mV | $I_{In}$ = leakage current (refer to the MCU's voltage and current operating ratings) |
| $V_{PP,DIFF}$ | Maximum differential input signal swing | | $\left(\frac{(\min(V_X, V_{DDA}-V_X)-0.2)\times 4}{Gain}\right)$ where $V_X = V_{REFPGA} \times 0.583$ | | | V | 6 |
| SNR | Signal-to-noise ratio | • Gain=1 | 80 | 90 | — | dB | 16-bit differential mode, Average=32 |
| | | • Gain=64 | 52 | 66 | — | dB | |

*Table continues on the next page...*

### 6.6.3.2 12-bit DAC operating behaviors

**Table 31. 12-bit DAC operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA\_DACLP}$ | Supply current — low-power mode | — | — | 150 | µA | |
| $I_{DDA\_DACHP}$ | Supply current — high-speed mode | — | — | 700 | µA | |
| $t_{DACLP}$ | Full-scale settling time (0x080 to 0xF7F) — low-power mode | — | 100 | 200 | µs | 1 |
| $t_{DACHP}$ | Full-scale settling time (0x080 to 0xF7F) — high-power mode | — | 15 | 30 | µs | 1 |
| $t_{CCDACLP}$ | Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode | — | 0.7 | 1 | µs | 1 |
| $V_{dacoutl}$ | DAC output voltage range low — high-speed mode, no load, DAC set to 0x000 | — | — | 100 | mV | |
| $V_{dacouth}$ | DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF | $V_{DACR}$ −100 | — | $V_{DACR}$ | mV | |
| INL | Integral non-linearity error — high speed mode | — | — | ±8 | LSB | 2 |
| DNL | Differential non-linearity error — $V_{DACR}$ > 2 V | — | — | ±1 | LSB | 3 |
| DNL | Differential non-linearity error — $V_{DACR}$ = VREF_OUT | — | — | ±1 | LSB | 4 |
| $V_{OFFSET}$ | Offset error | — | ±0.4 | ±0.8 | %FSR | 5 |
| $E_G$ | Gain error | — | ±0.1 | ±0.6 | %FSR | 5 |
| PSRR | Power supply rejection ratio, $V_{DDA}$ ≥ 2.4 V | 60 | — | 90 | dB | |
| $T_{CO}$ | Temperature coefficient offset voltage | — | 3.7 | — | µV/C | 6 |
| $T_{GE}$ | Temperature coefficient gain error | — | 0.000421 | — | %FSR/C | |
| Rop | Output resistance load = 3 kΩ | — | — | 250 | Ω | |
| SR | Slew rate -80h→ F7Fh→ 80h | | | | V/µs | |
| | • High power ($SP_{HP}$) | 1.2 | 1.7 | — | | |
| | • Low power ($SP_{LP}$) | 0.05 | 0.12 | — | | |
| CT | Channel to channel cross talk | — | — | -80 | dB | |
| BW | 3dB bandwidth | | | | kHz | |
| | • High power ($SP_{HP}$) | 550 | — | — | | |
| | • Low power ($SP_{LP}$) | 40 | — | — | | |

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV
3. The DNL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV
4. The DNL is measured for 0 + 100 mV to $V_{DACR}$ −100 mV with $V_{DDA}$ > 2.4 V
5. Calculated by a best fit curve from $V_{SS}$ + 100 mV to $V_{DACR}$ − 100 mV
6. $V_{DDA}$ = 3.0 V, reference select set for $V_{DDA}$ (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

**Table 42. I²C timing (continued)**

| Characteristic | Symbol | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| Fall time of SDA and SCL signals | $t_f$ | — | 300 | 20 +0.1$C_b$[5] | 300 | ns |
| Set-up time for STOP condition | $t_{SU}$; STO | 4 | — | 0.6 | — | µs |
| Bus free time between STOP and START condition | $t_{BUF}$ | 4.7 | — | 1.3 | — | µs |
| Pulse width of spikes that must be suppressed by the input filter | $t_{SP}$ | N/A | N/A | 0 | 50 | ns |

1. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
3. Input signal Slew = 10ns and Output Load = 50pf
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I²C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.
6. $C_b$ = total capacitance of the one bus line in pF.

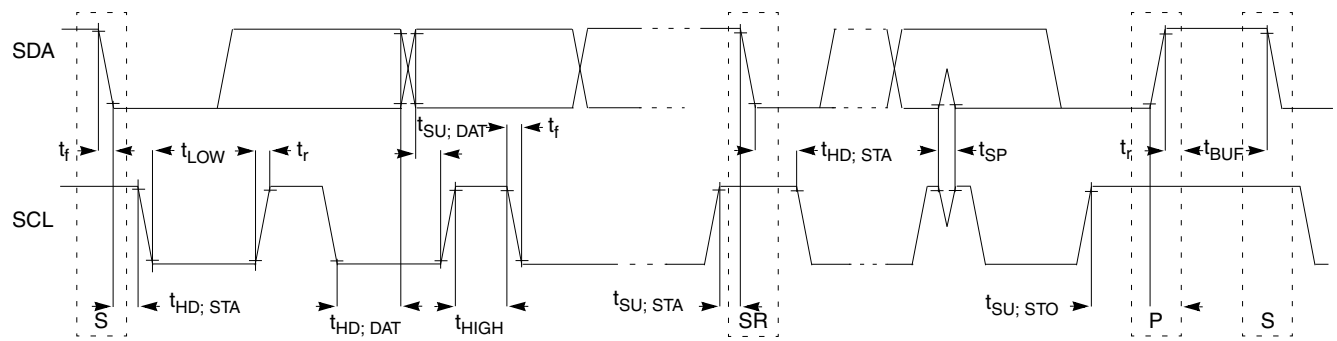



**Figure 21. Timing definition for fast and standard mode devices on the I²C bus**

## 6.8.8 UART switching specifications

See General switching specifications.

## 6.8.9 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

**Table 43. SDHC switching specifications**

| Num | Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|---|
| | **Card input clock** | | | | |
| SD1 | fpp | Clock frequency (low speed) | 0 | 400 | kHz |
| | fpp | Clock frequency (SD\SDIO full speed\high speed) | 0 | 25\50 | MHz |
| | fpp | Clock frequency (MMC full speed\high speed) | 0 | 20\50 | MHz |
| | $f_{OD}$ | Clock frequency (identification mode) | 0 | 400 | kHz |
| SD2 | $t_{WL}$ | Clock low time | 7 | — | ns |
| SD3 | $t_{WH}$ | Clock high time | 7 | — | ns |
| SD4 | $t_{TLH}$ | Clock rise time | — | 3 | ns |
| SD5 | $t_{THL}$ | Clock fall time | — | 3 | ns |
| | **SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)** | | | | |
| SD6 | $t_{OD}$ | SDHC output delay (output valid) | -5 | 8.3 | ns |
| | **SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)** | | | | |
| SD7 | $t_{ISU}$ | SDHC input setup time | 5 | — | ns |
| SD8 | $t_{IH}$ | SDHC input hold time | 0 | — | ns |

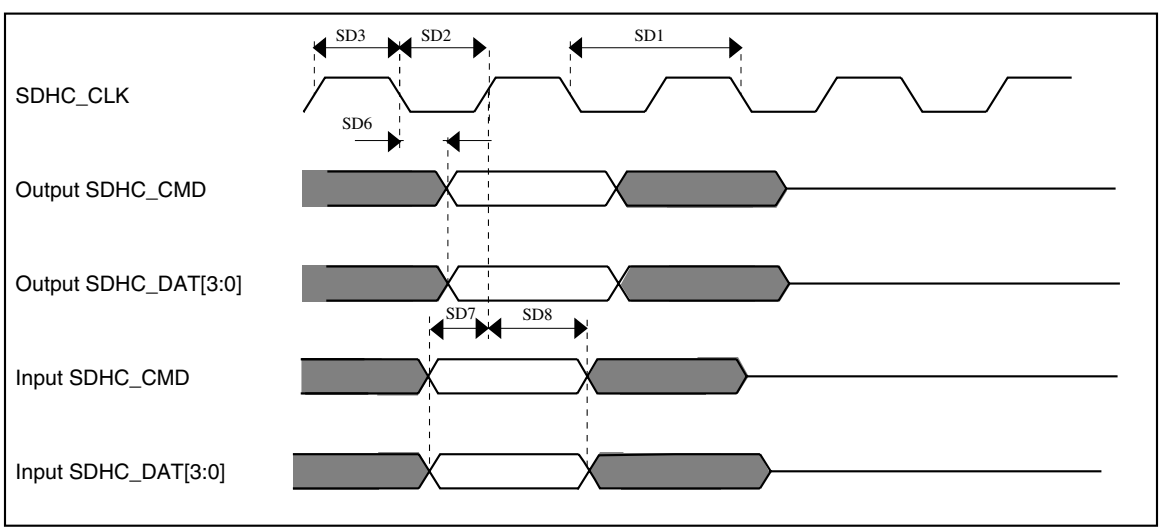



**Figure 22. SDHC timing**

## 6.8.10 I²S switching specifications

This section provides the AC timings for the I²S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S_BCLK) and/or the frame sync (I2S_FS) shown in the figures below.

**Table 44. I²S master mode timing (limited voltage range)**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 2 x $t_{SYS}$ | | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_BCLK cycle time | 5 x $t_{SYS}$ | — | ns |
| S4 | I2S_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_BCLK to I2S_FS output valid | — | 15 | ns |
| S6 | I2S_BCLK to I2S_FS output invalid | -2.5 | — | ns |
| S7 | I2S_BCLK to I2S_TXD valid | — | 15 | ns |
| S8 | I2S_BCLK to I2S_TXD invalid | -3 | — | ns |
| S9 | I2S_RXD/I2S_FS input setup before I2S_BCLK | 20 | — | ns |
| S10 | I2S_RXD/I2S_FS input hold after I2S_BCLK | 0 | — | ns |

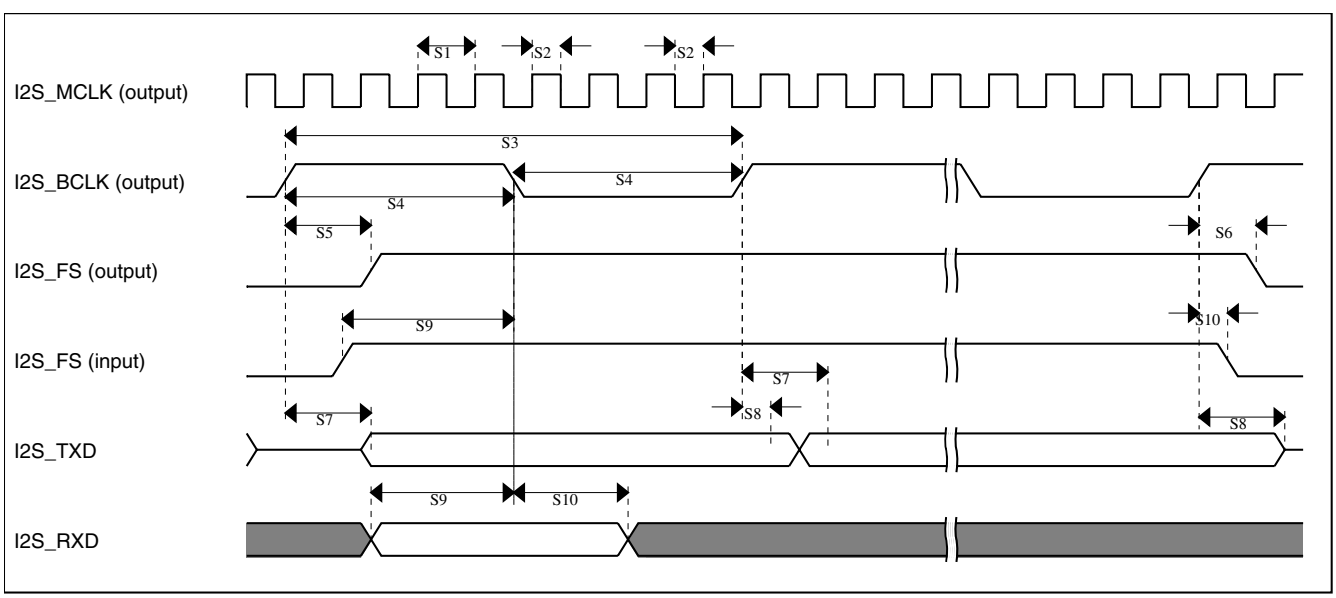



**Figure 23. I²S timing — master mode**

## 8.1 K40 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

**NOTE**

The 81-pin ballmap assignments are currently being developed. The • in the entries in this package column indicate which signals are present on the package.

| 81 MAP BGA | 80 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E4 | 1 | PTE0 | ADC1_SE4a | ADC1_SE4a | PTE0 | SPI1_PCS1 | UART1_TX | SDHC0_D1 | | I2C1_SDA | | |
| E3 | 2 | PTE1/ LLWU_P0 | ADC1_SE5a | ADC1_SE5a | PTE1/ LLWU_P0 | SPI1_SOUT | UART1_RX | SDHC0_D0 | | I2C1_SCL | | |
| E2 | 3 | PTE2/ LLWU_P1 | ADC1_SE6a | ADC1_SE6a | PTE2/ LLWU_P1 | SPI1_SCK | UART1_CTS_ b | SDHC0_DCLK | | | | |
| F4 | 4 | PTE3 | ADC1_SE7a | ADC1_SE7a | PTE3 | SPI1_SIN | UART1_RTS_ b | SDHC0_CMD | | | | |
| E7 | — | VDD | VDD | VDD | | | | | | | | |
| F7 | — | VSS | VSS | VSS | | | | | | | | |
| H7 | 5 | PTE4/ LLWU_P2 | DISABLED | | PTE4/ LLWU_P2 | SPI1_PCS0 | UART3_TX | SDHC0_D3 | | | | |
| G4 | 6 | PTE5 | DISABLED | | PTE5 | SPI1_PCS2 | UART3_RX | SDHC0_D2 | | | | |
| E6 | 7 | VDD | VDD | VDD | | | | | | | | |
| G7 | 8 | VSS | VSS | VSS | | | | | | | | |
| L6 | — | VSS | VSS | VSS | | | | | | | | |
| F1 | 9 | USB0_DP | USB0_DP | USB0_DP | | | | | | | | |
| F2 | 10 | USB0_DM | USB0_DM | USB0_DM | | | | | | | | |
| G1 | 11 | VOUT33 | VOUT33 | VOUT33 | | | | | | | | |
| G2 | 12 | VREGIN | VREGIN | VREGIN | | | | | | | | |
| K1 | 13 | PGA0_DP/ ADC0_DP0/ ADC1_DP3 | PGA0_DP/ ADC0_DP0/ ADC1_DP3 | PGA0_DP/ ADC0_DP0/ ADC1_DP3 | | | | | | | | |
| K2 | 14 | PGA0_DM/ ADC0_DM0/ ADC1_DM3 | PGA0_DM/ ADC0_DM0/ ADC1_DM3 | PGA0_DM/ ADC0_DM0/ ADC1_DM3 | | | | | | | | |
| L1 | 15 | PGA1_DP/ ADC1_DP0/ ADC0_DP3 | PGA1_DP/ ADC1_DP0/ ADC0_DP3 | PGA1_DP/ ADC1_DP0/ ADC0_DP3 | | | | | | | | |
| L2 | 16 | PGA1_DM/ ADC1_DM0/ ADC0_DM3 | PGA1_DM/ ADC1_DM0/ ADC0_DM3 | PGA1_DM/ ADC1_DM0/ ADC0_DM3 | | | | | | | | |
| F5 | 17 | VDDA | VDDA | VDDA | | | | | | | | |
| G5 | 18 | VREFH | VREFH | VREFH | | | | | | | | |
| G6 | 19 | VREFL | VREFL | VREFL | | | | | | | | |

| 81 MAP BGA | 80 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| F6 | 20 | VSSA | VSSA | VSSA | | | | | | | | |
| L3 | 21 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18 | | | | | | | | |
| K5 | 22 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | DAC0_OUT/ CMP1_IN3/ ADC0_SE23 | | | | | | | | |
| L4 | 23 | XTAL32 | XTAL32 | XTAL32 | | | | | | | | |
| L5 | 24 | EXTAL32 | EXTAL32 | EXTAL32 | | | | | | | | |
| K6 | 25 | VBAT | VBAT | VBAT | | | | | | | | |
| J6 | 26 | PTA0 | JTAG_TCLK/ SWD_CLK/ EZP_CLK | TSI0_CH1 | PTA0 | UART0_CTS_ b | FTM0_CH5 | | | | JTAG_TCLK/ SWD_CLK | EZP_CLK |
| H8 | 27 | PTA1 | JTAG_TDI/ EZP_DI | TSI0_CH2 | PTA1 | UART0_RX | FTM0_CH6 | | | | JTAG_TDI | EZP_DI |
| J7 | 28 | PTA2 | JTAG_TDO/ TRACE_SWO/ EZP_DO | TSI0_CH3 | PTA2 | UART0_TX | FTM0_CH7 | | | | JTAG_TDO/ TRACE_SWO | EZP_DO |
| H9 | 29 | PTA3 | JTAG_TMS/ SWD_DIO | TSI0_CH4 | PTA3 | UART0_RTS_ b | FTM0_CH0 | | | | JTAG_TMS/ SWD_DIO | |
| J8 | 30 | PTA4/ LLWU_P3 | NMI_b/ EZP_CS_b | TSI0_CH5 | PTA4/ LLWU_P3 | | FTM0_CH1 | | | | NMI_b | EZP_CS_b |
| K7 | 31 | PTA5 | DISABLED | | PTA5 | | FTM0_CH2 | | CMP2_OUT | I2S0_RX_ BCLK | JTAG_TRST | |
| E5 | — | VDD | VDD | VDD | | | | | | | | |
| G3 | — | VSS | VSS | VSS | | | | | | | | |
| K8 | 32 | PTA12 | CMP2_IN0 | CMP2_IN0 | PTA12 | CAN0_TX | FTM1_CH0 | | | I2S0_TXD | FTM1_QD_ PHA | |
| L8 | 33 | PTA13/ LLWU_P4 | CMP2_IN1 | CMP2_IN1 | PTA13/ LLWU_P4 | CAN0_RX | FTM1_CH1 | | | I2S0_TX_FS | FTM1_QD_ PHB | |
| K9 | 34 | PTA14 | DISABLED | | PTA14 | SPI0_PCS0 | UART0_TX | | | I2S0_TX_ BCLK | | |
| L9 | 35 | PTA15 | DISABLED | | PTA15 | SPI0_SCK | UART0_RX | | | I2S0_RXD | | |
| J10 | 36 | PTA16 | DISABLED | | PTA16 | SPI0_SOUT | UART0_CTS_ b | | | I2S0_RX_FS | | |
| H10 | 37 | PTA17 | ADC1_SE17 | ADC1_SE17 | PTA17 | SPI0_SIN | UART0_RTS_ b | | | I2S0_MCLK | I2S0_CLKIN | |
| L10 | 38 | VDD | VDD | VDD | | | | | | | | |
| K10 | 39 | VSS | VSS | VSS | | | | | | | | |
| L11 | 40 | PTA18 | EXTAL | EXTAL | PTA18 | | FTM0_FLT2 | FTM_CLKIN0 | | | | |
| K11 | 41 | PTA19 | XTAL | XTAL | PTA19 | | FTM1_FLT0 | FTM_CLKIN1 | | LPT0_ALT1 | | |
| J11 | 42 | RESET_b | RESET_b | RESET_b | | | | | | | | |
| G11 | 43 | PTB0/ LLWU_P5 | LCD_P0/ ADC0_SE8/ | LCD_P0/ ADC0_SE8/ ADC1_SE8/ TSI0_CH0 | PTB0/ LLWU_P5 | I2C0_SCL | FTM1_CH0 | | | FTM1_QD_ PHA | LCD_P0 | |

| 81 MAP BGA | 80 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| J9 | — | NC | NC | NC | | | | | | | | |
| J4 | — | NC | NC | NC | | | | | | | | |
| H11 | — | NC | NC | NC | | | | | | | | |
| F11 | — | NC | NC | NC | | | | | | | | |
| E11 | — | NC | NC | NC | | | | | | | | |
| F10 | — | NC | NC | NC | | | | | | | | |
| F9 | — | NC | NC | NC | | | | | | | | |
| F8 | — | NC | NC | NC | | | | | | | | |
| E8 | — | NC | NC | NC | | | | | | | | |
| B6 | — | NC | NC | NC | | | | | | | | |
| A6 | — | NC | NC | NC | | | | | | | | |
| A5 | — | NC | NC | NC | | | | | | | | |
| B5 | — | NC | NC | NC | | | | | | | | |
| D5 | — | NC | NC | NC | | | | | | | | |
| C4 | — | NC | NC | NC | | | | | | | | |
| B4 | — | NC | NC | NC | | | | | | | | |
| A4 | — | NC | NC | NC | | | | | | | | |
| B1 | — | NC | NC | NC | | | | | | | | |
| C1 | — | NC | NC | NC | | | | | | | | |
| D1 | — | NC | NC | NC | | | | | | | | |
| E1 | — | NC | NC | NC | | | | | | | | |
| C2 | — | NC | NC | NC | | | | | | | | |
| D2 | — | NC | NC | NC | | | | | | | | |

## 8.2 K40 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

## Table 50. Revision History

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 1 | 11/2010 | Initial public revision |
| 2 | 3/2011 | Many updates throughout<br>Corrected 81- and 104-pin package codes |
| 3 | 3/2011 | Added sections that were inadvertently removed in previous revision |
| 4 | 3/2011 | Reworded $I_{IC}$ footnote in "Voltage and Current Operating Requirements" table.<br>Added paragraph to "Peripheral operating requirements and behaviors" section.<br>Added "JTAG full voltage range electricals" table to the "JTAG electricals" section. |
| 5 | 6/2011 | • Changed supported part numbers per new part number scheme<br>• Changed *DC injection current* specs in "Voltage and current operating requirements" table<br>• Changed *Input leakage current* and *internal pullup/pulldown resistor* specs in "Voltage and current operating behaviors" table<br>• Split *Low power stop mode current* specs by temperature range in "Power consumption operating behaviors" table<br>• Changed typical $I_{DD\_VBAT}$ spec in "Power consumption operating behaviors" table<br>• Added LPTMR clock specs to "Device clock specifications" table<br>• Changed *Minimum external reset pulse width* in "General switching specifications" table<br>• Changed *PLL operating current* in "MCG specifications" table<br>• Added footnote to *PLL period jitter* in "MCG specifications" table<br>• Changed *Supply current* in "Oscillator DC electrical specifications" table<br>• Changed *Crystal startup time* in "Oscillator frequency specifications" table<br>• Changed *Operating voltage* in "EzPort switching specifications" table<br>• Changed *ADC asynchronous clock source* specs in "16-bit ADC characteristics" table<br>• Changed *Gain* spec in "16-bit ADC with PGA characteristics" table<br>• Added typical *Input DC current* to "16-bit ADC with PGA characteristics" table<br>• Changed *Input offset voltage* and *ENOB* notes field in "16-bit ADC with PGA characteristics" table<br>• Changed *Analog comparator initialization delay* in "Comparator and 6-bit DAC electrical specifications"<br>• Changed *Code-to-code settling time*, *DAC output voltage range low*, and *Temperature coefficient offset voltage* in "12-bit DAC operating behaviors" table<br>• Changed *Temperature drift* and *Load regulation* in "VREF full-range operating behaviors" table<br>• Changed *Regulator output voltage* in "USB VREG electrical specifications" table<br>• Changed $I_{LIM}$ description and specs in "USB VREG electrical specifications" table<br>• Changed *DSPI_SCK cycle time* specs in "DSPI timing" tables<br>• Changed $\overline{\text{DSPI\_SS}}$ specs in "Slave mode DSPI timing (low-speed mode)" table<br>• Changed *DSPI_SCK to DSPI_SOUT valid* spec in "Slave mode DSPI timing (high-speed mode)" table<br>• Changed *Reference oscillator current source base current* spec and added *Low-power current adder* footer in "TSI electrical specifications" table<br>• Added *LCD glass capacitance* footnote |

*Table continues on the next page...*

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Document Number: K40P81M100SF2
Rev. 7, 02/2013


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