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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78e365a40dl

6.2 Timers 0, 1, and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0, 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2. The operations of Timer 0 and Timer 1 are the same as in the W78C51. Timer 2 is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

6.2.1 Timer 2 Output

If set T2OE (T2MOD.1) bit and clear C/T2 (T2CON.1) bit at auto-reload mode, P1.0 will be toggled once overflow.

TIMER 2 Mode

Bit:	7	6	5	4	3	2	1	0
							T2OE	

Mnemonic: T2MOD Address: C9H

T2OE: Enable this bit to toggle P1.0 pin while Timer2 has been overflowed.

6.3 Clock

The W78E365 is designed with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used by default. This makes the W78E365 relatively insensitive to duty cycle variations in the clock.

6.3.1 Crystal Oscillator

The W78E365 incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground.

6.3.2 External Clock

An external clock should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator.

6.4 Power Management

6.4.1 Idle Mode

Setting the IDL bit in the PCON register enters the idle mode. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

6.4.2 Power-down Mode

When the PD bit in the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator. To exit from power-down mode is by a hardware reset or external interrupts $\overline{INT0}$ to $\overline{INT1}$ when enabled and set to level triggered.

6.4.3 Reduce EMI Emission

The W78E365 allows user to diminish the gain of on-chip oscillator amplifier by using programmer to clear the B7 bit of security register. Once B7 is set to 0, a half of gain will be decreased. Care must be taken if user attempts to diminish the gain of oscillator amplifier, reducing a half of gain may affect the external crystal operating improperly at high frequency. The value of C1 and C2 may need some adjustment while running at lower gain.

ALE Off Function

Auxiliary Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	ALEOFF

Mnemonic: AUXR Address: 8EH

ALEOFF: Set this bit to disable ALE output.

6.5 Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the W78E365 is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line. During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

6.5.1 W78E365 Special Function Registers (SFRs) and Reset Values

F8								
F0	+B 00000000						CHPENR 00000000	
E8								
E0	+ACC 00000000							
D8	+P4 11111111	PWMP 00000000	PWM0 00000000	PWM1 00000000	PWMCON1 00000000	PWM2 00000000	PWM3 00000000	
D0	+PSW 00000000							
C8	+T2CON 00000000	T2MOD 00000000	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000	PWMCON2 00000000	PWM4 00000000
C0	+XICON 00000000		P4CONA 00000000	P4CONB 00000000	SFRAL 00000000	SFRAH 00000000	SFRFD 00000000	SFRCN 00000000

Eight-source interrupt information:

INTERRUPT SOURCE	VECTOR ADDRESS	POLLING SEQUENCE WITHIN PRIORITY LEVEL	ENABLE REQUIRED SETTINGS	INTERRUPT TYPE EDGE/LEVEL
External Interrupt 0	03H	0 (highest)	IE.0	TCON.0
Timer/Counter 0	0BH	1	IE.1	-
External Interrupt 1	13H	2	IE.2	TCON.2
Timer/Counter 1	1BH	3	IE.3	-
Serial Port	23H	4	IE.4	-
Timer/Counter 2	2BH	5	IE.5	-
External Interrupt 2	33H	6	XICON.2	XICON.0
External Interrupt 3	3BH	7 (lowest)	XICON.6	XICON.3

P4CONB (C3H)

BIT	NAME	FUNCTION
7, 6	P43FUN1 P43FUN0	00: Mode 0. P4.3 is a general purpose I/O port which is the same as Port1. 01: Mode 1. P4.3 is a Read Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1 and P43CMP0. 10: Mode 2. P4.3 is a Write Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1 and P43CMP0. 11: Mode 3. P4.3 is a Read/Write Strobe signal for chip select purpose. The address range depends on the SFR P43AH, P43AL, P43CMP1, and P43CMP0.
5, 4	P43CMP1 P43CMP0	Chip-select signals address comparison: 00: Compare the full address (16 bits length) with the base address register P43AH, P43AL. 01: Compare the 15 high bits (A15–A1) of address bus with the base address register P43AH, P43AL. 10: Compare the 14 high bits (A15–A2) of address bus with the base address register P43AH, P43AL. 11: Compare the 8 high bits (A15–A8) of address bus with the base address register P43AH, P43AL.
3, 2	P42FUN1 P42FUN0	The P4.2 function control bits which are the similar definition as P43FUN1, P43FUN0.
1, 0	P42CMP1 P42CMP0	The P4.2 address comparator length control bits which are the similar definition as P43CMP1, P43CMP0.

6.7 Pulse Width Modulated Outputs (PWM)

There are five pulse width modulated output channels to generate pulses of programmable length and interval. The repetition frequency is defined by an 8-bit prescaler PWMP, which supplies the clock for the counter. The prescaler and counter are common to both PWM channels. The 8-bit counter counts modular 255 (0 ~ 254). The value of the 8-bit counter compared to the contents of five registers: PWM0, PWM1, PWM2, PWM3 and PWM4. Provided the contents of either these registers is greater than the counter value, the corresponding PWM0, PWM1, PWM2, PWM3 or PWM4 output is set HIGH. If the contents of these registers are equal to, or less than the counter value, the output will be LOW. The pulse-width-ratio is defined by the contents of the registers PWM0, PWM1, PWM2, PWM3 and PWM4. The pulse-width-ratio is in the range of 0 to 1 and may be programmed in increments of 1/255. ENPWM0, ENPWM1, ENPWM2, ENPWM3 and ENPWM4 bit will enable or disable PWM output.

Buffered PWM outputs may be used to drive DC motors. The rotation speed of the motor would be proportional to the contents of PWM0/1/2/3/4. The repetition frequency f_{pwm}, at the PWM0/1/2/3/4 output is given by:

$$f_{pwm} = \frac{f_{osc}}{2 \times (1 + PWMP) \times 255}$$

Prescaler division factor = PWM + 1

PWMn high/low ratio of $\mathrm{PWMn} = \dfrac{(\mathrm{PWMn})}{255 - (\mathrm{PWMn})}$

This gives a repetition frequency range of 123 Hz to 31.4K Hz (f_{osc} = 16M Hz). By loading the PWM registers with either 00H or FFH, the PWM channels will output a constant HIGH or LOW level, respectively. Since the 8-bit counter counts modulo 255, it can never actually reach the value of the PWM registers when they are loaded with FFH.

When a compare register (PWM0, PWM1, PWM2, PWM3, PWM4) is loaded with a new value, the associated output updated immediately. It does not have to wait until the end of the current counter period. There is weakly pulled high on PWM output.

PWM3 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM3 Address: DEH

PWM2 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM2 Address: DDH

PWM Control 1 Register

Bit:	7	6	5	4	3	2	1	0
	PWM3OE	PWM2OE	ENPWM3	ENPWM2	PWM1OE	PWM0OE	ENPWM1	ENWPM0

Mnemonic: PWMCON1 Address: DCH

PWM3OE: Output enable for PWM3
PWM2OE: Output enable for PWM2
ENPWM3: Enable PWM3
ENPWM2: Enable PWM2
PWM1OE: Output enable for PWM1
PWM0OE: Output enable for PWM0
ENPWM1: Enable PWM1
ENPWM0: Enable PWM0

PWM1 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM1 Address: DBH

PWM0 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM0 Address: DAH

PWMP Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWMP Address: D9H

PWM4 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM4 Address: CFH

PWM Control 2 Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	PWM4OE	-	ENWPM4

Mnemonic: PWMCON2 Address: CEH

PWM4OE: Output enable for PWM4

ENPWM: Enable for PWM4

6.8 Watchdog Timer

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs, a system reset can also be caused if it is enabled. The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed. The Watchdog timer will de disabled on reset. In general, software should restart the Watchdog timer to put it into a known state. The control bits that support the Watchdog timer are discussed below.

Watchdog Timer Control Register

Bit:	7	6	5	4	3	2	1	0
	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0

Mnemonic: WDTC Address: 8FH

ENW : Enable watch-dog if set.

CLRW : Clear watch-dog timer and prescaler if set. This flag will be cleared automatically

WIDL : If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.

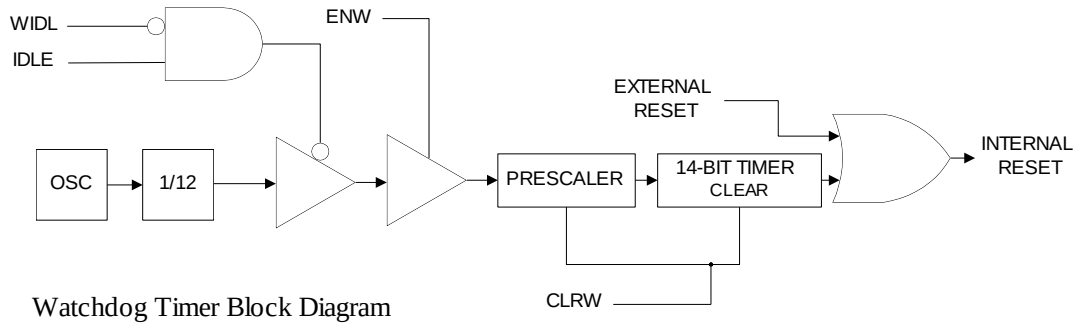
PS2, PS1, PS0: Watch-dog prescaler timer select. Prescaler is selected when set PS2–0 as follows:

PS2	PS1	PS0	PRESCALER SELECT
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

The time-out period is obtained using the following equation:

$$\frac{1}{OSC} \times 2^{14} \times PRESCALER \times 1000 \times 12 \text{ mS}$$

Before Watchdog time-out occurs, the program must clear the 14-bit timer by writing 1 to WDTC.6 (CLRW). After 1 is written to this bit, the 14-bit timer, prescaler and this bit will be reset on the next instruction cycle. The Watchdog timer is cleared on reset.



Watchdog Timer Block Diagram

Typical Watch-Dog time-out period when OSC = 20 MHz

PS2	PS1	PS0	WATCHDOG TIME-OUT PERIOD
0	0	0	19.66 mS
0	0	1	39.32 mS
0	1	0	78.64 mS
0	1	1	157.28 mS
1	0	0	314.57 mS
1	0	1	629.14 mS
1	1	0	1.25 S
1	1	1	2.50 S

6.9 In-System Programming (ISP) Mode

The W78E365 equips one 64K byte of main ROM bank for application program (called APROM) and one 4K byte of auxiliary ROM bank for loader program (called LDROM). In the normal operation, the microcontroller executes the code in the APROM. If the content of APROM needs to be modified, the W78E365 allows user to activate the In-System Programming (ISP) mode by setting the CHPCON register. **The CHPCON is read-only by default, software must write two specific values 87H, then 59H sequentially to the CHPENR register to enable the CHPCON write attribute. Writing CHPENR register with the values except 87H and 59H will close CHPCON register write attribute.** The W78E365 achieves all in-system programming operations including enter/exit ISP Mode, program, erase, read ... etc, during device in the idle mode. Setting the bit CHPCON.0 the device will enter in-system programming mode after a wake-up from idle mode. Because device needs proper time to complete the ISP operations before awaken from idle mode, software may use timer interrupt to control the duration for device wake-up from idle mode. To perform ISP operation for revising contents of APROM, software located at APROM setting the CHPCON register then enter idle mode, after awaken from idle mode the device executes the corresponding interrupt service routine in LDROM. Because the device will clear the program counter while switching from APROM to LDROM, the first execution of RETI instruction in interrupt service routine will jump to 00H at LDROM area. The device offers a software reset for switching back to APROM while the content of APROM has been updated completely. **Setting CHPCON register bit 0, 1 and 7 to logic-1 will result a software reset to reset the CPU**. The software reset serves as a external reset. This in-system programming feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-system programming feature make it possible to easily update the system firmware without opening the chassis.

SFRAH, SFRAL: The objective address of on-chip ROM in the in-system programming mode. SFRAH contains the high-order byte of address, SFRAL contains the low-order byte of address.

SFRFD: The programming data for on-chip ROM in programming mode.

SFRCN: The control byte of on-chip ROM programming mode.

SFRCN (C7)

BIT	NAME	FUNCTION
7	-	Reserve.
6	WFWIN	On-chip ROM bank select for in-system programming. = 0: 64K bytes ROM bank is selected as destination for re-programming. = 1: 4K bytes ROM bank is selected as destination for re-programming.
5	OEN	ROM output enable.
4	CEN	ROM chip enable.
3, 2, 1, 0	CTRL[3:0]	The flash control signals

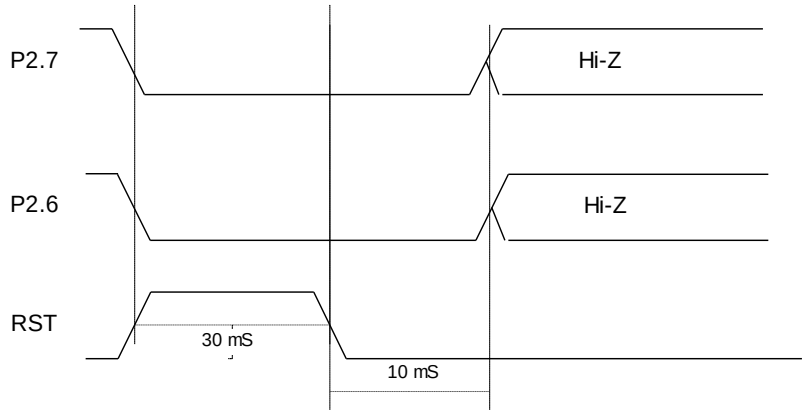
6.11 H/W Reboot Mode (Boot from LDROM)

By default, the W78E365 boots from APROM program after a power on reset. On some occasions, user can force the W78E365 to boot from the LDROM program via following settings. The possible situation that you need to enter H/W REBOOT mode when the APROM program can not run properly and device can not jump back to LDROM to execute in-system programming function. Then you can use this H/W REBOOT mode to force the W78E365 jumps to LDROM and executes in-system programming procedure. When you design your system, you may reserve the pins P2.6, P2.7 to switches or jumpers. For example in a CD-ROM system, you can connect the P2.6 and P2.7 to PLAY and EJECT buttons on the panel. When the APROM program fails to execute the normal application program. User can press both two buttons at the same time and then turn on the power of the personal computer to force the W78E365 to enter the H/W REBOOT mode. After power on of personal computer, you can release both buttons and finish the in-system programming procedure to update the APROM code. In application system design, user must take care of the P2, P3, ALE, $\overline{EA}$ and $\overline{PSEN}$ pin value at reset to prevent from accidentally activating the programming mode or H/W REBOOT mode. It is necessary to add 10K resistor on these P2.6, P2.7 and P4.3 pins.

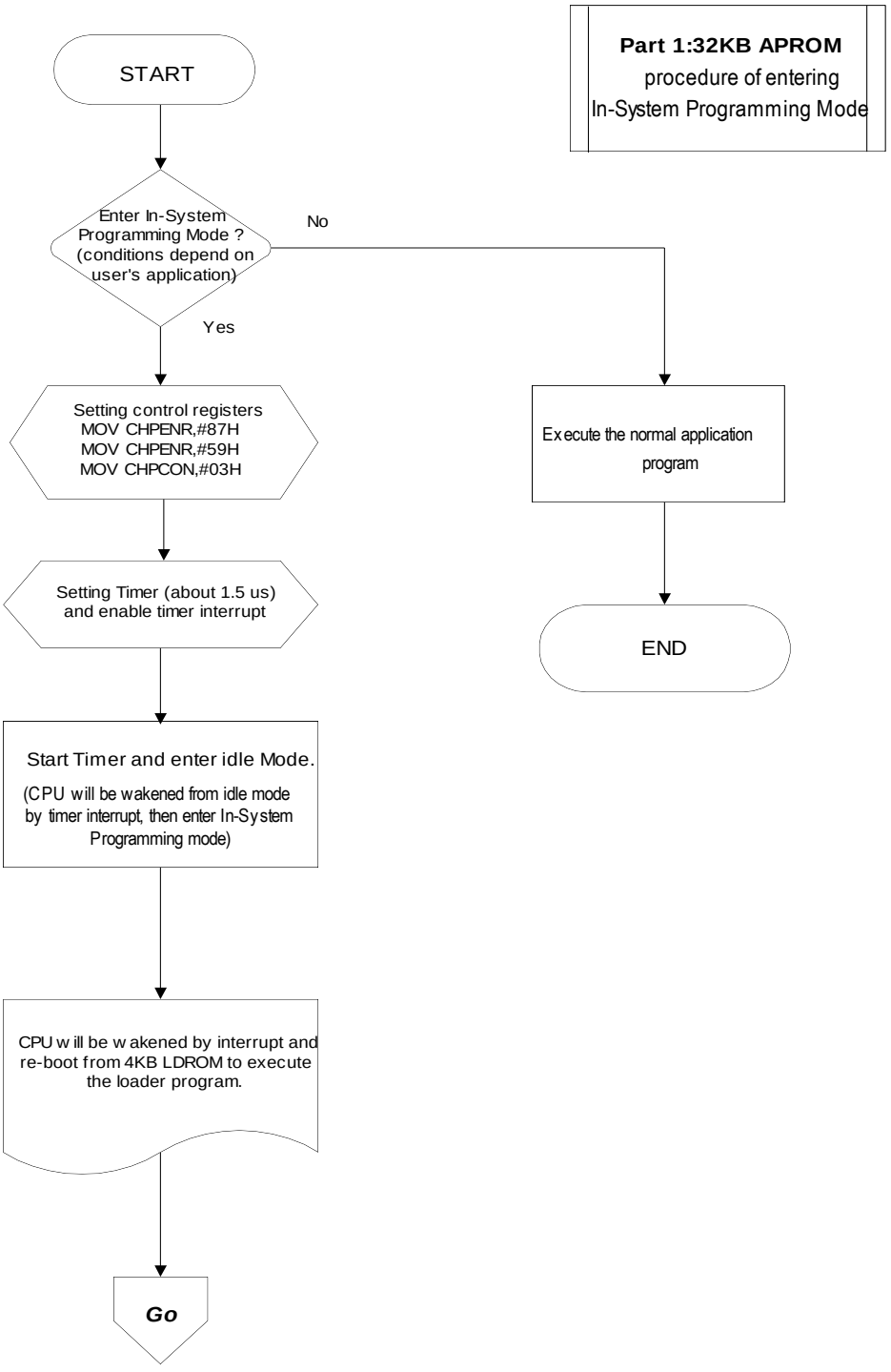
H/W Reboot Mode

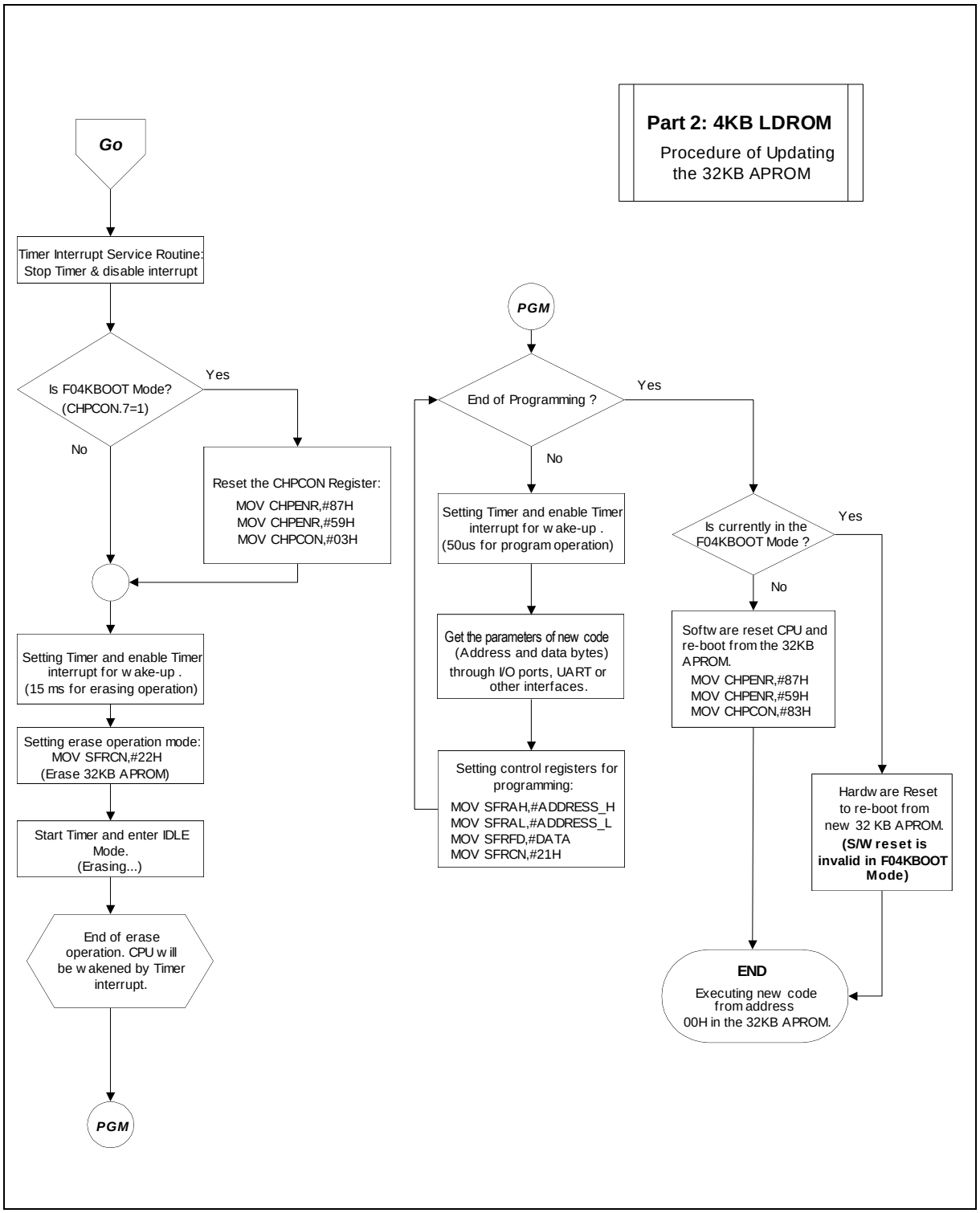
P4.3	P2.7	P2.6	MODE
X	L	L	REBOOT
L	X	X	REBOOT

The Reset Timing For Entering F04KBOOT Mode



The Algorithm of In-System Programming

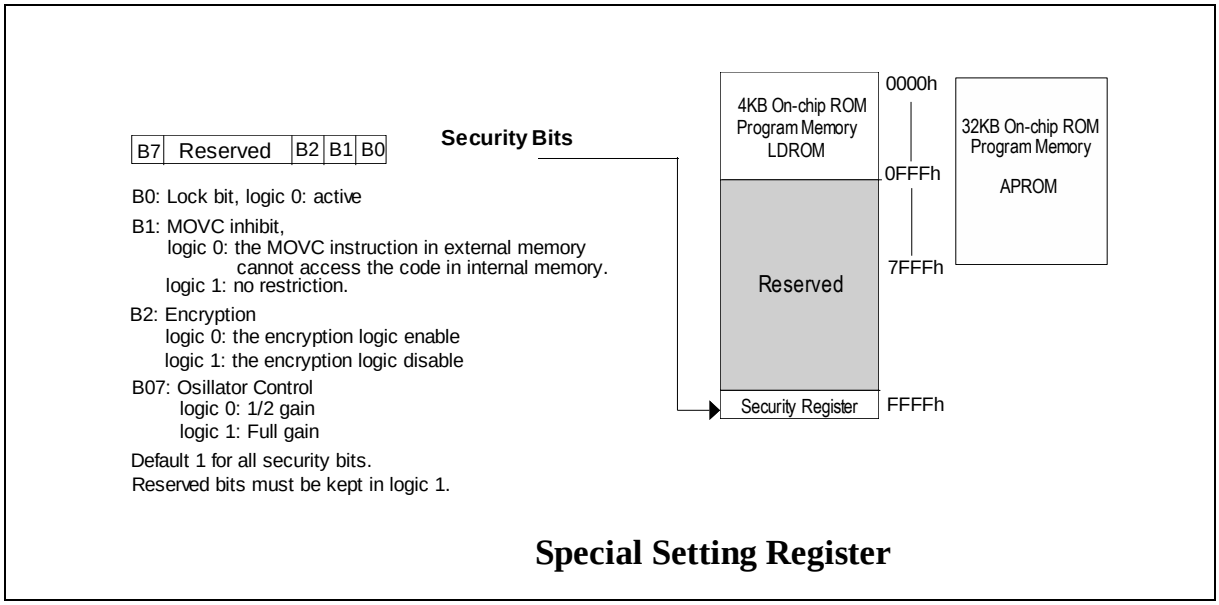



Part 2: 4KB LDROM
Procedure of Updating the 32KB APROM
Go
Timer Interrupt Service Routine: Stop Timer & disable interrupt
Is F04KBOOT Mode? (CHPCON.7=1)
Yes
No
Reset the CHPCON Register:
MOV CHPENR,#87H
MOV CHPENR,#59H
MOV CHPCON,#03H
Setting Timer and enable Timer interrupt for w ake-up . (15 ms for erasing operation)
Setting erase operation mode: MOV SFRCN,#22H (Erase 32KB APROM)
Start Timer and enter IDLE Mode. (Erasing...)
End of erase operation. CPU w ill be w akened by Timer interrupt.
PGM
PGM
End of Programming ?
Yes
No
Setting Timer and enable Timer interrupt for w ake-up . (50us for program operation)
Get the parameters of new code (Address and data bytes) through I/O ports, UART or other interfaces.
Setting control registers for programming:
MOV SFRAH,#ADDRESS_H
MOV SFRAL,#ADDRESS_L
MOV SFRFD,#DATA
MOV SFRCN,#21H
Is currently in the F04KBOOT Mode ?
Yes
No
Softw are reset CPU and re-boot from the 32KB APROM.
MOV CHPENR,#87H
MOV CHPENR,#59H
MOV CHPCON,#83H
Hardw are Reset to re-boot from new 32 KB APROM.
(S/W reset is invalid in F04KBOOT Mode)
END
Executing new code from address 00H in the 32KB APROM.

6.12 Security

During the on-chip ROM programming mode, the ROM can be programmed and verified repeatedly. Until the code inside the ROM is confirmed OK, the code can be protected. The protection of ROM and those operations on it are described below.

The W78E365 has a Security Register that can be accessed in programming mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The Security Register is located at the 0FFFFH of the LDROM space.



Special Setting Register

Lock bit

This bit is used to protect the customer's program code in the W78E365. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the ROM data and Security Register can not be accessed again.

MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+6.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{ST}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

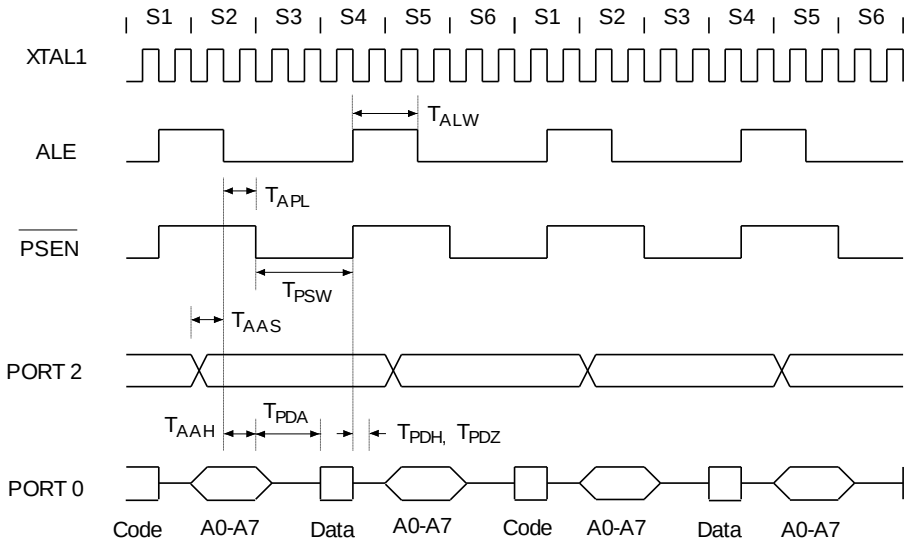
7.2 D.C. Characteristics

(V_{DD} – V_{SS}= 5V ±10%, T_A = 25°C, Fosc = 20 MHz, unless otherwise specified.)

SYMBOL	PARAMETER	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
V_{DD}	Operating Voltage	4.5	5.5	V	RST = 1, P0 = V_{DD}
I_{DD}	Operating Current	-	20	mA	No load V_{DD} = 5.5V
I_{IDLE}	Idle Current	-	6	mA	Idle mode V_{DD} = 5.5V
I_{PWDN}	Power Down Current	-	10	µA	Power-down mode V_{DD} = 5.5V
I_{IN1}	Input Current P1, P2, P3, P4	-50	+10	µA	V_{DD} = 5.5V V_{IN} = 0V or V_{DD}
I_{IN2}	Input Current RST	-10	+300	µA	V_{DD} = 5.5V 0<V_{IN}<V_{DD}
I_{LK}	Input Leakage Current P0, $\overline{EA}$	-10	+10	µA	V_{DD} = 5.5V 0V<V_{IN}<V_{DD}
I_{TL} [*4]	Logic 1 to 0 Transition Current P1, P2, P3, P4	-500	-200	µA	V_{DD} = 5.5V V_{IN} = 2.0V
VIL1	Input Low Voltage P0, P1, P2, P3, P4, $\overline{EA}$	0	0.8	V	VDD = 4.5V
V IL2	Input Low Voltage RST	0	0.8	V	VDD = 4.5V

8. TIMING WAVEFORMS

8.1 Program Fetch Cycle

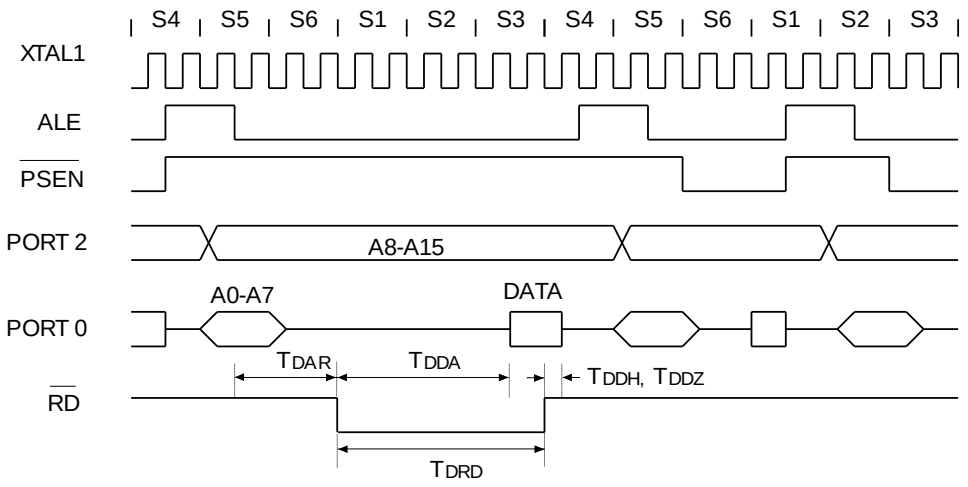


PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	T_{AAS}	1 T_{CP}-Δ	-	-	nS	4
Address Hold from ALE Low	T_{AAH}	1 T_{CP}-Δ	-	-	nS	1, 4
ALE Low to $\overline{PSEN}$ Low	T_{APL}	1 T_{CP}-Δ	-	-	nS	4
$\overline{PSEN}$ Low to Data Valid	T_{PDA}	-	-	2 T_{CP}	nS	2
Data Hold after $\overline{PSEN}$ High	T_{PDH}	0	-	1 T_{CP}	nS	3
Data Float after $\overline{PSEN}$ High	T_{PDZ}	0	-	1 T_{CP}	nS	
ALE Pulse Width	T_{ALW}	2 T_{CP}-Δ	2 T_{CP}	-	nS	4
$\overline{PSEN}$ Pulse Width	T_{PSW}	3 T_{CP}-Δ	3 T_{CP}	-	nS	4

Notes:

1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 T_{CP}.
3. Data have been latched internally prior to $\overline{PSEN}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

8.2 Data Read Cycle

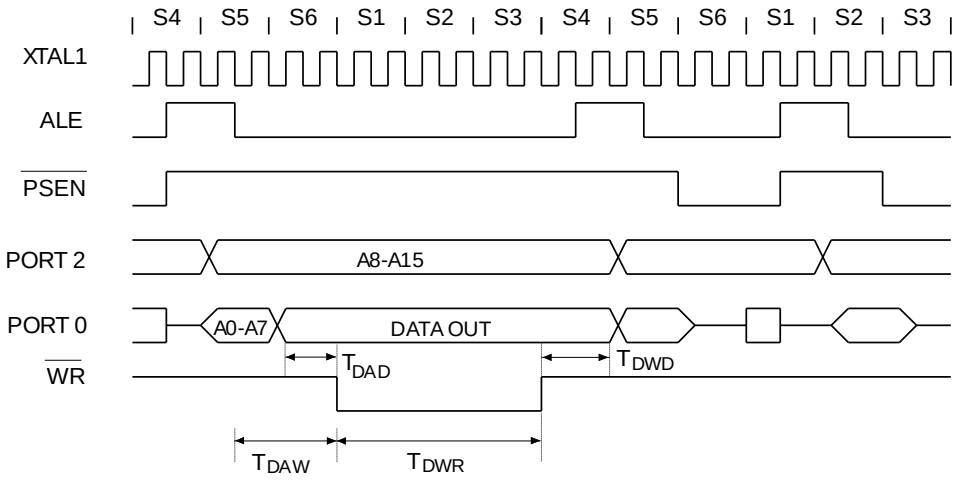


PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{RD}$ Low	TDAR	3 TCP-Δ	-	3 TCP+Δ	nS	1, 2
$\overline{RD}$ Low to Data Valid	TDDA	-	-	4 TCP	nS	1
Data Hold from $\overline{RD}$ High	TDDH	0	-	2 TCP	nS	
Data Float from $\overline{RD}$ High	TDDZ	0	-	2 TCP	nS	
$\overline{RD}$ Pulse Width	TDRD	6 TCP-Δ	6 TCP	-	nS	2

Notes:

1. Data memory access time is 8 TCP.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

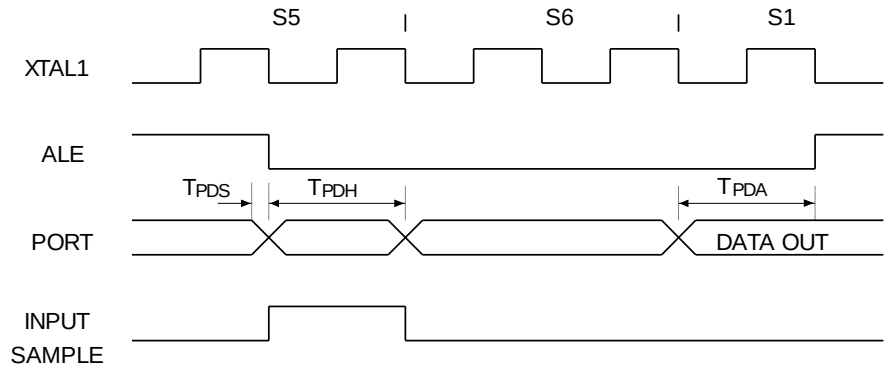
8.3 Data Write Cycle



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{WR}$ Low	TDAW	3 TCP-Δ	-	3 TCP+Δ	nS
Data Valid to $\overline{WR}$ Low	TDAD	1 TCP-Δ	-	-	nS
Data Hold from $\overline{WR}$ High	TDWD	1 TCP-Δ	-	-	nS
$\overline{WR}$ Pulse Width	TDWR	6 TCP-Δ	6 TCP	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

8.4 Port Access Cycle



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	TPDS	1 TCP	-	-	nS
Port Input Hold from ALE Low	TPDH	0	-	-	nS
Port Output to ALE	TPDA	1 TCP	-	-	nS

Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

```
;*******************************************************************************
;*  4KB LDROM MAIN PROGRAM
;*******************************************************************************
        ORG 100H
MAIN_4K:
        MOV SP, #C0H
        MOV CHPENR, #87H      ; CHPENR = 87H, CHPCON WRITE ENABLE.
        MOV CHPENR, #59H      ; CHPENR = 59H, CHPCON WRITE ENABLE.
        MOV CHPCON, #03H      ; CHPCON = 03H, ENABLE IN-SYSTEM PROGRAMMING.
        MOV CHPENR, #00H      ; DISABLE CHPCON WRITE ATTRIBUTE

        MOV TCON, #00H        ; TCON = 00H, TR = 0 TIMER0 STOP
        MOV TMOD, #01H        ; TMOD = 01H, SET TIMER0 A 16BIT TIMER
        MOV IP, #00H          ; IP = 00H
        MOV IE, #82H          ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV R6, #F0H
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV TCON, #10H        ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H        ; ENTER IDLE MODE

UPDATE_64K:
        MOV TCON, #00H        ; TCON = 00H, TR = 0 TIM0 STOP
        MOV IP, #00H          ; IP = 00H
        MOV IE, #82H          ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV TMOD, #01H        ; TMOD = 01H, MODE1
        MOV R6, #E0H          ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15 mS. DEPENDING
                              ; ON USER'S SYSTEM CLOCK RATE.
        MOV R7, #B1H
        MOV TL0, R6
        MOV TH0, R7

ERASE_P_4K:
        MOV SFRCN, #22H     ; SFRCN(C7H) = 22H  ERASE 64K
        MOV TCON, #10H      ; TCON = 10H, TR0 = 1,GO
        MOV PCON, #01H      ; ENTER IDLE MODE (FOR ERASE OPERATION)

;*******************************************************************************
;* BLANK CHECK
;*******************************************************************************
        MOV SFRCN, #0H      ; READ 64KB APROM MODE
        MOV SFRAH, #0H      ; START ADDRESS = 0H
        MOV SFRAL, #0H
        MOV R6, #FEH        ; SET TIMER FOR READ OPERATION, ABOUT 1.5 μS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7

BLANK_CHECK_LOOP:
        SETB TR0            ; ENABLE TIMER 0
        MOV PCON, #01H      ; ENTER IDLE MODE
        MOV A, SFRFD        ; READ ONE BYTE
        CJNE A, #FFH, BLANK_CHECK_ERROR
        INC SFRAL           ; NEXT ADDRESS
        MOV A, SFRAL
```

```
        JNZ BLANK_CHECK_LOOP
        INC SFRAH
        MOV A, SFRAH
        CJNE A, #80H, BLANK_CHECK_LOOP   ; END ADDRESS = 7FFFH
        JMP PROGRAM_64KROM

BLANK_CHECK_ERROR:
        MOV P1, #F0H
        MOV P3, #F0H
        JMP $

;*******************************************************************************
;* RE-PROGRAMMING 64KB APROM BANK
;*******************************************************************************
PROGRAM_64KROM:
        MOV DPTR, #0H           ; THE ADDRESS OF NEW ROM CODE
        MOV R2, #00H            ; TARGET LOW BYTE ADDRESS
        MOV R1, #00H            ; TARGET HIGH BYTE ADDRESS
        MOV DPTR, #0H           ; EXTERNAL SRAM BUFFER ADDRESS
        MOV SFRAH, R1           ; SFRAH, TARGET  HIGH ADDRESS
        MOV SFRCN, #21H         ; SFRCN(C7H) = 21 (PROGRAM 64K)
        MOV R6, #BEH            ; SET TIMER FOR PROGRAMMING, ABOUT 50 μS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7

PROG_D_64K:
        MOV SFRAL, R2           ; SFRAL(C4H) = LOW BYTE ADDRESS
        MOVX A, @DPTR           ; READ DATA FROM EXTERNAL SRAM BUFFER. BY ACCORDING USER?
                                ; CIRCUIT, USER MUST MODIFY THIS INSTRUCTION TO FETCH CODE
        MOV SFRFD, A            ; SFRFD(C6H) = DATA IN
        MOV TCON, #10H          ; TCON = 10H, TR0 = 1,GO
        MOV PCON, #01H          ; ENTER IDLE MODE (PRORGAMMING)
        INC DPTR
        INC R2
        CJNE R2, #0H, PROG_D_64K
        INC  R1
        MOV SFRAH, R1
        CJNE R1, #80H, PROG_D_64K

;*******************************************************************************
; * VERIFY 64KB APROM BANK
;*******************************************************************************
        MOV R4, #03H            ; ERROR COUNTER
        MOV R6, #FEH            ; SET TIMER FOR READ VERIFY, ABOUT 1.5 μS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV DPTR, #0H           ; The start address of sample code
        MOV R2, #0H             ; Target  low byte address
        MOV R1, #0H             ; Target  high byte address
        MOV SFRAH, R1           ; SFRAH, Target high address
        MOV SFRCN, #00H         ; SFRCN = 00 (Read ROM CODE)
READ_VERIFY_64K:
        MOV SFRAL, R2             ; SFRAL(C4H) = LOW ADDRESS
        MOV TCON, #10H            ; TCON = 10H, TR0 = 1,GO
```