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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

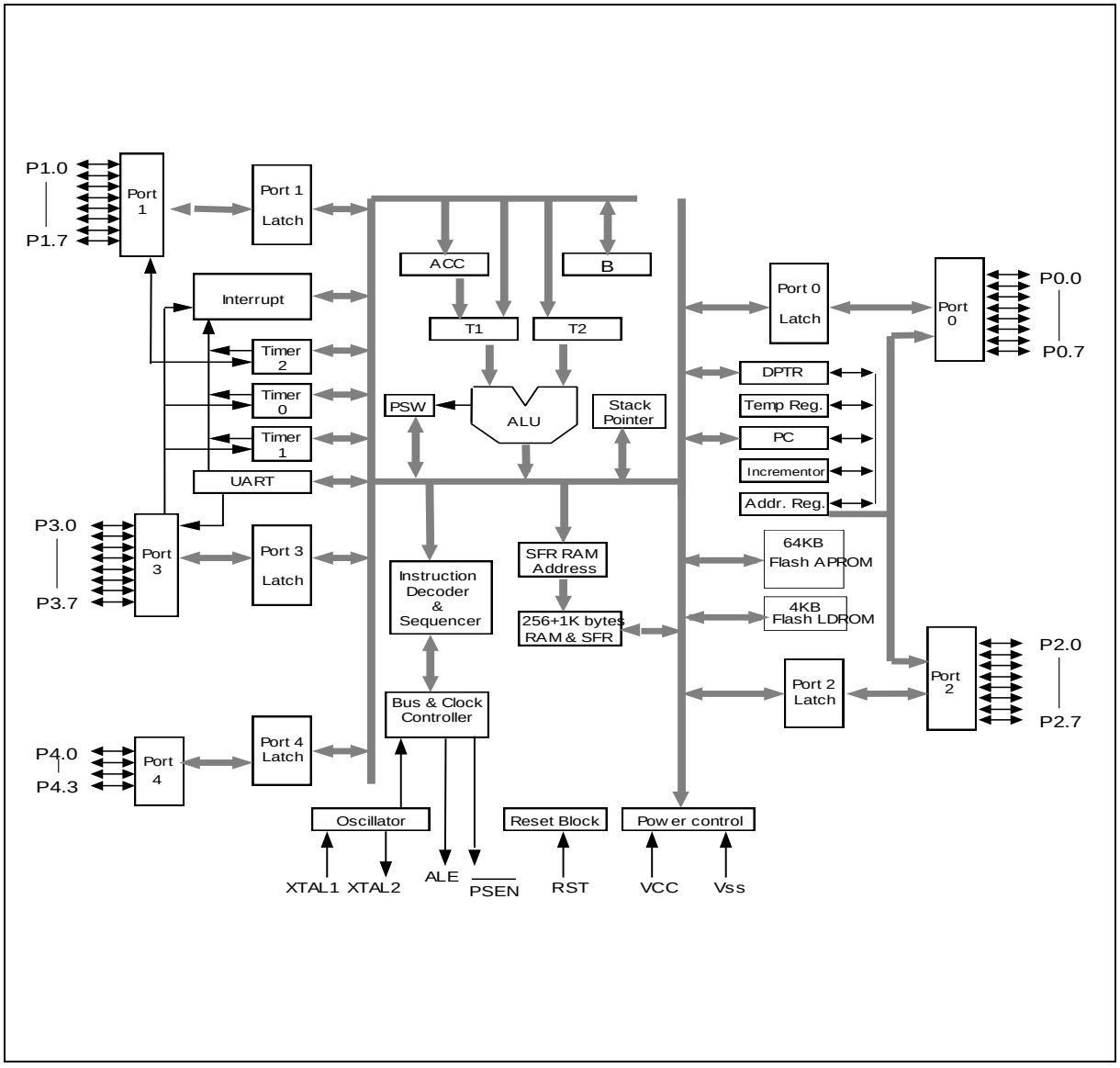
Details	
Product Status	Not For New Designs
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78e365a40fl

4. PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTIONS
$\overline{EA}$	I	EXTERNAL ACCESS ENABLE: This pin forces the processor to execute the external ROM. The ROM address and data will not be presented on the bus if the $\overline{EA}$ pin is high.
$\overline{PSEN}$	O H	PROGRAM STORE ENABLE: $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.
ALE	O H	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency.
RST	I L	RESET: A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	I	CRYSTAL 1: This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	O	CRYSTAL 2: This is the crystal oscillator output. It is the inversion of XTAL1.
V_{SS}	I	GROUND: ground potential.
V_{DD}	I	POWER SUPPLY: Supply voltage for operation.
P0.0 – P0.7	I/O D	PORT 0: Function is the same as that of standard 8052. This port also provides a multiplexed low order address/data bus during accesses to external memory. Port 0 has internal pull-up resisters enabled by software.
P1.0 – P1.7	I/O H	PORT 1: Function is the same as that of standard 8052.
P2.0 – P2.7	I/O H	PORT 2: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory. The P2.6 and P2.7 also provide the alternate function $\overline{REBOOT}$ which is H/W reboot from LD flash.
P3.0 – P3.7	I/O H	PORT 3: Function is the same as that of the standard 8052.
P4.0 – P4.7	I/O H	PORT 4: A bi-directional I/O. The P4.3 also provides the alternate function $\overline{REBOOT}$ which is H/W reboot from LD flash.

*** Note: TYPE** I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain

5. BLOCK DIAGRAM



6. FUNCTIONAL DESCRIPTION

The W78E365 architecture consists of a core controller surrounded by various registers, four general purpose I/O ports, one special purpose programmable 4-bits I/O port, 256+1K bytes of RAM, three timer/counters, a serial port. The processor supports 111 different opcodes and references both a 64K program address space and a 64K data storage space.

6.1 RAM

The internal data RAM in the W78E365 is 256+1K bytes. It is divided into two banks: 256 bytes of scratchpad RAM and 1K bytes of AUX-RAM. These RAMs are addressed by different ways.

- RAM 0H – 7FH can be addressed directly and indirectly as the same as in 8051. Address pointers are R0 and R1 of the selected register bank.
- RAM 80H – FFH can only be addressed indirectly as the same as in 8051. Address pointers are R0, R1 of the selected registers bank.
- AUX-RAM 0H – 3FFH is addressed indirectly as the same way to access external data memory with the MOVX instruction. Address pointer are R0 and R1 of the selected register bank and DPTR register. An access to external data memory locations higher than 3FFH will be performed with the MOVX instruction in the same way as in the 8051. The AUX-RAM is **enabled** after a reset. Clearing the bit 4 in CHPCON register will disable the access to AUX-RAM. When executing from internal program memory, an access to AUX-RAM will not affect the Ports P0, P2, $\overline{WR}$ and $\overline{RD}$.

Example:

```
CHPENR    REG     F6H
CHPCON    REG     BFH
XRAMAH    REG     A1H

MOV     CHPENR, #87H
MOV     CHPENR, #59H
ORL     CHPCON, #00010000B  ; enable AUX-RAM
MOV     CHPENR, #00H
MOV     XRAMAH, #01H        ; internal high address
MOV     R0, #23H
MOV     A, #55H
MOVX    @R0, A              ; Write 55h data to 0123h AUX-RAM address.
MOV     XRAMAH, #02H
MOV     R1, #FFH            ; Read data from 02FFh AUX-RAM address.
MOVX    A, @R1
MOV     DPTR, #0134H
MOV     A, #78H
MOVX    @DPTR, A            ; Write 78h data to 0134h AUX-RAM address.
MOV     DPTR, #7FFFH
MOVX    A, @DPRT            ; Read data from the external 7FFFh address SRAM
```

6.6.1 Port Options Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	P0UP

Mnemonic: POR Address: 86H

P0UP: Enable Port 0 weak up. The pins of Port 0 can be configured with either the open drain or standard port with internal pull-up. By the default, Port 0 is an open drain bi-directional I/O port. When the P0UP bit in the POR register is set, the pins of port 0 will perform a bi-directional I/O port with internal pull-up that is structurally the same Port2.

6.6.2 $\overline{INT2}$ / $\overline{INT3}$

Two additional external interrupts, $\overline{INT2}$ and $\overline{INT3}$, whose functions are similar to those of external interrupt 0 and 1 in the standard 80C52. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 80C52. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB ($\overline{CLR}$) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON.

XICON - external interrupt control (C0H)

PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

PX3: External interrupt 3 priority high if set

EX3: External interrupt 3 enable if set

IE3: If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced

IT3: External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software

PX2: External interrupt 2 priority high if set

EX2: External interrupt 2 enable if set

IE2: If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced

IT2: External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

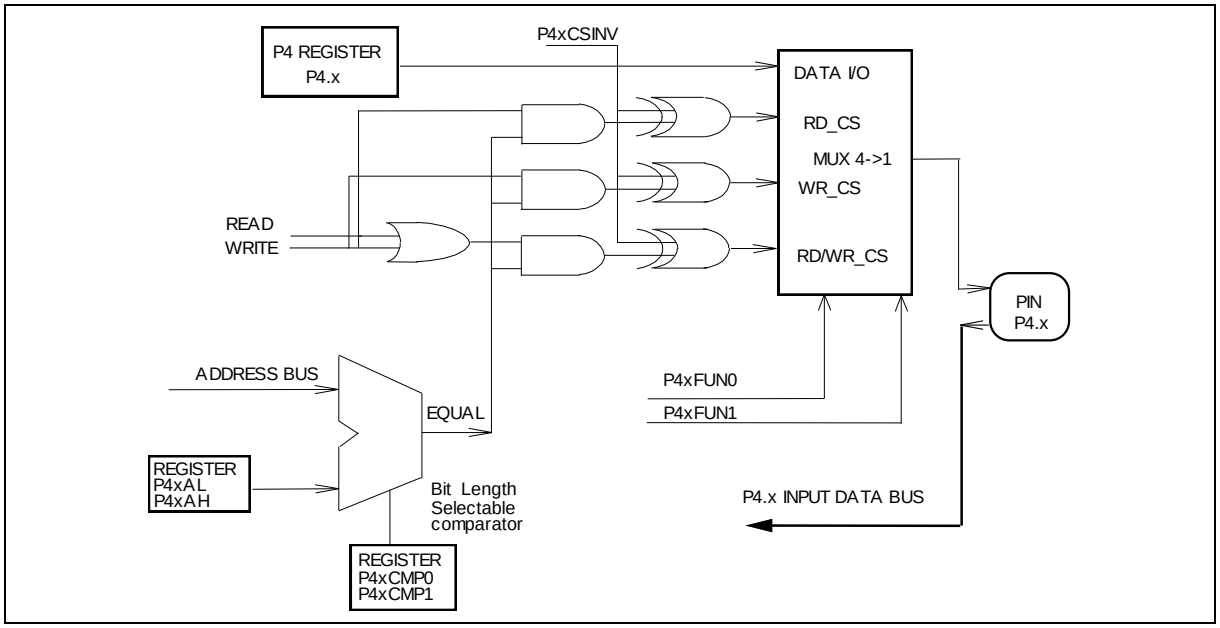
P4 (D8H)

BIT	NAME	FUNCTION
7	P47	I/O pin
6	P46	I/O pin.
5	P45	I/O pin.
4	P44	I/O pin.
3	P43	Port 4 Data bit which outputs to pin P4.3 at mode 0.
2	P42	Port 4 Data bit. which outputs to pin P4.2 at mode 0.
1	P41	Port 4 Data bit. which outputs to pin P4.1at mode 0.
0	P40	Port 4 Data bit which outputs to pin P4.0 at mode 0.

Here is an example to program the P4.0 as a write strobe signal at the I/O port address 1234H – 1237H and positive polarity, and P4.1 – P4.3 are used as general I/O ports.

```
MOV  P40AH, #12H
MOV  P40AL, #34H          ; Base I/O address 1234H for P4.0
MOV  P4CONA, #00001010B   ; P4.0 a write strobe signal and address line A0 and A1 are masked.
MOV  P4CONB, #00H         ; P4.1 – P4.3 as general I/O port which are the same as PORT1
MOV  P2ECON, #10H         ; Write the P40SINV = 1 to inverse the P4.0 write strobe polarity
                          ; default is negative.
```

Then any instruction MOVX @DPTR, A (with DPTR = 1234H – 1237H) will generate the positive polarity write strobe signal at pin P4.0. And the instruction MOV P4, #XX will output the bit3 to bit1 of data #XX to pin P4.3 – P4.1.



6.7 Pulse Width Modulated Outputs (PWM)

There are five pulse width modulated output channels to generate pulses of programmable length and interval. The repetition frequency is defined by an 8-bit prescaler PWMP, which supplies the clock for the counter. The prescaler and counter are common to both PWM channels. The 8-bit counter counts modular 255 (0 ~ 254). The value of the 8-bit counter compared to the contents of five registers: PWM0, PWM1, PWM2, PWM3 and PWM4. Provided the contents of either these registers is greater than the counter value, the corresponding PWM0, PWM1, PWM2, PWM3 or PWM4 output is set HIGH. If the contents of these registers are equal to, or less than the counter value, the output will be LOW. The pulse-width-ratio is defined by the contents of the registers PWM0, PWM1, PWM2, PWM3 and PWM4. The pulse-width-ratio is in the range of 0 to 1 and may be programmed in increments of 1/255. ENPWM0, ENPWM1, ENPWM2, ENPWM3 and ENPWM4 bit will enable or disable PWM output.

Buffered PWM outputs may be used to drive DC motors. The rotation speed of the motor would be proportional to the contents of PWM0/1/2/3/4. The repetition frequency f_{pwm}, at the PWM0/1/2/3/4 output is given by:

$$f_{pwm} = \frac{f_{osc}}{2 \times (1 + PWMP) \times 255}$$

Prescaler division factor = PWM + 1

PWMn high/low ratio of $\mathrm{PWMn} = \dfrac{(\mathrm{PWMn})}{255 - (\mathrm{PWMn})}$

This gives a repetition frequency range of 123 Hz to 31.4K Hz (f_{osc} = 16M Hz). By loading the PWM registers with either 00H or FFH, the PWM channels will output a constant HIGH or LOW level, respectively. Since the 8-bit counter counts modulo 255, it can never actually reach the value of the PWM registers when they are loaded with FFH.

When a compare register (PWM0, PWM1, PWM2, PWM3, PWM4) is loaded with a new value, the associated output updated immediately. It does not have to wait until the end of the current counter period. There is weakly pulled high on PWM output.

PWM4 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM4 Address: CFH

PWM Control 2 Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	PWM4OE	-	ENWPM4

Mnemonic: PWMCON2 Address: CEH

PWM4OE: Output enable for PWM4

ENPWM: Enable for PWM4

6.8 Watchdog Timer

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs, a system reset can also be caused if it is enabled. The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed. The Watchdog timer will de disabled on reset. In general, software should restart the Watchdog timer to put it into a known state. The control bits that support the Watchdog timer are discussed below.

Watchdog Timer Control Register

Bit:	7	6	5	4	3	2	1	0
	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0

Mnemonic: WDTC Address: 8FH

ENW : Enable watch-dog if set.

CLRW : Clear watch-dog timer and prescaler if set. This flag will be cleared automatically

WIDL : If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.

MODE	WFWIN	CTRL<3:0>	OEN	CEN	SFRAH, SFRAL	SFRFD
Erase 64KB APROM	0	0010	1	0	X	X
Program 64KB APROM	0	0001	1	0	Address in	Data in
Read 64KB APROM	0	0000	0	0	Address in	Data out
Erase 4KB LDROM	1	0010	1	0	X	X
Program 4KB LDROM	1	0001	1	0	Address in	Data in
Read 4KB LDROM	1	0000	0	0	Address in	Data out

6.9.1 In-System Programming Control Register (CHPCON)

CHPCON (BFH)

BIT	NAME	FUNCTION
7	SWRESET	When this bit is set to 1, and both FBOOTSL and FPROGEN are set to 1. It will enforce microcontroller reset to initial condition just like power on reset.
6	-	Reserve.
5	LD/AP	This bit is read only. 1: CPU is running LDROM program. 0: CPU is running APROM program.
4	ENAUXRAM	1: Enable on-chip AUX-RAM. 0: Disable the on-chip AUX-RAM
3	1	Must be 1
2	-	Reserve.
1	FBOOTSL	When this bit is set to 1, and both SWRESET and FPROGEN are set to 1. It will enforce microcontroller reset to initial condition just like power on reset.
0	FPROGEN	When this bit is set to 1, and both SWRESET and FBOOTSL are set to 1. It will enforce microcontroller reset to initial condition just like power on reset.

This register is protected by CHPENR register. Please write as below procedures while you would like to write CHPCON register.

```
Mov CHPENR, #87h
Mov CHPENR, #59h
Anl CHPCON, #EFh    ; Disable AUX-RAM
Mov CHPENR, #0h
```

6.10 Software Reset

Set CHPCON = 0X83, timer and enter IDLE mode. CPU will reset and restart from APFLASH after time out.

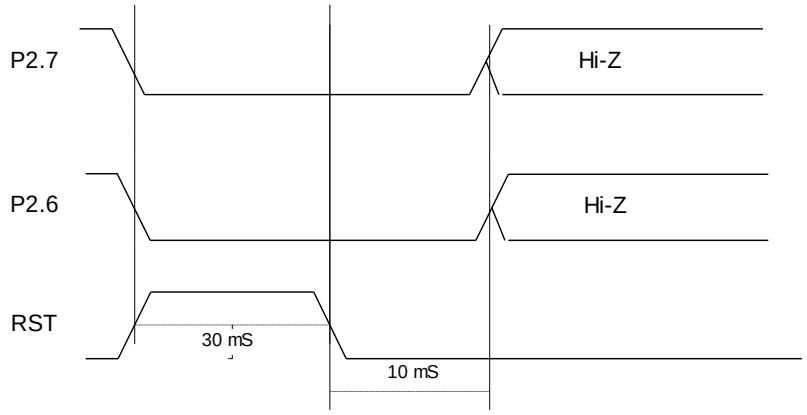
6.11 H/W Reboot Mode (Boot from LDROM)

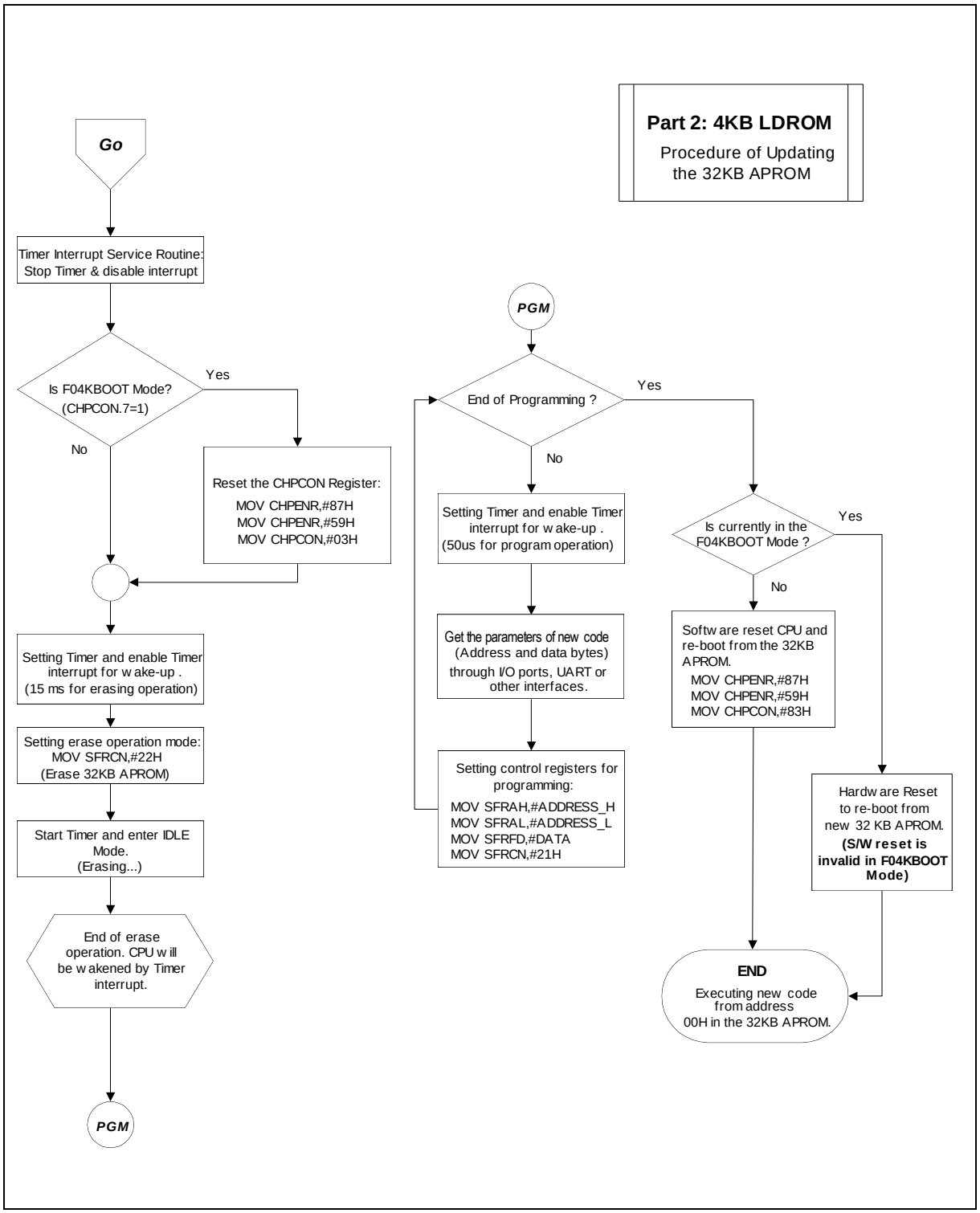
By default, the W78E365 boots from APROM program after a power on reset. On some occasions, user can force the W78E365 to boot from the LDROM program via following settings. The possible situation that you need to enter H/W REBOOT mode when the APROM program can not run properly and device can not jump back to LDROM to execute in-system programming function. Then you can use this H/W REBOOT mode to force the W78E365 jumps to LDROM and executes in-system programming procedure. When you design your system, you may reserve the pins P2.6, P2.7 to switches or jumpers. For example in a CD-ROM system, you can connect the P2.6 and P2.7 to PLAY and EJECT buttons on the panel. When the APROM program fails to execute the normal application program. User can press both two buttons at the same time and then turn on the power of the personal computer to force the W78E365 to enter the H/W REBOOT mode. After power on of personal computer, you can release both buttons and finish the in-system programming procedure to update the APROM code. In application system design, user must take care of the P2, P3, ALE, $\overline{EA}$ and $\overline{PSEN}$ pin value at reset to prevent from accidentally activating the programming mode or H/W REBOOT mode. It is necessary to add 10K resistor on these P2.6, P2.7 and P4.3 pins.

H/W Reboot Mode

P4.3	P2.7	P2.6	MODE
X	L	L	REBOOT
L	X	X	REBOOT

The Reset Timing For Entering F04KBOOT Mode




Part 2: 4KB LDROM
Procedure of Updating the 32KB APROM
Go
Timer Interrupt Service Routine: Stop Timer & disable interrupt
Is F04KBOOT Mode? (CHPCON.7=1)
Yes
No
Reset the CHPCON Register:
MOV CHPENR,#87H
MOV CHPENR,#59H
MOV CHPCON,#03H
Setting Timer and enable Timer interrupt for w ake-up . (15 ms for erasing operation)
Setting erase operation mode: MOV SFRCN,#22H (Erase 32KB APROM)
Start Timer and enter IDLE Mode. (Erasing...)
End of erase operation. CPU w ill be w akened by Timer interrupt.
PGM
PGM
End of Programming ?
Yes
No
Setting Timer and enable Timer interrupt for w ake-up . (50us for program operation)
Get the parameters of new code (Address and data bytes) through I/O ports, UART or other interfaces.
Setting control registers for programming:
MOV SFRAH,#ADDRESS_H
MOV SFRAL,#ADDRESS_L
MOV SFRFD,#DATA
MOV SFRCN,#21H
Is currently in the F04KBOOT Mode ?
Yes
No
Softw are reset CPU and re-boot from the 32KB APROM.
MOV CHPENR,#87H
MOV CHPENR,#59H
MOV CHPCON,#83H
Hardw are Reset to re-boot from new 32 KB APROM.
(S/W reset is invalid in F04KBOOT Mode)
END
Executing new code from address 00H in the 32KB APROM.

7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+6.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{ST}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7.2 D.C. Characteristics

(V_{DD} – V_{SS}= 5V ±10%, T_A = 25°C, Fosc = 20 MHz, unless otherwise specified.)

SYMBOL	PARAMETER	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
V_{DD}	Operating Voltage	4.5	5.5	V	RST = 1, P0 = V_{DD}
I_{DD}	Operating Current	-	20	mA	No load V_{DD} = 5.5V
I_{IDLE}	Idle Current	-	6	mA	Idle mode V_{DD} = 5.5V
I_{PWDN}	Power Down Current	-	10	µA	Power-down mode V_{DD} = 5.5V
I_{IN1}	Input Current P1, P2, P3, P4	-50	+10	µA	V_{DD} = 5.5V V_{IN} = 0V or V_{DD}
I_{IN2}	Input Current RST	-10	+300	µA	V_{DD} = 5.5V 0<V_{IN}<V_{DD}
I_{LK}	Input Leakage Current P0, $\overline{EA}$	-10	+10	µA	V_{DD} = 5.5V 0V<V_{IN}<V_{DD}
I_{TL} [*4]	Logic 1 to 0 Transition Current P1, P2, P3, P4	-500	-200	µA	V_{DD} = 5.5V V_{IN} = 2.0V
VIL1	Input Low Voltage P0, P1, P2, P3, P4, $\overline{EA}$	0	0.8	V	VDD = 4.5V
V IL2	Input Low Voltage RST	0	0.8	V	VDD = 4.5V

D.C. Characteristics, continued

SYMBOL	PARAMETER	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
V_{IL3}	Input Low Voltage XTAL1[*4]	0	0.8	V	V_{DD} = 4.5V
V_{IH1}	Input High Voltage P0, P1, P2, P3, P4, $\overline{EA}$	2.4	V_{DD} +0.2	V	V_{DD} = 5.5V
V_{IH2}	Input High Voltage RST	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
V_{IH3}	Input High Voltage XTAL1[*4]	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
V_{OL1}	Output Low Voltage P1, P2, P3, P4	-	0.45	V	V_{DD} = 4.5V I_{OL} = +2 mA
V_{OL2}	Output Low Voltage P0, ALE, $\overline{PSEN}$ [*3]	-	0.45	V	V_{DD} = 4.5V I_{OL} = +4 mA
Isk1	Sink current P1, P3, P4	4	8	mA	V_{DD} = 4.5V VOL = 0.45V
Isk2	Sink current P0, P2, ALE, $\overline{PSEN}$	10	14	mA	V_{DD}=4.5V VOL = 0.45V
V_{OH1}	Output High Voltage P1, P2, P3, P4	2.4	-	V	V_{DD} = 4.5V I_{OH} = -100 μA
V_{OH2}	Output High Voltage P0, ALE, $\overline{PSEN}$ [*3]	2.4	-	V	V_{DD} = 4.5V I_{OH} = -400 μA
Isr1	Source current P1, P2, P3, P4	-120	-180	μA	V_{DD} = 4.5V VOH = 2.4V
Isr2	Source current P0, P2, ALE, $\overline{PSEN}$	-10	-14	mA	V_{DD} =4.5V VOH = 2.4V

Notes:

*1. RST pin is a Schmitt trigger input.

*2. P0, ALE and $\overline{PSEN}$ are tested in the external access mode.

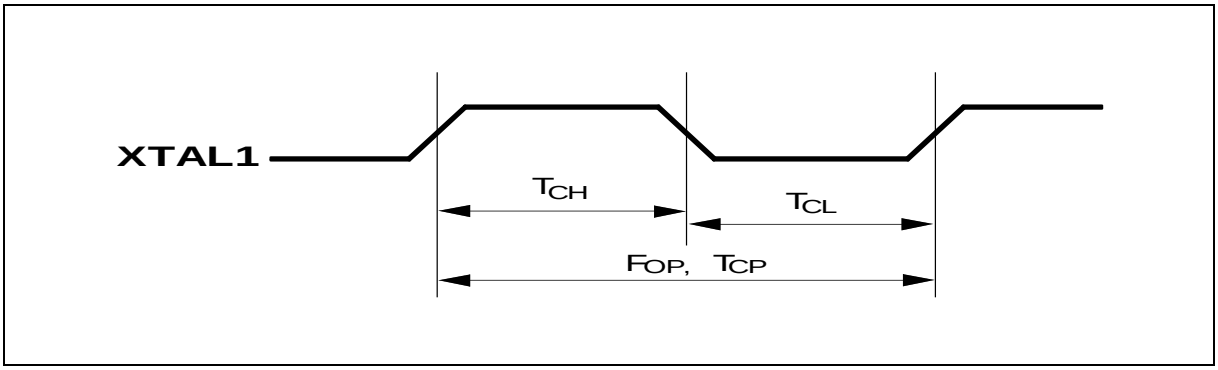
*3. XTAL1 is a CMOS input.

*4. Pins of P1, P2, P3, P4 can source a transition current when they are being externally driven from 1 to 0.

7.3 A.C. Characteristics

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (T_{CP}), and actual parts will usually experience less than a ±20 nS variation.

Clock Input Waveform

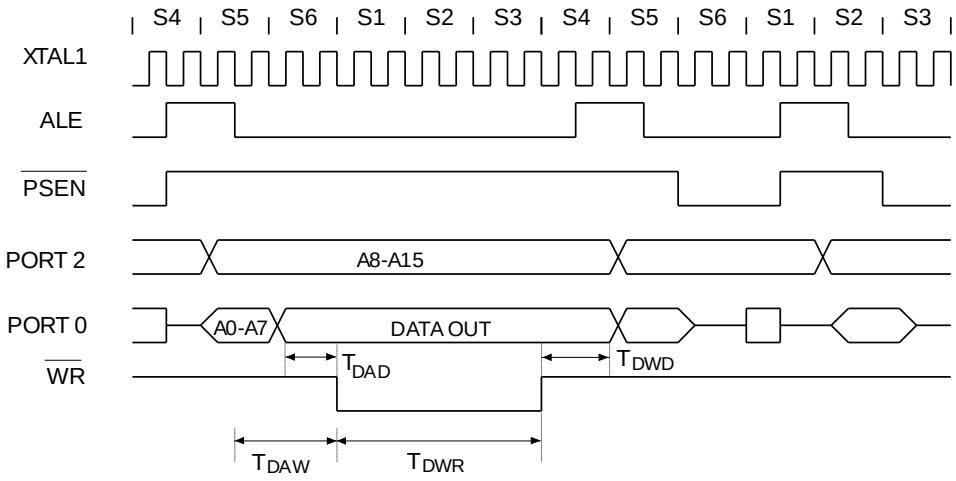


PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	F_{OP}	0	-	40	MHz	1
Clock Period	T_{CP}	25	-	-	nS	2
Clock High	T_{CH}	20	-	-	nS	3
Clock Low	T_{CL}	20	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.
2. The T_{CP} specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

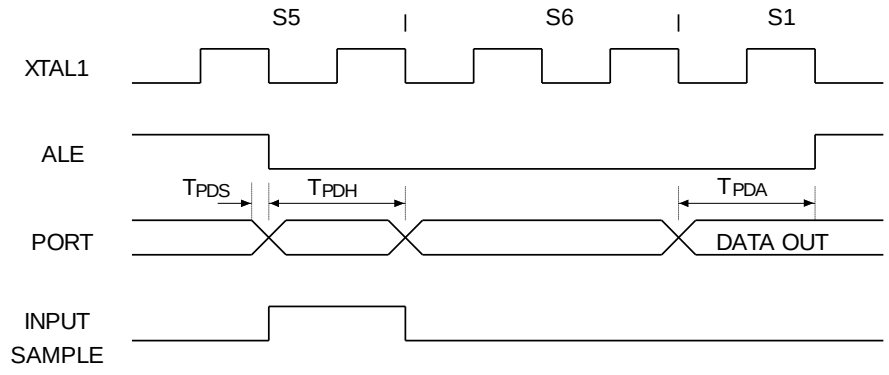
8.3 Data Write Cycle



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{WR}$ Low	TDAW	3 TCP-Δ	-	3 TCP+Δ	nS
Data Valid to $\overline{WR}$ Low	TDAD	1 TCP-Δ	-	-	nS
Data Hold from $\overline{WR}$ High	TDWD	1 TCP-Δ	-	-	nS
$\overline{WR}$ Pulse Width	TDWR	6 TCP-Δ	6 TCP	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

8.4 Port Access Cycle



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	TPDS	1 TCP	-	-	nS
Port Input Hold from ALE Low	TPDH	0	-	-	nS
Port Output to ALE	TPDA	1 TCP	-	-	nS

Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

9. TYPICAL APPLICATION CIRCUIT

9.1 External Program Memory and Crystal

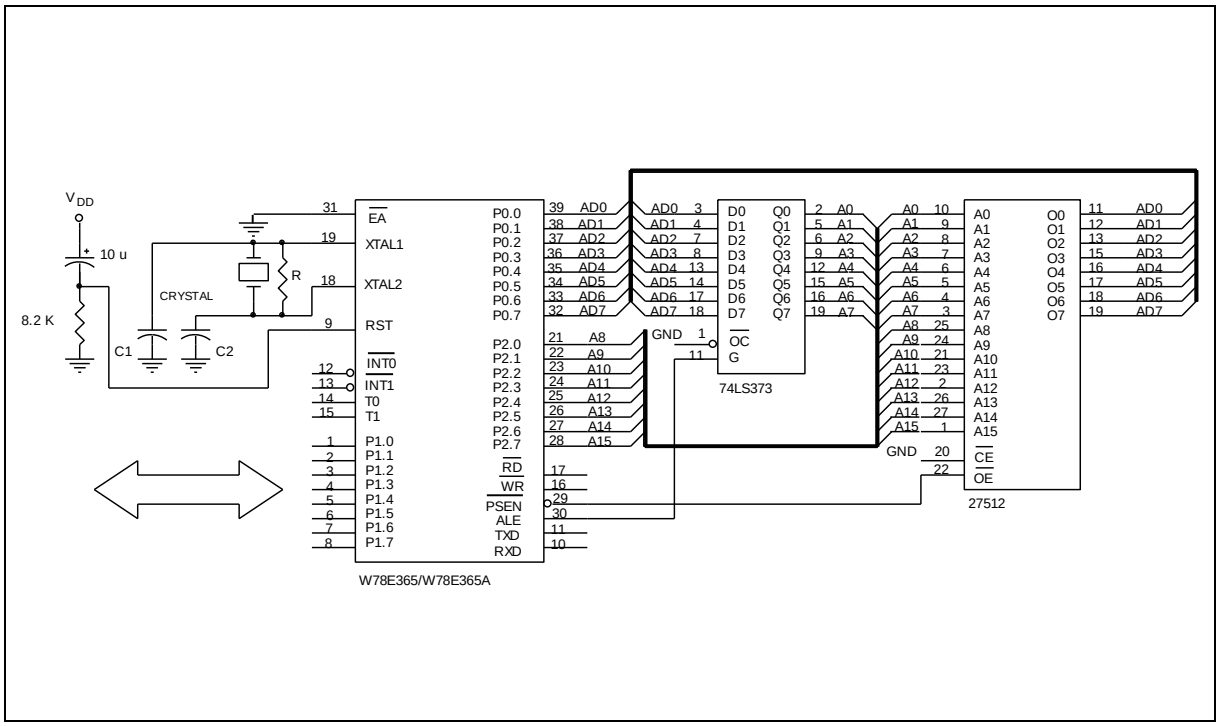


Figure A

CRYSTAL	C1	C2	R
6 MHz	47P	47P	-
16 MHz	30P	30P	-
24 MHz	15P	15P	-
32 MHz	10P	10P	6.8K
40 MHz	5P	5P	4.7K

Above table shows the reference values for crystal applications.

Notes:

1. C1, C2, R components refer to Figure A
2. Crystal layout must get close to XTAL1 and XTAL2 pins on user's application board.

Typical Application Circuit, continued

11. APPLICATION NOTE

11.1 In-system Programming Software Examples

This application note illustrates the in-system programmability of the Nuvoton W78E365 ROM microcontroller. In this example, microcontroller will boot from 64KB APROM bank and waiting for a key to enter in-system programming mode for re-programming the contents of 64KB APROM. While entering in-system programming mode, microcontroller executes the loader program in 4KB LDROM bank. The loader program erases the 64KB APROM then reads the new code data from external SRAM buffer (or through other interfaces) to update the 64KB APROM.

Example 1:

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;*****************************************************************************************************************
;* Example of 64K APROM program: Program will scan the P1.0. if P1.0 = 0, enters in-system
;* programming mode for updating the content of APROM code else executes the current ROM code.
;* XTAL = 16 MHz
;*****************************************************************************************************************
        .chip 8052
        .RAMCHK OFF
        .symbols

        CHPCON    EQU     BFH
        CHPENR    EQU     F6H
        SFRAL     EQU     C4H
        SFRAH     EQU     C5H
        SFRFD     EQU     C6H
        SFRCN     EQU     C7H

        ORG     0H
        LJMP    100H                    ; JUMP TO MAIN PROGRAM
    ;*************************************************************************
    ;*  TIMER0 SERVICE VECTOR ORG = 000BH
    ;*************************************************************************
        ORG     00BH
        CLR     TR0                     ; TR0 = 0, STOP TIMER0
        MOV     TL0, R6
        MOV     TH0, R7
        RETI
    ;*************************************************************************
    ;*  64K APROM MAIN PROGRAM
    ;*************************************************************************
       ORG 100H

MAIN_64K:
        MOV A,P1                        ; SCAN P1.0
        ANL A, #01H
        CJNE A, #01H,PROGRAM_64K ; IF P1.0 = 0, ENTER IN-SYSTEM PROGRAMMING MODE
        JMP NORMAL_MODE

PROGRAM_64K:
        MOV CHPENR, #87H                ; CHPENR = 87H, CHPCON REGISTER WRTE ENABLE
        MOV CHPENR, #59H                ; CHPENR = 59H, CHPCON REGISTER WRITE ENABLE
        MOV CHPCON, #03H                ; CHPCON = 03H, ENTER IN-SYSTEM PROGRAMMING MODE
        MOV TCON, #00H                  ; TR = 0 TIMER0 STOP
```

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;*****************************************************************************
;*  4KB LDROM MAIN PROGRAM
;*****************************************************************************
        ORG 100H
MAIN_4K:
        MOV SP, #C0H
        MOV CHPENR, #87H      ; CHPENR = 87H, CHPCON WRITE ENABLE.
        MOV CHPENR, #59H      ; CHPENR = 59H, CHPCON WRITE ENABLE.
        MOV CHPCON, #03H      ; CHPCON = 03H, ENABLE IN-SYSTEM PROGRAMMING.
        MOV CHPENR, #00H      ; DISABLE CHPCON WRITE ATTRIBUTE

        MOV TCON, #00H        ; TCON = 00H, TR = 0 TIMER0 STOP
        MOV TMOD, #01H        ; TMOD = 01H, SET TIMER0 A 16BIT TIMER
        MOV IP, #00H          ; IP = 00H
        MOV IE, #82H          ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV R6, #F0H
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV TCON, #10H        ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H        ; ENTER IDLE MODE

UPDATE_64K:
        MOV TCON, #00H        ; TCON = 00H, TR = 0 TIM0 STOP
        MOV IP, #00H          ; IP = 00H
        MOV IE, #82H          ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV TMOD, #01H        ; TMOD = 01H, MODE1
        MOV R6, #E0H          ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15 mS. DEPENDING
                              ; ON USER'S SYSTEM CLOCK RATE.
        MOV R7, #B1H
        MOV TL0, R6
        MOV TH0, R7

ERASE_P_4K:
        MOV SFRCN, #22H     ; SFRCN(C7H) = 22H  ERASE 64K
        MOV TCON, #10H      ; TCON = 10H, TR0 = 1,GO
        MOV PCON, #01H      ; ENTER IDLE MODE (FOR ERASE OPERATION)

;*****************************************************************************
;* BLANK CHECK
;*****************************************************************************
        MOV SFRCN, #0H      ; READ 64KB APROM MODE
        MOV SFRAH, #0H      ; START ADDRESS = 0H
        MOV SFRAL, #0H
        MOV R6, #FEH        ; SET TIMER FOR READ OPERATION, ABOUT 1.5 μS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7

BLANK_CHECK_LOOP:
        SETB TR0            ; ENABLE TIMER 0
        MOV PCON, #01H      ; ENTER IDLE MODE
        MOV A, SFRFD        ; READ ONE BYTE
        CJNE A, #FFH, BLANK_CHECK_ERROR
        INC SFRAL           ; NEXT ADDRESS
        MOV A, SFRAL
```

12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	May, 2003	-	Initial Issued
A2	August, 2004	32	Revise title of 9.1
A3	Sep. 14, 2004	2	Remove P4.4 ~ P4.7
A4	Dec. 23, 2004	2, 15	Add PWM in feature list and modify PWM block diagram
A5	April 20, 2005	41	Add Important Notice
A6	June 22, 2005	3 33	Add lead free(RoHS) part number Add 32M/40Mhz items in the table
A7	Aug. 25, 2005	3, 5	Add Port 0 pull-up resisters information
A8	Dec 4, 2006	3	Remove all Leaded package parts
A9	January 10, 2007	3 4 37	Add 48-pin LQFP part. Add 48-pin LQFP package Add 48-pin LQFP package dimension
A10	April 22, 2008	10	Modified P3 reset state
A11	July 15, 2008	7	Revise typo Incorrect: AUX-RAM is enable after a reset Correct: AUX-RAM is disabled after a reset
A12	January 12, 2009	7 10	Revise typo, on-chip AUX-RAM is enabled after a reset. (Ver A11 is incorrect) Revise CHPCON initial value from 0xx00000b to 00x11000b.