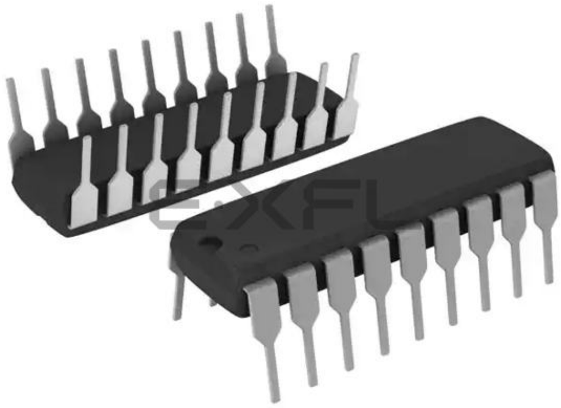

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	6KB (6K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj06gs101-e-p

dsPIC33FJ06GS101/X02 AND dsPIC33FJ16GSX02/X04 PRODUCT FAMILIES

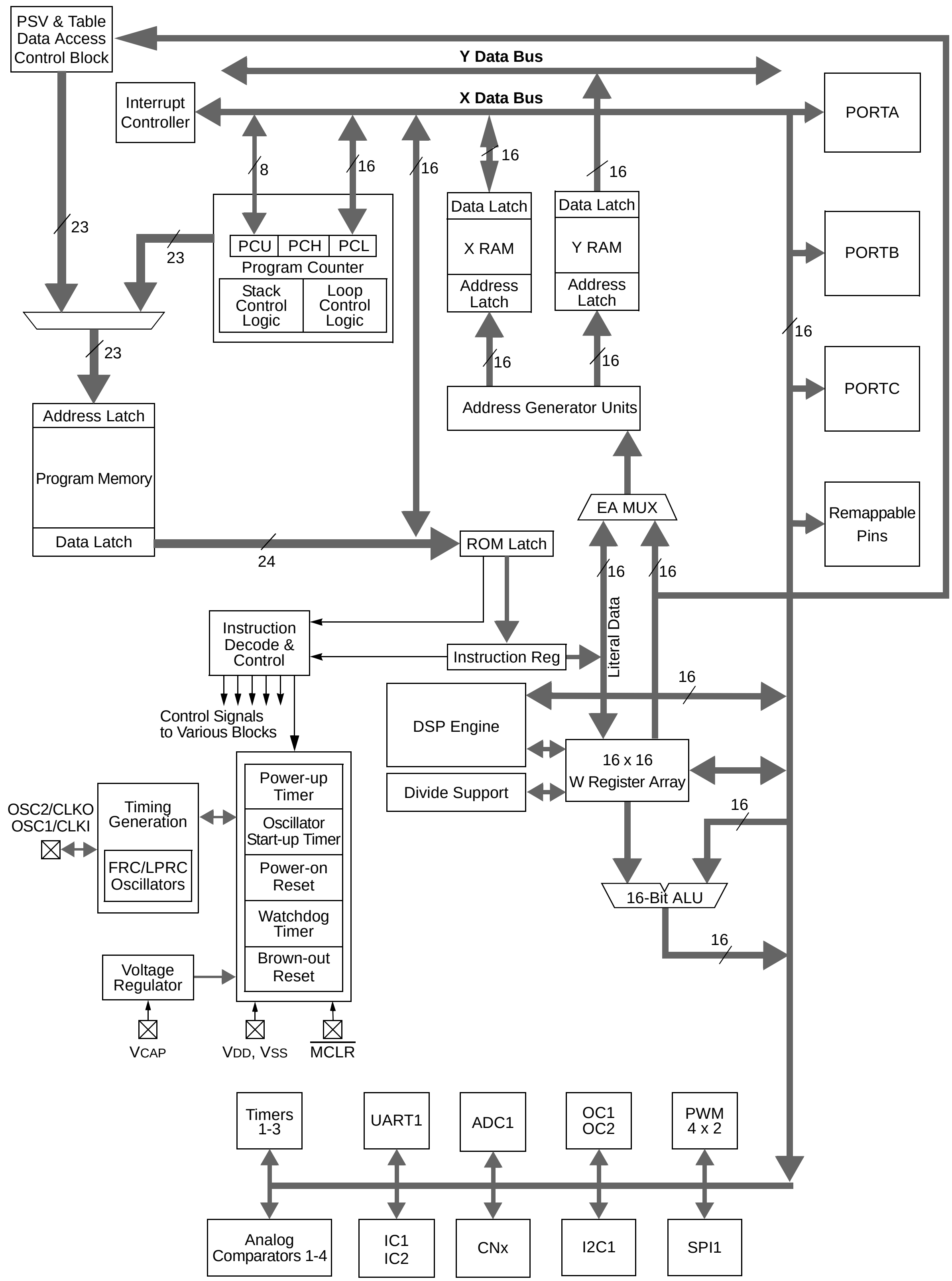
The device names, pin counts, memory sizes and peripheral availability of each device are listed below. The following pages show their pinout diagrams.

TABLE 1: dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 CONTROLLER FAMILIES

Device	Pins	Program Flash Memory (Kbytes)	RAM (Bytes)	Remappable Peripherals									DAC Output	I^2C^{TM}	ADC			I/O Pins	Packages
				Remappable Pins	16-Bit Timer	Input Capture	Output Compare	UART	SPI	PWM(2)	Analog Comparator	External Interrupts(3)			SARs	Sample-and-Hold (S&H) Circuit	Analog-to-Digital Inputs		
dsPIC33FJ06GS101	18	6	256	8	2	0	1	1	1	2x2(1)	0	3	0	1	1	3	6	13	SOIC
dsPIC33FJ06GS102	28	6	256	16	2	0	1	1	1	2x2	0	3	0	1	1	3	6	21	SPDIP, SOIC, QFN-S
dsPIC33FJ06GS202	28	6	1K	16	2	1	1	1	1	2x2	2	3	1	1	1	3	6	21	SPDIP, SOIC, QFN-S
dsPIC33FJ16GS402	28	16	2K	16	3	2	2	1	1	3x2	0	3	0	1	1	4	8	21	SPDIP, SOIC, QFN-S
dsPIC33FJ16GS404	44	16	2K	30	3	2	2	1	1	3x2	0	3	0	1	1	4	8	35	QFN, TQFP, VTLA
dsPIC33FJ16GS502	28	16	2K	16	3	2	2	1	1	4x2(1)	4	3	1	1	2	6	8	21	SPDIP, SOIC, QFN-S, UQFN
dsPIC33FJ16GS504	44	16	2K	30	3	2	2	1	1	4x2(1)	4	3	1	1	2	6	12	35	QFN, TQFP, VTLA

Note 1: The PWM4H:PWM4L pins are remappable.
2: The PWM Fault pins and PWM synchronization pins are remappable.
3: Only two out of three interrupts are remappable.

FIGURE 1-1: dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 BLOCK DIAGRAM



Note: Not all pins or features are implemented on all device pinout configurations. See pinout diagrams for the specific pins and features present on each device.

3.6.1 MULTIPLIER

The 17-bit x 17-bit multiplier is capable of signed or unsigned operation and can multiplex its output using a scaler to support either 1.31 fractional (Q31) or 32-bit integer results. Unsigned operands are zero-extended into the 17th bit of the multiplier input value. Signed operands are sign-extended into the 17th bit of the multiplier input value. The output of the 17-bit x 17-bit multiplier/scaler is a 33-bit value that is sign-extended to 40 bits. Integer data is inherently represented as a signed 2's complement value, where the Most Significant bit (MSb) is defined as a sign bit. The range of an N-bit 2's complement integer is -2^{N-1} to $2^{N-1} – 1$.

- For a 16-bit integer, the data range is -32768 (0x8000) to 32767 (0x7FFF), including 0.
- For a 32-bit integer, the data range is -2,147,483,648 (0x8000 0000) to 2,147,483,647 (0x7FFF FFFF).

When the multiplier is configured for fractional multiplication, the data is represented as a 2's complement fraction, where the MSb is defined as a sign bit and the radix point is implied to lie just after the sign bit (QX format). The range of an N-bit 2's complement fraction with this implied radix point is -1.0 to $(1 – 2^{1-N})$. For a 16-bit fraction, the Q15 data range is -1.0 (0x8000) to 0.999969482 (0x7FFF) including 0 and has a precision of 3.01518×10^{-5}. In Fractional mode, the 16 x 16 multiply operation generates a 1.31 product that has a precision of 4.65661×10^{-10}.

The same multiplier is used to support the MCU multiply instructions, which include integer 16-bit signed, unsigned and mixed sign multiply operations.

The `MUL` instruction can be directed to use byte or word-sized operands. Byte operands will direct a 16-bit result, and word operands will direct a 32-bit result to the specified register(s) in the W array.

3.6.2 DATA ACCUMULATORS AND ADDER/SUBTRACTER

The data accumulator consists of a 40-bit adder/subtracter with automatic sign extension logic. It can select one of two accumulators (A or B) as its pre-accumulation source and post-accumulation destination. For the `ADD` and `LAC` instructions, the data to be accumulated or loaded can be optionally scaled using the barrel shifter prior to accumulation.

3.6.2.1 Adder/Subtracter, Overflow and Saturation

The adder/subtracter is a 40-bit adder with an optional zero input into one side, and either true or complement data into the other input.

- In the case of addition, the Carry/$\overline{\text{Borrow}}$ input is active-high and the other input is true data (not complemented).
- In the case of subtraction, the Carry/$\overline{\text{Borrow}}$ input is active-low and the other input is complemented.

The adder/subtracter generates Overflow Status bits, SA/SB and OA/OB, which are latched and reflected in the STATUS Register:

- Overflow from bit 39: this is a catastrophic overflow in which the sign of the accumulator is destroyed.
- Overflow into guard bits, 32 through 39: this is a recoverable overflow. This bit is set whenever all the guard bits are not identical to each other.

The adder has an additional saturation block that controls accumulator data saturation, if selected. It uses the result of the adder, the Overflow Status bits described previously and the SAT<A:B> (CORCON<7:6>) and ACCSAT (CORCON<4>) mode control bits to determine when and to what value to saturate.

Six STATUS Register bits support saturation and overflow:

- OA: ACCA overflowed into guard bits
- OB: ACCB overflowed into guard bits
- SA: ACCA saturated (bit 31 overflow and saturation)
  or
  ACCA overflowed into guard bits and saturated (bit 39 overflow and saturation)
- SB: ACCB saturated (bit 31 overflow and saturation)
  or
  ACCB overflowed into guard bits and saturated (bit 39 overflow and saturation)
- OAB: Logical OR of OA and OB
- SAB: Logical OR of SA and SB

The OA and OB bits are modified each time data passes through the adder/subtracter. When set, they indicate that the most recent operation has overflowed into the accumulator guard bits (bits 32 through 39). The OA and OB bits can also optionally generate an arithmetic warning trap when set and the corresponding Overflow Trap Flag Enable bits (OVATE, OVBTE) in the INTCON1 register are set (refer to **Section 7.0 "Interrupt Controller"**). This allows the user application to take immediate action, for example, to correct system gain.

TABLE 4-37: PORTA REGISTER MAP

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	02C0	—	—	—	—	—	—	—	—	—	—	—	TRISA<4:0>					001F
PORTA	02C2	—	—	—	—	—	—	—	—	—	—	—	RA<4:0>					xxxx
LATA	02C4	—	—	—	—	—	—	—	—	—	—	—	LATA<4:0>					0000
ODCA	02C6	—	—	—	—	—	—	—	—	—	—	—	ODCA<4:3>		—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-38: PORTB REGISTER MAP FOR dsPIC33FJ06GS101

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	—	—	—	—	—	—	—	—	TRISB<7:0>								00FF
PORTB	02CA	—	—	—	—	—	—	—	—	RB<7:0>								xxxx
LATB	02CC	—	—	—	—	—	—	—	—	LATB<7:0>								0000
ODCB	02CE	—	—	—	—	—	—	—	—	ODCB<7:6>		—	ODCB4	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-39: PORTB REGISTER MAP FOR dsPIC33FJ06GS102, dsPIC33FJ06GS202, dsPIC33FJ16GS402, dsPIC33FJ16GS404, dsPIC33FJ16GS502 AND dsPIC33FJ16GS504

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	TRISB<15:0>																FFFF
PORTB	02CA	RB<15:0>																xxxx
LATB	02CC	LATB<15:0>																0000
ODCB	02CE	ODCB<15:11>					—	—	ODCB<8:6>			—	ODCB4(1)	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: This bit is not available on dsPIC33FJ06GS202/502 devices.

TABLE 4-40: PORTC REGISTER MAP FOR dsPIC33FJ16GS404 AND dsPIC33FJ16GS504

SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	02D0	—	—	TRISC<13:0>														3FFF
PORTC	02D2	—	—	RC<13:0>														xxxx
LATC	02D4	—	—	LATC<13:0>														0000
ODCC	02D6	—	—	ODCC<13:11>			—	—	ODCC<8:3>						—	—	ODCC0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-41: SYSTEM CONTROL REGISTER MAP

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	—	—	—	—	CM	VREGS	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	xxxx[1]
OSCCON	0742	—	COSC2	COSC1	COSC0	—	NOSC2	NOSC1	NOSC0	CLKLOCK	IOLOCK	LOCK	—	CF	—	—	OSWEN	0300[2]
CLKDIV	0744	ROI	DOZE2	DOZE1	DOZE0	DOZEN	FRCDIV2	FRCDIV1	FRCDIV0	PLLPOST1	PLLPOST0	—	PLLPRE4	PLLPRE3	PLLPRE2	PLLPRE1	PLLPRE0	3040
PLLFBD	0746	—	—	—	—	—	—	—	PLLDIV<8:0>									0030
REFOCON	074E	ROON	—	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0	—	—	—	—	—	—	—	—	0000
OSCTUN	0748	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000
ACLKCON	0750	ENAPLL	APLLCK	SELACLK	—	—	APSTSCLR2	APSTSCLR1	APSTSCLR0	ASRCSEL	FRCSEL	—	—	—	—	—	—	2300

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The RCON register Reset values are dependent on the type of Reset.

2: The OSCCON register Reset values are dependent on the FOSCx Configuration bits and on type of Reset.

TABLE 4-42: NVM REGISTER MAP

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0760	WR	WREN	WRERR	—	—	—	—	—	—	ERASE	—	—	NVMOP3	NVMOP2	NVMOP1	NVMOP0	0000[1]
NVMKEY	0766	—	—	—	—	—	—	—	—	NVMKEY<7:0>								0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset value shown is for POR only. The value on other Reset states is dependent on the state of memory write or erase operations at the time of Reset.

TABLE 4-43: PMD REGISTER MAP FOR dsPIC33FJ06GS101 DEVICES ONLY

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	—	—	—	T2MD	T1MD	—	PWMMD	—	I2C1MD	—	U1MD	—	SPI1MD	—	—	ADCMD	0000
PMD2	0772	—	—	—	—	—	—	IC2MD	IC1MD	—	—	—	—	—	—	OC2MD	OC1MD	0000
PMD3	0774	—	—	—	—	—	CMPMD	—	—	—	—	—	—	—	—	—	—	0000
PMD4	0776	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	—	—	—	0000
PMD6	077A	—	—	—	—	PWM4MD	—	—	PWM1MD	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-44: PMD REGISTER MAP FOR dsPIC33FJ06GS102 DEVICES ONLY

File Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	—	—	—	T2MD	T1MD	—	PWMMD	—	I2C1MD	—	U1MD	—	SPI1MD	—	—	ADCMD	0000
PMD2	0772	—	—	—	—	—	—	IC2MD	IC1MD	—	—	—	—	—	—	OC2MD	OC1MD	0000
PMD3	0774	—	—	—	—	—	CMPMD	—	—	—	—	—	—	—	—	—	—	0000
PMD4	0776	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	—	—	—	0000
PMD6	077A	—	—	—	—	—	—	PWM2MD	PWM1MD	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

FIGURE 4-8: BIT-REVERSED ADDRESS EXAMPLE

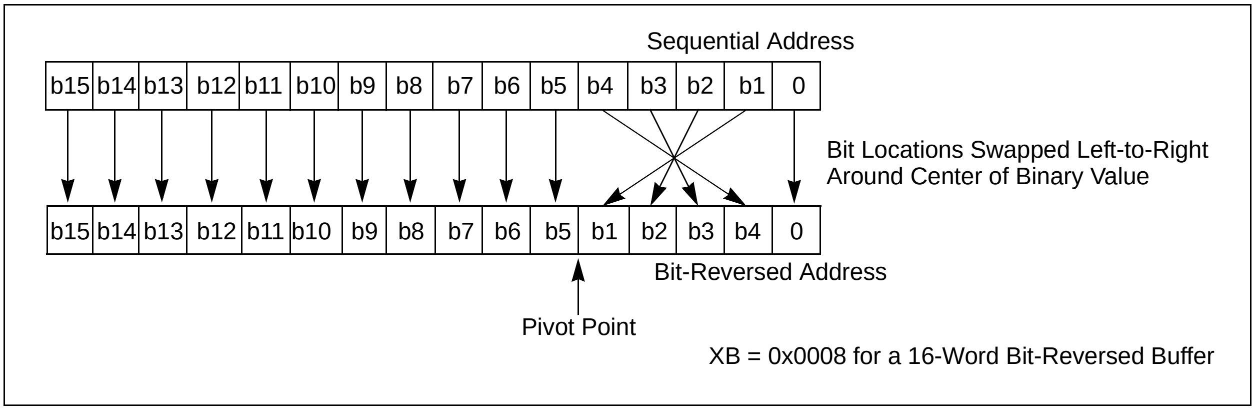


TABLE 4-49: BIT-REVERSED ADDRESS SEQUENCE (16-ENTRY)

Normal Address					Bit-Reversed Address				
A3	A2	A1	A0	Decimal	A3	A2	A1	A0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	8
0	0	1	0	2	0	1	0	0	4
0	0	1	1	3	1	1	0	0	12
0	1	0	0	4	0	0	1	0	2
0	1	0	1	5	1	0	1	0	10
0	1	1	0	6	0	1	1	0	6
0	1	1	1	7	1	1	1	0	14
1	0	0	0	8	0	0	0	1	1
1	0	0	1	9	1	0	0	1	9
1	0	1	0	10	0	1	0	1	5
1	0	1	1	11	1	1	0	1	13
1	1	0	0	12	0	0	1	1	3
1	1	0	1	13	1	0	1	1	11
1	1	1	0	14	0	1	1	1	7
1	1	1	1	15	1	1	1	1	15

5.4.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

One row of program Flash memory can be programmed at a time. To achieve this, it is necessary to erase the 8-row erase page that contains the desired row. The general process is:

1. Read eight rows of program memory (512 instructions) and store in data RAM.
2. Update the program data in RAM with the desired new data.
3. Erase the block (see Example 5-1):
    a) Set the NVMOP<3:0> bits (NVMCON<3:0>) to '`0010`' to configure for block erase. Set the ERASE (NVMCON<6>) and WREN (NVMCON<14>) bits.
    b) Write the starting address of the page to be erased into the TBLPAG and W registers.
    c) Write 0x55 to NVMKEY.
    d) Write 0xAA to NVMKEY.
    e) Set the WR bit (NVMCON<15>). The erase cycle begins and the CPU stalls for the duration of the erase cycle. When the erase is done, the WR bit is cleared automatically.
4. Write the first 64 instructions from data RAM into the program memory buffers (see Example 5-2).
5. Write the program block to Flash memory:
    a) Set the NVMOP<3:0> bits to '`0001`' to configure for row programming. Clear the ERASE bit and set the WREN bit.
    b) Write 0x55 to the NVMKEY register.
    c) Write 0xAA to the NVMKEY register.
    d) Set the WR bit. The programming cycle begins and the CPU stalls for the duration of the write cycle. When the write to Flash memory is done, the WR bit is cleared automatically.
6. Repeat Steps 4 and 5, using the next available 64 instructions from the block in data RAM by incrementing the value in the TBLPAG register, until all 512 instructions are written back to Flash memory.

For protection against accidental operations, the write initiate sequence for the NVMKEY register must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be `NOP`s, as shown in Example 5-3.

EXAMPLE 5-1: ERASING A PROGRAM MEMORY PAGE

```
; Set up NVMCON for block erase operation
       MOV     #0x4042, W0                 ;
       MOV     W0, NVMCON                  ; Initialize NVMCON
; Init pointer to row to be ERASED
       MOV     #tblpage(PROG_ADDR), W0     ;
       MOV     W0, TBLPAG                  ; Initialize PM Page Boundary SFR
       MOV     #tbloffset(PROG_ADDR), W0   ; Initialize in-page EA[15:0] pointer
       TBLWTL  W0, [W0]                    ; Set base address of erase block
       DISI    #5                          ; Block all interrupts with priority <7
                                           ; for next 5 instructions
       MOV     #0x55, W0
       MOV     W0, NVMKEY                  ; Write the 55 key
       MOV     #0xAA, W1                   ;
       MOV     W1, NVMKEY                  ; Write the AA key
       BSET    NVMCON, #WR                 ; Start the erase sequence
       NOP                                 ; Insert two NOPs after the erase
       NOP                                 ; command is asserted
```

REGISTER 7-16: IEC5: INTERRUPT ENABLE CONTROL REGISTER 5

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
PWM2IE	PWM1IE	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **PWM2IE:** PWM2 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 14 **PWM1IE:** PWM1 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13-0 **Unimplemented:** Read as ‘0’

REGISTER 10-22: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP15R5	RP15R4	RP15R3	RP15R2	RP15R1	RP15R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP14R5	RP14R4	RP14R3	RP14R2	RP14R1	RP14R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14	**Unimplemented:** Read as ‘0’
bit 13-8	**RP15R<5:0>:** Peripheral Output Function is Assigned to RP15 Output Pin bits (see Table 10-2 for peripheral function numbers)
bit 7-6	**Unimplemented:** Read as ‘0’
bit 5-0	**RP14R<5:0>:** Peripheral Output Function is Assigned to RP14 Output Pin bits (see Table 10-2 for peripheral function numbers)

Note 1: This register is not implemented in the dsPIC33FJ06GS101 device.

REGISTER 10-23: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP17R5	RP17R4	RP17R3	RP17R2	RP17R1	RP17R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP16R5	RP16R4	RP16R3	RP16R2	RP16R1	RP16R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14	**Unimplemented:** Read as ‘0’
bit 13-8	**RP17R<5:0>:** Peripheral Output Function is Assigned to RP17 Output Pin bits (see Table 10-2 for peripheral function numbers)
bit 7-6	**Unimplemented:** Read as ‘0’
bit 5-0	**RP16R<5:0>:** Peripheral Output Function is Assigned to RP16 Output Pin bits (see Table 10-2 for peripheral function numbers)

Note 1: This register is implemented in the dsPIC33FJ16GS404 and dsPIC33FJ16GS504 devices only.

The Timer2/3 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (F_{CY}). In Synchronous Counter mode, the input clock is derived from the external clock input at the TxCK pin.

The timer modes are determined by the following bits:

- TCS (TxCON<1>): Timer Clock Source Control bit
- TGATE (TxCON<6>): Timer Gate Control bit

Timer control bit settings for different operating modes are given in the Table 12-1.

TABLE 12-1: TIMER MODE SETTINGS

Mode	TCS	TGATE
Timer	0	0
Gated Timer	0	1
Synchronous Counter	1	x

12.1 16-Bit Operation

To configure any of the timers for individual 16-bit operation:

1. Clear the T32 bit corresponding to that timer.
2. Select the timer prescaler ratio using the TCKPS<1:0> bits.
3. Set the Clock and Gating modes using the TCS and TGATE bits.
4. Load the timer period value into the PRx register.
5. If interrupts are required, set the interrupt enable bit, TxIE. Use the priority bits, TxIP<2:0>, to set the interrupt priority.
6. Set the TON bit.

12.2 32-Bit Operation

A 32-bit timer module can be formed by combining a Type B and a Type C 16-bit timer module. For 32-bit timer operation, the T32 control bit in the Type B Timer Control (TxCON<3>) register must be set. The Type C timer holds the most significant word (msw) and the Type B timer holds the least significant word (lsw) for 32-bit operation.

When configured for 32-bit operation, only the Type B Timer Control (TxCON) register bits are required for setup and control while the Type C Timer Control register bits are ignored (except the TSIDL bit).

For interrupt control, the combined 32-bit timer uses the interrupt enable, interrupt flag and interrupt priority control bits of the Type C timer. The interrupt control and status bits for the Type B timer are ignored during 32-bit timer operation.

The Timer2 and Timer 3 that can be combined to form a 32-bit timer are listed in Table 12-2.

TABLE 12-2: 32-BIT TIMER

Type B Timer (lsw)	Type C Timer (msw)
Timer2	Timer3

A block diagram representation of the 32-bit timer module is shown in Figure 12-3. The 32-timer module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode

To configure the features of Timer2/3 for 32-bit operation:

1. Set the T32 control bit.
2. Select the prescaler ratio for Timer2 using the TCKPS<1:0> bits.
3. Set the Clock and Gating modes using the corresponding TCS and TGATE bits.
4. Load the timer period value. PR3 contains the most significant word of the value, while PR2 contains the least significant word.
5. If interrupts are required, set the interrupt enable bit, T3IE. Use the priority bits, T3IP<2:0>, to set the interrupt priority. While Timer2 controls the timer, the interrupt appears as a Timer3 interrupt.
6. Set the corresponding TON bit.

The timer value at any point is stored in the register pair, TMR3:TMR2, which always contains the most significant word of the count, while TMR2 contains the least significant word.

REGISTER 15-1: PTCON: PWM TIME BASE CONTROL REGISTER

R/W-0	U-0	R/W-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU(1)	SYNCPOL(1)	SYNCOEN(1)
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCEN(1)	—	SYNCSRC1(1)	SYNCSRC0(1)	SEVTPS3(1)	SEVTPS2(1)	SEVTPS1(1)	SEVTPS0(1)
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PTEN:** PWM Module Enable bit
1 = PWM module is enabled
0 = PWM module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **PTSIDL:** PWM Time Base Stop in Idle Mode bit
1 = PWM time base halts in CPU Idle mode
0 = PWM time base runs in CPU Idle mode

bit 12 **SESTAT:** Special Event Interrupt Status bit
1 = Special event interrupt is pending
0 = Special event interrupt is not pending

bit 11 **SEIEN:** Special Event Interrupt Enable bit
1 = Special event interrupt is enabled
0 = Special event interrupt is disabled

bit 10 **EIPU:** Enable Immediate Period Updates bit(1)
1 = Active Period register is updated immediately
0 = Active Period register updates occur on PWM cycle boundaries

bit 9 **SYNCPOL:** Synchronization Input/Output Polarity bit(1)
1 = SYNCIx and SYNCO polarity is inverted (active-low)
0 = SYNCIx and SYNCO are active-high

bit 8 **SYNCOEN:** Primary Time Base Sync Enable bit(1)
1 = SYNCO output is enabled
0 = SYNCO output is disabled

bit 7 **SYNCEN:** External Time Base Synchronization Enable bit(1)
1 = External synchronization of primary time base is enabled
0 = External synchronization of primary time base is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **SYNCSRC<1:0>:** Synchronous Source Selection bits(1)
11 = Reserved
10 = Reserved
01 = SYNCI2
00 = SYNCI1

Note 1: These bits should be changed only when PTEN = 0. In addition, when using the SYNCIx feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

REGISTER 15-11: DTRx: PWMx DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTRx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-0 **DTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 15-12: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ALTDTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALTDTR <7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-0 **ALTDTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

16.0 SERIAL PERIPHERAL INTERFACE (SPI)

Note 1: This data sheet summarizes the features of the dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Serial Peripheral Interface (SPI)"** (DS70206) in the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available on the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Serial Peripheral Interface (SPI) module is a synchronous serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, Analog-to-Digital Converters and so on. The SPI module is compatible with SPI and SIOP from Motorola®.

The SPI module consists of a 16-bit shift register, SPIxSR (where x = 1), used for shifting data in and out, and a buffer register, SPIxBUF. A control register, SPIxCON, configures the module. Additionally, a status register, SPIxSTAT, indicates status conditions.

The serial interface consists of the following four pins:

- SDIx (Serial Data Input)
- SDOx (Serial Data Output)
- SCKx (Shift Clock Input Or Output)
- $\overline{\text{SSx}}$ (Active-Low Slave Select).

In Master mode operation, SCK is a clock output; in Slave mode, it is a clock input.

FIGURE 16-1: SPIx MODULE BLOCK DIAGRAM

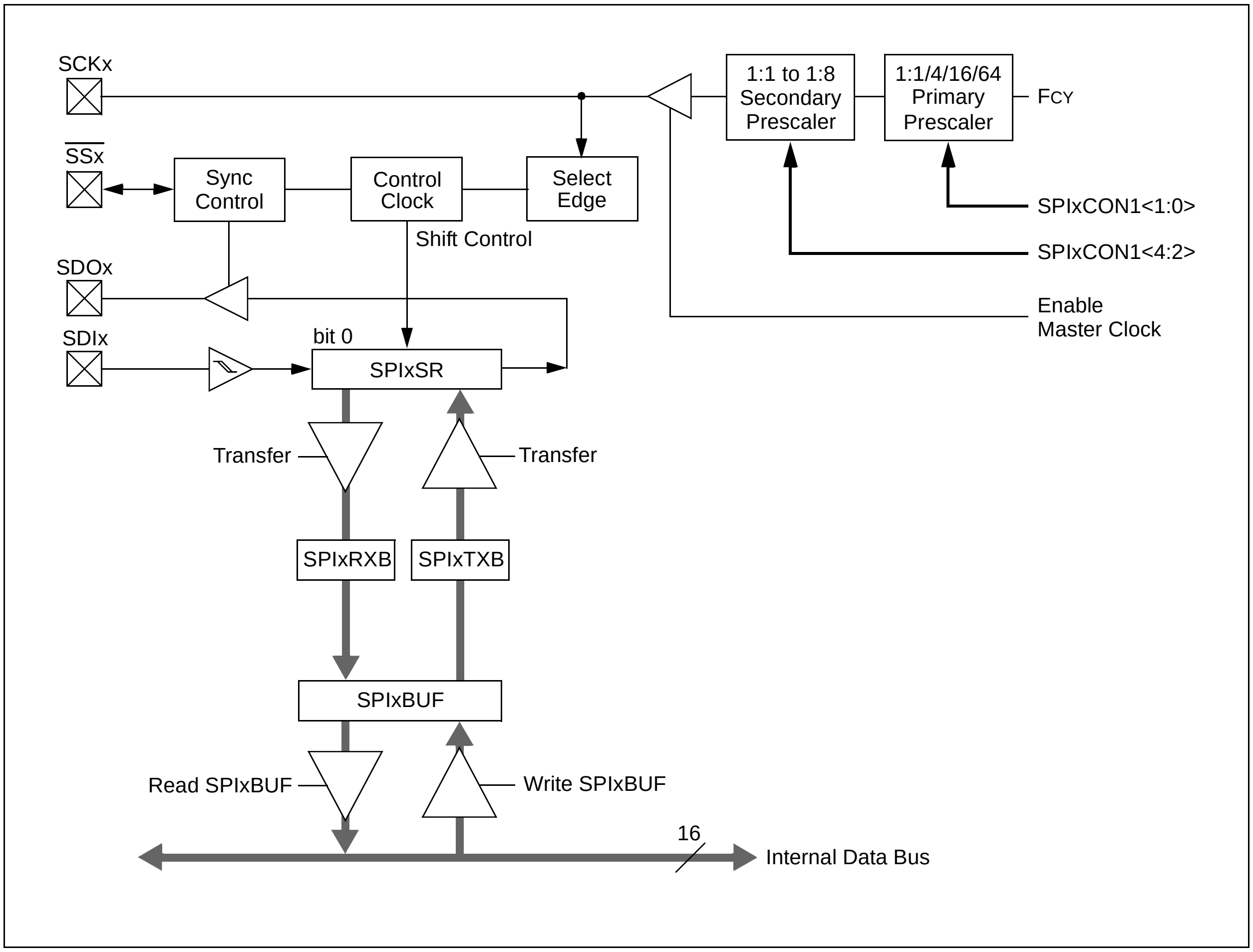
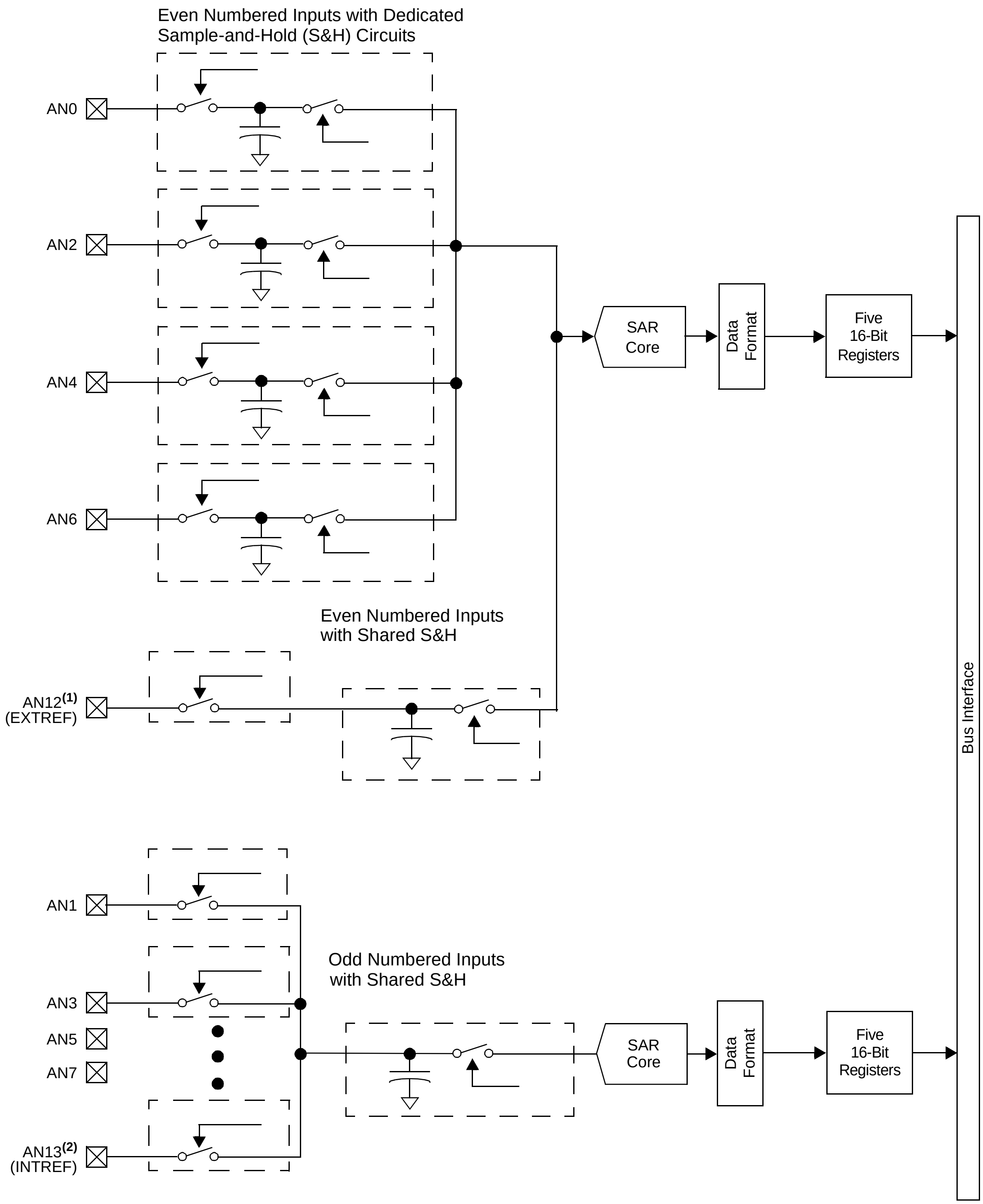


FIGURE 19-5: ADC BLOCK DIAGRAM FOR dsPIC33FJ16GS502 DEVICES WITH TWO SARS



Note 1: AN12 (EXTREF) is an internal analog input. To measure the voltage at AN12 (EXTREF), an analog comparator must be enabled and EXTREF must be selected as the comparator reference.

2: AN13 (INTREF) is an internal analog input and is not available on a pin.

REGISTER 19-7: ADCPC2: ANALOG-TO-DIGITAL CONVERT PAIR CONTROL REGISTER 2[1] (CONTINUED)

bit 4-0 **TRGSRC4<4:0>:** Trigger 4 Source Selection bits

Selects trigger source for conversion of Analog Channels AN9 and AN8.
`11111` = Timer2 period match
•
•
•
`11011` = Reserved
`11010` = PWM Generator 4 current-limit ADC trigger
`11001` = PWM Generator 3 current-limit ADC trigger
`11000` = PWM Generator 2 current-limit ADC trigger
`10111` = PWM Generator 1 current-limit ADC trigger
`10110` = Reserved
•
•
•
`10010` = Reserved
`10001` = PWM Generator 4 secondary trigger is selected
`10000` = PWM Generator 3 secondary trigger is selected
`01111` = PWM Generator 2 secondary trigger is selected
`01110` = PWM Generator 1 secondary trigger is selected
`01101` = Reserved
`01100` = Timer1 period match
•
•
•
`01000` = Reserved
`00111` = PWM Generator 4 primary trigger is selected
`00110` = PWM Generator 3 primary trigger is selected
`00101` = PWM Generator 2 primary trigger is selected
`00100` = PWM Generator 1 primary trigger is selected
`00011` = PWM Special Event Trigger is selected
`00010` = Global software trigger is selected
`00001` = Individual software trigger is selected
`00000` = No conversion is enabled

Note 1: This register is only implemented in the dsPIC33FJ16GS504 devices.

2: The trigger source must be set as a global software trigger prior to setting this bit to '1'. If other conversions are in progress, then the conversion will be performed when the conversion resources are available.

23.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

23.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

TABLE 24-24: TIMER2 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic		Min.	Typ.	Max.	Units	Conditions
TB10	TTXH	T2CK High Time	Synchronous	Greater of: 20 ns or (TCY + 20)/N	—	—	ns	Must also meet Parameter TB15, N = Prescale value (1, 8, 64, 256)
TB11	TTXL	T2CK Low Time	Synchronous	Greater of: 20 ns or (TCY + 20)/N	—	—	ns	Must also meet Parameter TB15, N = Prescale value (1, 8, 64, 256)
TB15	TTXP	T2CK Input Period	Synchronous	Greater of: 40 ns or (2 TCY + 40)/N	—	—	ns	N = Prescale value (1, 8, 64, 256)
TB20	TCKEXTMRL	Delay from External T2CK Clock Edge to Timer Increment		0.75 TCY + 40	—	1.75 TCY + 40	ns	

TABLE 24-25: TIMER3 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
TC10	TTXH	T3CK High Time	Synchronous	TCY + 20	—	—	ns	Must also meet Parameter TC15
TC11	TTXL	T3CK Low Time	Synchronous	TCY + 20	—	—	ns	Must also meet Parameter TC15
TC15	TTXP	T3CK Input Period	Synchronous, with prescaler	2 TCY + 40	—	—	ns	
TC20	TCKEXTMRL	Delay from External T3CK Clock Edge to Timer Increment		0.75 TCY + 40	—	1.75 TCY + 40	—	

TABLE 24-40: 10-BIT HIGH-SPEED ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 2): 3.0V and 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	—	—	—	—	AVDD is internally connected to VDD; see Parameter DC10 in Table 24-4
AD02	AVSS	Module VSS Supply	—	—	—	—	AVSS is internally connected to VSS
Analog Input							
AD10	VINH-VINL	Full-Scale Input Span	VSS	—	VDD	V	
AD11	VIN	Absolute Input Voltage	AVSS	—	AVDD	V	
AD12	IAD	Operating Current	—	8	—	mA	
AD13	—	Leakage Current	—	±0.6	—	μA	VINL = AVSS = 0V, AVDD = 3.3V, Source Impedance = 100Ω
AD17	RIN	Recommended Impedance Of Analog Voltage Source	—	—	100	Ω	
DC Accuracy @ 1.5 Msps							
AD20A	Nr	Resolution	10 Data Bits				
AD21A	INL	Integral Nonlinearity	-0.5	-0.3/+0.5	+1.2	LSb	
AD22A	DNL	Differential Nonlinearity	-0.9	±0.6	+0.9	LSb	
AD23A	GERR	Gain Error	13	15	22	LSb	
AD24A	EOFF	Offset Error	6	7	8	LSb	
AD25A	—	Monotonicity(1)	—	—	—	—	Guaranteed
DC Accuracy @ 1.7 Msps							
AD20B	Nr	Resolution	10 Data Bits				
AD21B	INL	Integral Nonlinearity	-0.5	-0.4/+1.1	+1.8	LSb	
AD22B	DNL	Differential Nonlinearity	-1.0	±1.0	+1.5	LSb	
AD23B	GERR	Gain Error	13	15	22	LSb	
AD24B	EOFF	Offset Error	6	7	8	LSb	
AD25B	—	Monotonicity(1)	—	—	—	—	Guaranteed
DC Accuracy @ 2.0 Msps							
AD20C	Nr	Resolution	10 Data Bits				
AD21C	INL	Integral Nonlinearity	-0.8	-0.5/+1.8	+2.8	LSb	
AD22C	DNL	Differential Nonlinearity	-1.0	-1.0/+1.8	+2.8	LSb	
AD23C	GERR	Gain Error	14	16	23	LSb	
AD24C	EOFF	Offset Error	6	7	8	LSb	
AD25C	—	Monotonicity(1)	—	—	—	—	Guaranteed
Dynamic Performance							
AD30	THD	Total Harmonic Distortion	—	-73	—	dB	
AD31	SINAD	Signal to Noise and Distortion	—	58	—	dB	
AD32	SFDR	Spurious Free Dynamic Range	—	-73	—	dB	
AD33	FNYQ	Input Signal Bandwidth	—	—	1	MHz	
AD34	ENOB	Effective Number of Bits	—	9.4	—	bits	

Note 1: The Analog-to-Digital conversion result never decreases with an increase in input voltage, and has no missing codes.

2: Module is functional at VBOR < VDD < VDDMIN, but with degraded performance. Module functionality is tested but not characterized.

TABLE 25-5: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +150°C for High Temperature				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
DO10	V_{OL}	**Output Low Voltage** I/O Pins: 4x Sink Driver Pins – RA0-RA2, RB0-RB2, RB5-RB10, RB15, RC1, RC2, RC9, RC10	—	—	0.4	V	I_{OL} ≤ 3.6 mA, V_{DD} = 3.3V See **Note 1**
		Output Low Voltage I/O Pins: 8x Sink Driver Pins – RC0, RC3-RC8, RC11-RC13	—	—	0.4	V	I_{OL} ≤ 6 mA, V_{DD} = 3.3V See **Note 1**
		Output Low Voltage I/O Pins: 16x Sink Driver Pins – RA3, RA4, RB3, RB4, RB11-RB14	—	—	0.4	V	I_{OL} ≤ 12 mA, V_{DD} = 3.3V See **Note 1**
DO20	V_{OH}	**Output High Voltage** I/O Pins: 4x Source Driver Pins – RA0-RA2, RB0-RB2, RB5-RB10, RB15, RC1, RC2, RC9, RC10	2.4	—	—	V	I_{OL} ≥ -4 mA, V_{DD} = 3.3V See **Note 1**
		Output High Voltage I/O Pins: 8x Source Driver Pins – RC0, RC3-RC8, RC11-RC13	2.4	—	—	V	I_{OL} ≥ -8 mA, V_{DD} = 3.3V See **Note 1**
		Output High Voltage I/O Pins: 16x Source Driver Pins – RA3, RA4, RB3, RB4, RB11-RB14	2.4	—	—	V	I_{OL} ≥ -16 mA, V_{DD} = 3.3V See **Note 1**
DO20A	V_{OH1}	**Output High Voltage** I/O Pins: 4x Source Driver Pins – RA0-RA2, RB0-RB2, RB5-RB10, RB15, RC1, RC2, RC9, RC10	1.5	—	—	V	I_{OH} ≥ -3.9 mA, V_{DD} = 3.3V See **Note 1**
			2.0	—	—		I_{OH} ≥ -3.7 mA, V_{DD} = 3.3V See **Note 1**
			3.0	—	—		I_{OH} ≥ -2 mA, V_{DD} = 3.3V See **Note 1**
		Output High Voltage I/O Pins: 8x Source Driver Pins – RC0, RC3-RC8, RC11-RC13	1.5	—	—	V	I_{OH} ≥ -7.5 mA, V_{DD} = 3.3V See **Note 1**
			2.0	—	—		I_{OH} ≥ -6.8 mA, V_{DD} = 3.3V See **Note 1**
			3.0	—	—		I_{OH} ≥ -3 mA, V_{DD} = 3.3V See **Note 1**
		Output High Voltage I/O Pins: 16x Source Driver Pins – RA3, RA4, RB3, RB4, RB11-RB14	1.5	—	—	V	I_{OH} ≥ -15 mA, V_{DD} = 3.3V See **Note 1**
			2.0	—	—		I_{OH} ≥ -14 mA, V_{DD} = 3.3V See **Note 1**
			3.0	—	—		I_{OH} ≥ -7 mA, V_{DD} = 3.3V See **Note 1**

Note 1: Parameters are characterized, but not tested.

TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 24.0 "Electrical Characteristics"	Updated Typical values for Thermal Packaging Characteristics (see Table 24-3). Updated Min and Max values for Parameter DC12 (RAM Data Retention Voltage) and added Note 4 (see Table 24-4). Updated Characteristics for I/O Pin Input Specifications (see Table 24-9). Added ISOURCE to I/O Pin Output Specifications (see Table 24-10). Updated Program Memory values for Parameters 136, 137, and 138 (renamed to 136a, 137a, and 138a), added Parameters 136b, 137b, and 138b, and added Note 2 (see Table 24-12). Added Parameter OS42 (GM) to the External Clock Timing Requirements (see Table 24-16). Updated Conditions for symbol TPDLY (Tap Delay) and added symbol ACLK (PWM Input Clock) to the High-Speed PWM Module Timing Requirements (see Table 24-29). Updated Parameters AD01 and AD02 in the 10-bit High-Speed Analog-to-Digital Module Specifications (see Table 24-36). Updated Parameters AD50b, AD55b, and AD56b, and removed Parameters AD57b and AD60b from the 10-bit High-Speed Analog-to-Digital Module Timing Requirements (see Table 24-37).